

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch CD4724BM/CD4724BC 8-Bit Addressable Latch

General Description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input (\bar{E}), and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0–Q3). The CD4724B is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input (\bar{E}), active high clear input (CL), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable (\bar{E}) is low. Data entry is inhibited when enable (\bar{E}) is high.

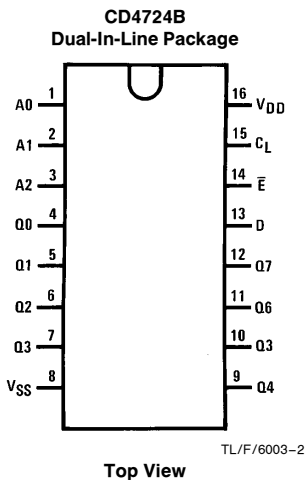
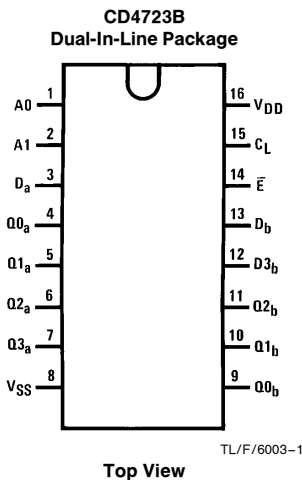
When clear (CL) and enable (\bar{E}) are high, all outputs are low. When clear (CL) is high and enable (\bar{E}) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the address-

able latch mode ($\bar{E} = CL = \text{low}$), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\bar{E} = \text{high}$, $CL = \text{low}$).

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagrams



Order Number CD4723B or
CD4724B

Truth Table

| Mode Selection | | | | |
|----------------|----|--------------------|---------------------|--------------------------|
| \bar{E} | CL | Addressed Latch | Unaddressed Latch | Mode |
| L | L | Follows Data | Holds Previous Data | Addressable Latch Memory |
| H | L | Hold Previous Data | Holds Previous Data | |
| L | H | Follows Data | Reset to "0" | Demultiplexer |
| H | H | Reset to "0" | Reset to "0" | Clear |

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|----------------------------------|
| DC Supply Voltage (V_{DD}) | -0.5V to +18 V_{DC} |
| Input Voltage (V_{IN}) | -0.5V to V_{DD} + 0.5 V_{DC} |
| Storage Temperature (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|---------------------------------------|-------------------------|
| DC Supply Voltage (V_{DD}) | 3.0V to 15 V_{DC} |
| Input Voltage (V_{IN}) | 0V to V_{DD} V_{DC} |
| Operating Temperature Range (T_A) | |
| CD4723BM/CD4724BM | -55°C to +125°C |
| CD4723BC/CD4724BC | -40°C to +85°C |

DC Electrical Characteristics CD4723BM/CD4724BM (Note 2)

| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|------------------------------------|-------------------------------------|-------|------|-------|------------|------|--------|------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ | | 5.0 | | 0.02 | 5.0 | | 150 | μA |
| | | $V_{DD} = 10V$ | | 10 | | 0.02 | 10 | | 300 | μA |
| | | $V_{DD} = 15V$ | | 20 | | 0.02 | 20 | | 600 | μA |
| V_{OL} | Low Level Output Voltage | $ I_O \leq 1 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| V_{OH} | High Level Output Voltage | $ I_O \leq 1 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5.0 | | 4.95 | | V |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| V_{IL} | Low Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or 4.5V | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1V$ or 9V | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or 13.5V | | 4.0 | | 6.75 | 4.0 | | 4.0 | V |
| V_{IH} | High Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or 4.5V | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 1V$ or 9V | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or 13.5V | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| I_{OL} | Low Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 0.4V$ | 0.64 | | 0.51 | 0.88 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.6 | | 1.3 | 2.25 | | 0.9 | | mA |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 4.2 | | 3.4 | 8.8 | | 2.4 | | mA |
| I_{OH} | High Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 4.6V$ | -0.64 | | -0.51 | -0.88 | | -0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -1.6 | | -1.3 | -2.25 | | -0.9 | | mA |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -4.2 | | -3.4 | -8.8 | | -2.4 | | mA |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.1 | | -10^{-5} | -0.1 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | 10^{-5} | 0.1 | | 1.0 | μA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4723BC/CD4724BC (Note 2)

| Symbol | Parameter | Conditions | - 40°C | | + 25°C | | | + 85°C | | Units |
|-----------------|------------------------------------|---|--------|-------|--------|-------------------|-------|--------|------|-------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I _{DD} | Quiescent Device Current | V _{DD} = 5V | | 20 | | 0.02 | 20 | | 150 | μA |
| | | V _{DD} = 10V | | 40 | | 0.02 | 40 | | 300 | μA |
| | | V _{DD} = 15V | | 80 | | 0.02 | 80 | | 600 | μA |
| V _{OL} | Low Level Output Voltage | I _O ≤ 1 μA | | | | | | | | |
| | | V _{DD} = 5V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | V _{DD} = 10V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | V _{DD} = 15V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| V _{OH} | High Level Output Voltage | I _O ≤ 1 μA | | | | | | | | |
| | | V _{DD} = 5V | 4.95 | | 4.95 | 5.0 | | 4.95 | | V |
| | | V _{DD} = 10V | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | V _{DD} = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| V _{IL} | Low Level Input Voltage | V _{DD} = 5V, V _O = 0.5V or 4.5V | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | V _{DD} = 10V, V _O = 1V or 9V | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | V _{DD} = 15V, V _O = 1.5V or 13.5V | | 4.0 | | 6.75 | 4.0 | | 4.0 | V |
| V _{IH} | High Level Input Voltage | V _{DD} = 5V, V _O = 0.5V or 4.5V | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | V _{DD} = 10V, V _O = 1V or 9V | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | V _{DD} = 15V, V _O = 1.5V or 13.5V | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| I _{OL} | Low Level Output Current (Note 3) | V _{DD} = 5V, V _O = 0.4V | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | V _{DD} = 10V, V _O = 0.5V | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | V _{DD} = 15V, V _O = 1.5V | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| I _{OH} | High Level Output Current (Note 3) | V _{DD} = 5V, V _O = 4.6V | -0.52 | | -0.44 | -0.88 | | -0.36 | | mA |
| | | V _{DD} = 10V, V _O = 9.5V | -1.3 | | -1.1 | -2.25 | | -0.9 | | mA |
| | | V _{DD} = 15V, V _O = 13.5V | -3.6 | | -3.0 | -8.8 | | -2.4 | | mA |
| I _{IN} | Input Current | V _{DD} = 15V, V _{IN} = 0V | | -0.30 | | -10 ⁻⁵ | -0.30 | | -1.0 | μA |
| | | V _{DD} = 15V, V _{IN} = 15V | | 0.30 | | 10 ⁻⁵ | 0.30 | | 1.0 | μA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, Input $t_r = t_f = 20\text{ ns}$, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|--|-------------------------|-----|-----|-----|-------|
| t_{PHL} , t_{PLH} | Propagation Delay Data to Output | $V_{DD} = 5\text{V}$ | | 200 | 400 | ns |
| | | $V_{DD} = 10\text{V}$ | | 75 | 150 | ns |
| | | $V_{DD} = 15\text{V}$ | | 50 | 100 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay Enable to Output | $V_{DD} = 5\text{V}$ | | 200 | 400 | ns |
| | | $V_{DD} = 10\text{V}$ | | 80 | 160 | ns |
| | | $V_{DD} = 15\text{V}$ | | 60 | 120 | ns |
| t_{PHL} | Propagation Delay Clear to Output | $V_{DD} = 5\text{V}$ | | 175 | 350 | ns |
| | | $V_{DD} = 10\text{V}$ | | 80 | 160 | ns |
| | | $V_{DD} = 15\text{V}$ | | 65 | 130 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay Address to Output | $V_{DD} = 5\text{V}$ | | 225 | 450 | ns |
| | | $V_{DD} = 10\text{V}$ | | 100 | 200 | ns |
| | | $V_{DD} = 15\text{V}$ | | 75 | 150 | ns |
| t_{THL} , t_{TLH} | Transition Time (Any Output) | $V_{DD} = 5\text{V}$ | | 100 | 200 | ns |
| | | $V_{DD} = 10\text{V}$ | | 50 | 100 | ns |
| | | $V_{DD} = 15\text{V}$ | | 40 | 80 | ns |
| T_{WH} , T_{WL} | Minimum Data Pulse Width | $V_{DD} = 5\text{V}$ | | 100 | 200 | ns |
| | | $V_{DD} = 10\text{V}$ | | 50 | 100 | ns |
| | | $V_{DD} = 15\text{V}$ | | 40 | 80 | ns |
| t_{WH} , t_{WL} | Minimum Address Pulse Width | $V_{DD} = 5\text{V}$ | | 200 | 400 | ns |
| | | $V_{DD} = 10\text{V}$ | | 100 | 200 | ns |
| | | $V_{DD} = 15\text{V}$ | | 65 | 125 | ns |
| t_{WH} | Minimum Clear Pulse Width | $V_{DD} = 5\text{V}$ | | 75 | 150 | ns |
| | | $V_{DD} = 10\text{V}$ | | 40 | 75 | ns |
| | | $V_{DD} = 15\text{V}$ | | 25 | 50 | ns |
| t_{SU} | Minimum Setup Time Data to E | $V_{DD} = 5\text{V}$ | | 40 | 80 | ns |
| | | $V_{DD} = 10\text{V}$ | | 20 | 40 | ns |
| | | $V_{DD} = 15\text{V}$ | | 15 | 30 | ns |
| t_H | Minimum Hold Time Data to E | $V_{DD} = 5\text{V}$ | | 60 | 120 | ns |
| | | $V_{DD} = 10\text{V}$ | | 30 | 60 | ns |
| | | $V_{DD} = 15\text{V}$ | | 25 | 50 | ns |
| t_{SU} | Minimum Setup Time Address to E | $V_{DD} = 5\text{V}$ | | -15 | 50 | ns |
| | | $V_{DD} = 10\text{V}$ | | 0 | 30 | ns |
| | | $V_{DD} = 15\text{V}$ | | 0 | 20 | ns |
| t_H | Minimum Hold Time Address to E | $V_{DD} = 5\text{V}$ | | -50 | 15 | ns |
| | | $V_{DD} = 10\text{V}$ | | -20 | 10 | ns |
| | | $V_{DD} = 15\text{V}$ | | -15 | 5 | ns |
| C_{PD} | Power Dissipation Capacitance | Per Package (Note 4) | | 100 | | pF |
| C_{IN} | Input Capacitance | Any Input | | 5.0 | 7.5 | pF |

*AC Parameters are guaranteed by DC correlated testing.

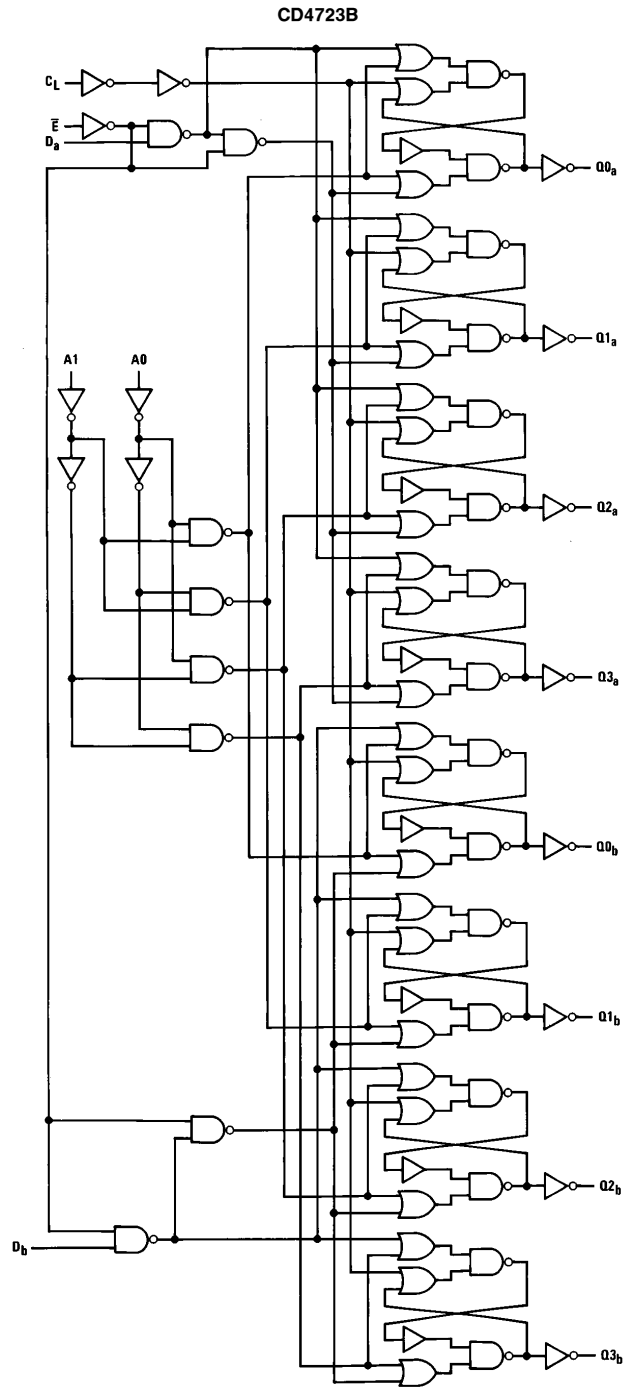
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see Application Note AN-90, "54C/74C Family Characteristics".

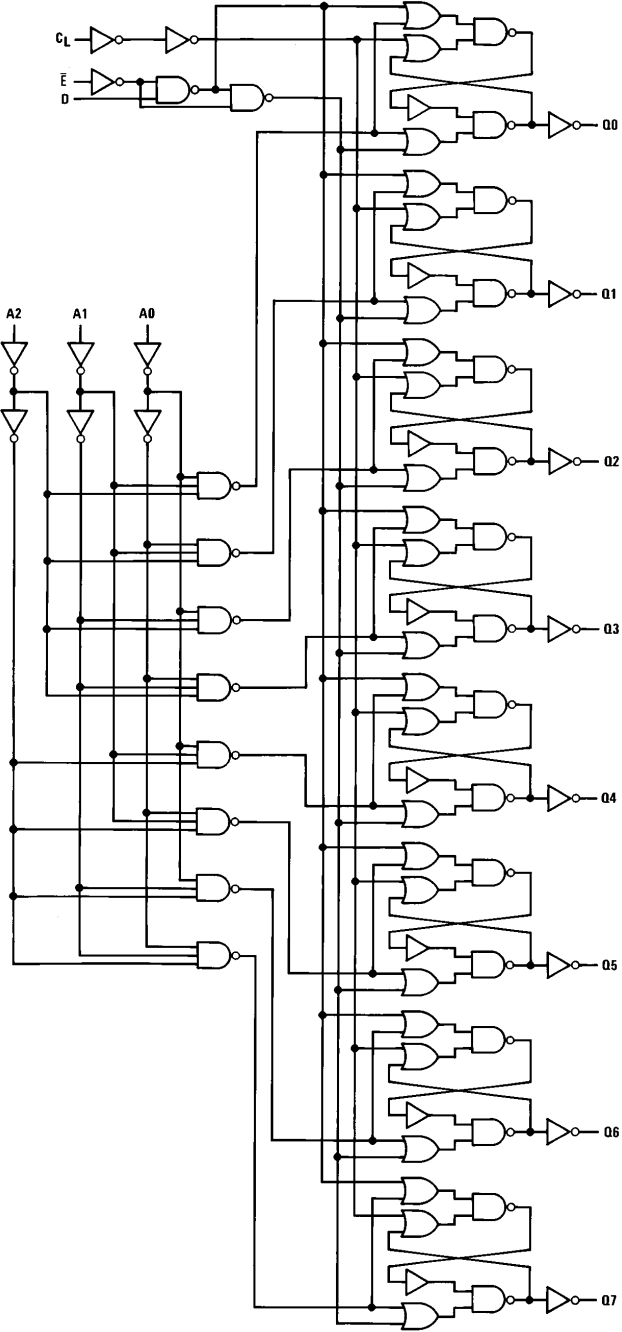
Logic Diagrams



TL/F/6003-3

Logic Diagrams (Continued)

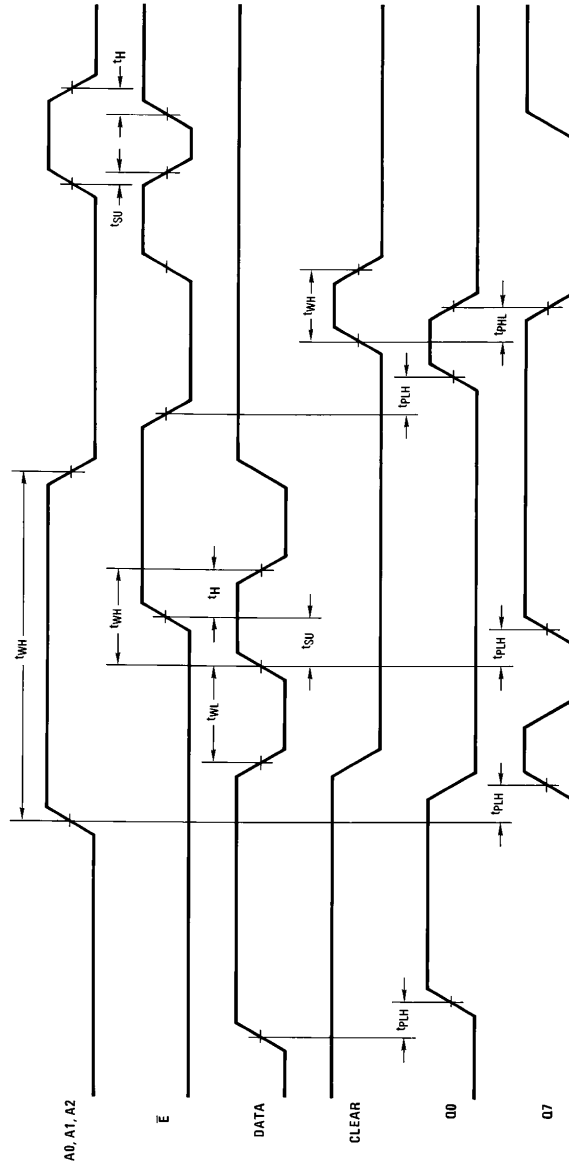
CD4724B



TL/F/6003-4

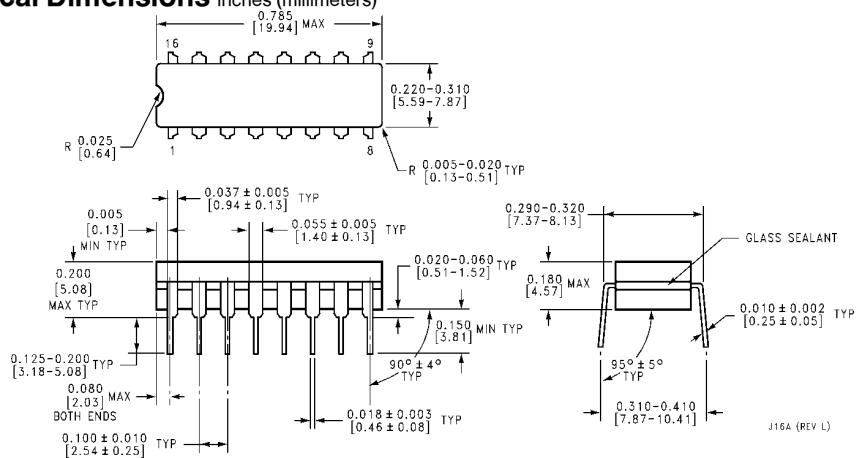
Switching Time Waveforms

TL/F/6000-5

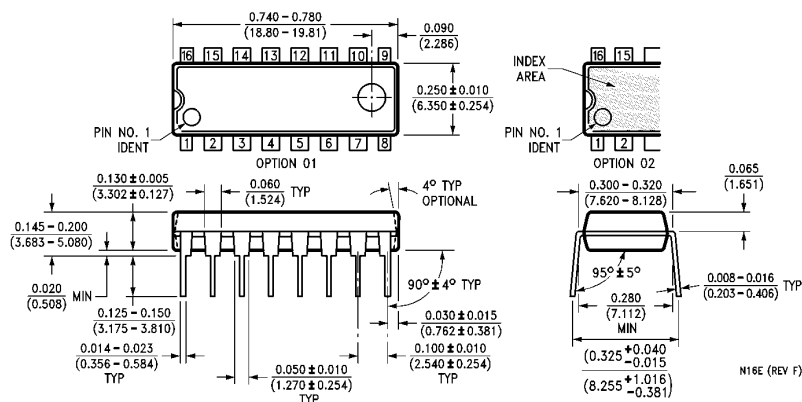


**CD4723BM/CD4723BC Dual 4-Bit Addressable Latch
CD4724BM/CD4724BC 8-Bit Addressable Latch**

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4723BMJ, CD4723BCJ, CD4724BMJ or CD4724BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD4723BMN, CD4723BCN, CD4724BMN or CD4724BCN
NS Package Number N16E

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