FM24C04

4Kb FRAM Serial Memory

Features

4K bit Ferroelectric Nonvolatile RAM

- Organized as 512 x 8 bits
- High endurance 10 Billion (10^{10}) read/writes
- 10 year data retention at 85° C
- No write delay
- Advanced high-reliability ferroelectric process

Fast Two-wire Serial Interface

- Up to 400 kHz maximum bus frequency
- Direct hardware replacement for EEPROM

Low Power Operation

- True 5V operation
- 150 µA Active current (100 kHz)
- 10 µA standby current

Industry Standard Configuration

- Industrial temperature -40° C to +85° C
- 8-pin SOP or DIP

Description

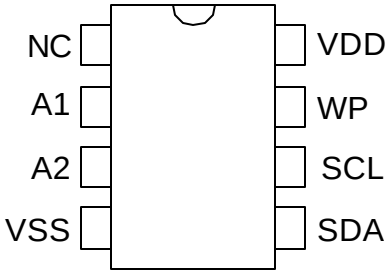
The FM24C04 is a 4-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory, or FRAM, is nonvolatile but operates in other respects as a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike serial EEPROMs, the FM24C04 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array mere hundreds of nanoseconds after it has been successfully transferred to the device. The next bus cycle may commence immediately. In addition the product offers substantial write endurance compared with other nonvolatile memories. The FM24C04 is capable of supporting up to 1E10 read/write cycles -- far more than most systems will require from a serial memory.

These capabilities make the FM24C04 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24C04 provides substantial benefits to users of serial EEPROM, yet these benefits are available in a hardware drop-in replacement. The FM24C04 is provided in industry standard 8-pin packages using a familiar two-wire protocol. They are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Names	Function
A1	Device Select Address 1
A2	Device Select Address 2
SDA	Serial Data/address
SCL	Serial Clock
WP	Write Protect
VSS	Ground
VDD	Supply Voltage 5V

Ordering Information	
FM24C04-P	8-pin plastic DIP
FM24C04-S	8-pin SOP

This data sheet contains design specifications for product development.
These specifications may change in any manner without notice

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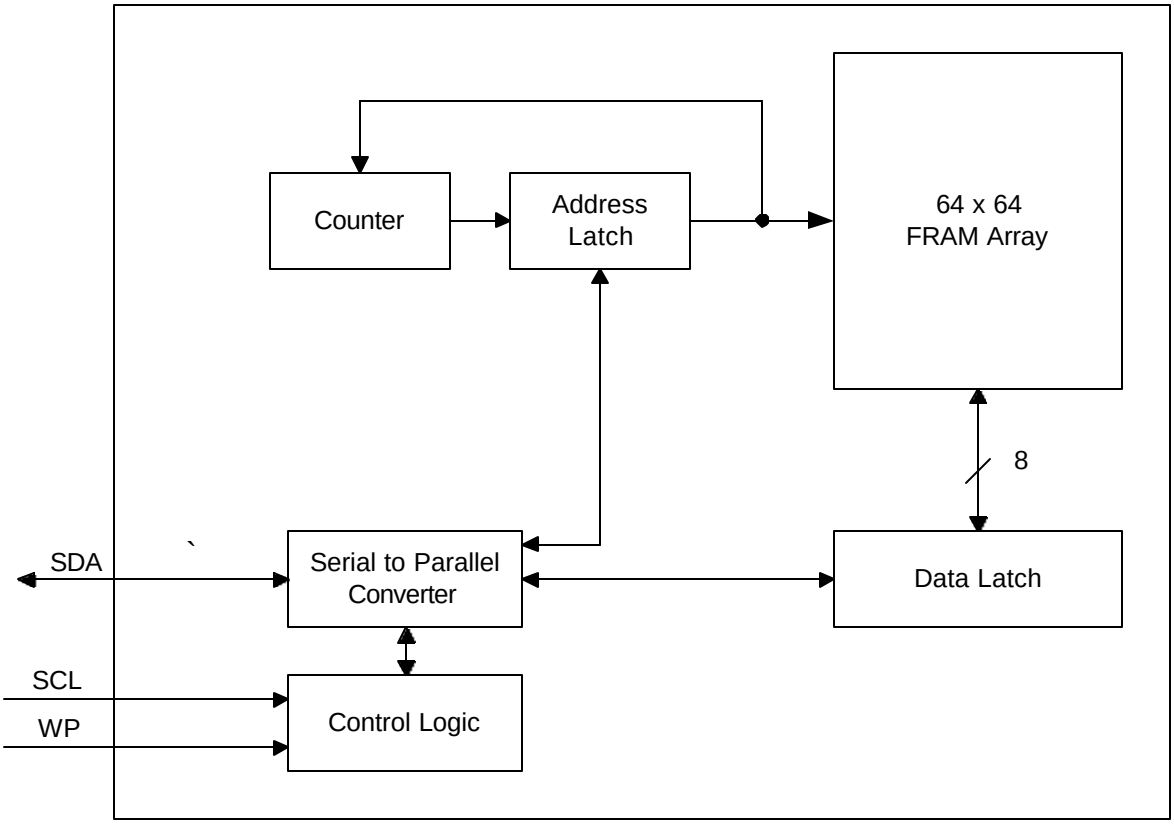
Figure 1. Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Pin Description
NC	1		No connect.
A1-A2	2-3	I	Address 1, 2. The address pins set the device address. The device address value in the 2-wire slave address must match the setting of these two pins.
VSS	4	I	Ground
SDA	5	I/O	Serial Data Address. This is a bi-directional data line for the two-wire interface. It is open-drain and is intended to be wire-ORed with other devices on the two-wire bus. The input buffer incorporates a schmitt trigger for noise immunity and the output driver includes slope control for falling edges.
SCL	6	I	Serial Clock. The serial clock line for the two-wire interface. Data is clocked out of the part on the falling edge and in on the rising edge.
WP	7	I	Write Protect. When tied to VDD, addresses in the upper half of the logical memory map (A0=1 in the slave address) will be write-protected. Write access to the lower half of the addresses is permitted. When WP is connected to ground, all addresses may be written. This pin must not be left floating.
VDD	8	I	Supply Voltage. 5V

Overview

The FM24C04 is a serial FRAM memory. The memory array is logically organized as 512 x 8 and is accessed using an industry standard two-wire interface. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM24C04 and a serial EEPROM with the same pin-out relates to its superior write performance.

Memory Architecture

When accessing the FM24C04, the user addresses 512 locations each with 8 data bits. These data bits are shifted serially. The 512 addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish other devices), a page address, and a word address. The word address consists of 8-bits that specify one of 256 addresses. The page address is 1-bit and so there are 2 pages each of 256 locations. The complete address of 9-bits specifies each byte address uniquely.

Most functions of the FM24C04 either are controlled by the two-wire interface or are handled automatically by on-board circuitry. The access time for memory operation essentially is zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the two-wire bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section below.

Users expect several obvious system benefits from the FM24C04 due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM24C04 contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Two-wire Interface

The FM24C04 employs a bi-directional two-wire bus protocol using few pins and little board space. Figure 2 illustrates a typical system configuration using the FM24C04 in a microcontroller-based system. The industry standard two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24C04 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including start, stop, data bit, or acknowledge. Figure 3 illustrates the signal conditions that specify the four states. Detailed timing diagrams are in the electrical specifications.

Figure 2. Typical System Configuration

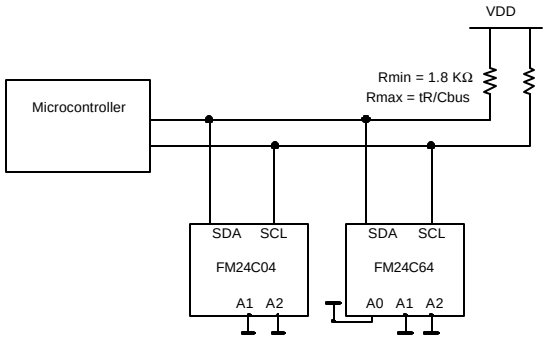
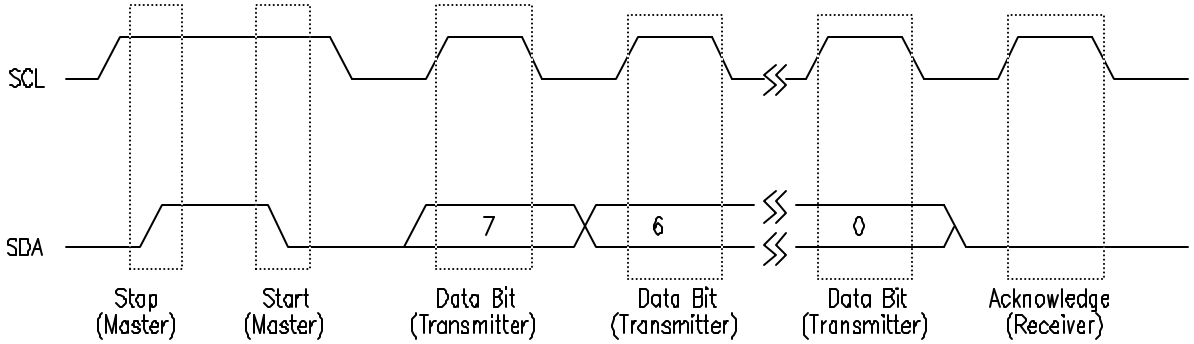


Figure 3. Data Transfer Protocol



Start Condition

A start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All commands must be preceded by a start condition. An operation in progress can be aborted by asserting a start condition at any time. Aborting an operation using the start condition will ready the FM24C04 for a new operation.

If during operation the power supply drops below the specified VDD minimum, the system should issue a start condition prior to performing another operation.

Stop Condition

A stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations using the FM24C04 should end with a stop condition. If an operation is in progress when a stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a stop condition.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high.

Acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case the no-acknowledge ceases the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24C04 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24C04 to attempt to drive the bus on the next clock while the master is sending a new command such as stop.

Slave Address

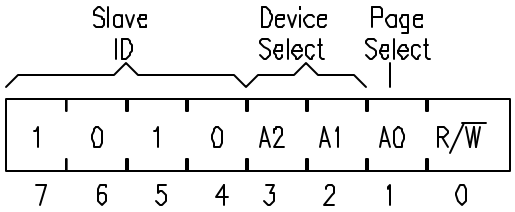
The first byte that the FM24C04 expects after a start condition is the slave address. As shown in Figure 4, the slave address contains the device type, the device select, the page of memory to be accessed, and a bit that specifies if the transaction is a read or a write.

Bits 7-4 are the device type and should be set to 1010b for the FM24C04. The device type allows other types of functions to reside on the 2-wire bus within an identical address range. Bits 3-2 are the device address. If bit 3 matches the A2 pin and bit 2 matches the A1 pin the device will be selected. Bit 1 is the page select. It specifies the 256-byte block of memory that is targeted for the current operation. Bit 0 is the read/write bit. A 0 indicates a write operation.

Word Address

After the FM24C04 (as receiver) acknowledges the slave ID, the master will place the word address on the bus for a write operation. The word address is the lower 8-bits of the address to be combined with the 1-bit page select to specify exactly the byte to be written. The complete 9-bit address is latched internally.

Figure 4. Slave Address



No word address occurs for a read operation. Reads always use the lower 8-bits that are held internally in the address latch and the 9th address bit is part of the slave address. Reads always begin at the address following the previous access. A random read address can be loaded by doing a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24C04 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (1FFh) is reached, the address latch will roll over to 000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After all address information has been transmitted, data transfer between the bus master and the FM24C04 can begin. For a read operation the FM24C04 will place 8 data bits on the bus then wait for an acknowledge. If the acknowledge occurs, the next sequential byte will be transferred. If the acknowledge is not sent, the read operation is concluded. For a write operation, the FM24C04 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24C04 is designed to operate in a manner very similar to other 2-wire interface memory products. The major differences result from the higher performance write capability of FRAM technology. These improvements result in some differences between the FM24C04 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave address then a word address as mentioned above. The bus master indicates a write operation by setting the LSB of the Slave address to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 1FFh to 000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a done condition.

An actual memory array write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore if the user desires to abort a write without altering the memory contents, this should be done using a start or stop condition prior to the 8th data bit. The FM24C04 needs no page buffering.

Portions of the memory array can be write protected using the WP pin. Setting the WP pin to a high condition (VDD) will write-protect addresses from 100h to 1FFh. The FM24C04 will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a low state (VSS) will deactivate this feature. WP must not be left floating.

Figure 5 below illustrates both a single-byte and multiple-write.

Figure 5 Byte Write

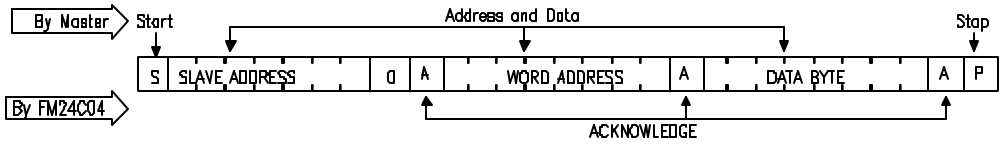
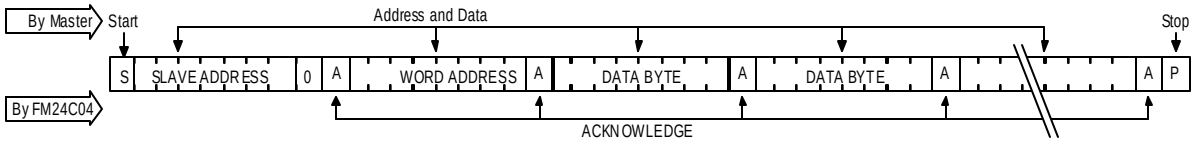


Figure 6 Multiple Byte Write



Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24C04 uses the internal address latch to supply the lower 8 address bits. In a selective read, the user performs a procedure to set these lower address bits to a specific value.

Current Address & Sequential Read

As mentioned above the FM24C04 uses an internal latch to supply the lower 8 address bits for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. This is the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to 1. This indicates that a read operation is requested. The page select bit in the slave address specifies the block of memory that is used for the read operation. After the acknowledge, the FM24C04 will begin shifting out data from the current address. The current address is the bit from the slave address combined with the 8 bits that were in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented. Each time the bus master acknowledges a byte, this indicates that the FM24C04 should read out the next sequential byte. There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24C04 attempts to read out additional data onto the bus. The four valid methods are as follows.

1. The bus master issues a no-acknowledge in the 9th clock cycle and a stop in the 10th clock cycle. This is illustrated in the diagrams below. This is the preferred method.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a start in the 10th.
3. The bus master issues a stop in the 9th clock cycle. Bus contention may result.
4. The bus master issues a start in the 9th clock cycle. Bus contention may result.

If the internal address reaches 1FFh it will wrap around to 000h on the next read cycle. Figures 7 and 8 below show the proper operation for current address reads.

Selective (Random) Read

A simple technique allows a user to select a random address location as the starting point for a read operation. This involves using the first two bytes of a write operation to set the internal address byte followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the word address byte that is loaded into the internal address latch. After the FM24C04 acknowledges the word address, the bus master issues a start condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a 1. The operation is now a current address read. This operation is illustrated in Figure 9.

Figure 7 Current Address Read

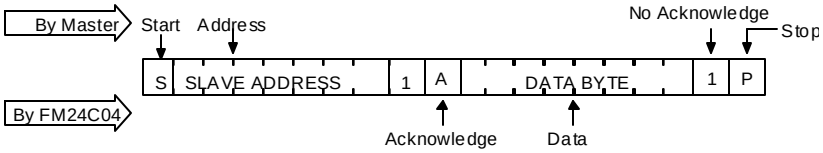


Figure 8 Sequential Read

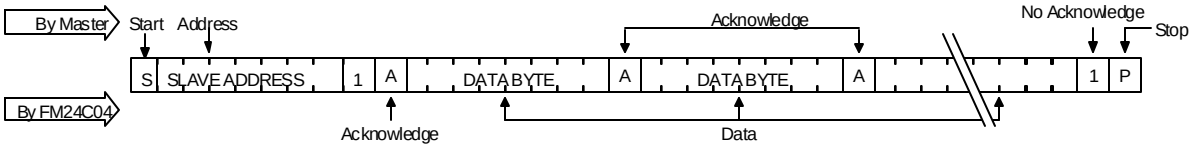
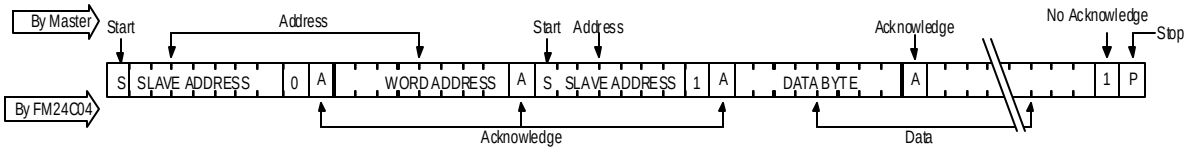


Figure 9 Selective (Random) Read



Data Retention and Endurance

Data retention is specified in the electrical specifications below. For purposes of clarity, this section contrasts the retention and endurance of FRAM with EEPROM. The retention performance of FRAM is very comparable to EEPROM in its characteristics. However, the effect of endurance cycles on retention is different.

A typical EEPROM has a write endurance specification that is fixed. Surpassing the specified level of cycles on an EEPROM usually leads to a hard memory failure. By contrast, the effect of increasing cycles on FRAM produces an increase in the soft error rate. That is, there is a higher likelihood of data loss but the memory continues to function properly. A hard failure would not occur by simply exceeding the endurance specification; simply a reduction in data retention reliability. While enough cycles would cause an apparent hard error, this is simply a very high soft error rate. This characteristic makes it problematic to assign a fixed endurance specification.

Endurance is a soft specification. Therefore, the user may operate the device with different levels of endurance cycling for different portions of the memory. For example, critical data needing the highest reliability level could be stored in memory locations that receive comparatively few cycles. Data with shorter-term use could be located in an area receiving many more cycles. A scratchpad area, needing little if any retention can be cycled until there is virtually no retention capability remaining. This would occur several orders of magnitude above the endurance spec.

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore, endurance cycles are applied for each access: read or write. The FRAM architecture is based on an array of rows and columns. Each access causes a cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles should not be located within the same row. In the FM24C04, there are 64 rows each 64 bits wide. Each 8 bytes in the address mark the beginning of a new row.

Applications

The versatility of FRAM technology fits into many diverse applications. Clearly the strength of higher write endurance and faster writes make FRAM superior to EEPROM in all but one-time programmable applications. The advantage is most obvious in data collection environments where writes are frequent and data must be nonvolatile.

The attributes of fast writes and high write endurance combine in many innovative ways. A short list of ideas is provided here.

1. Data collection. In applications where data is collected and saved, FRAM provides a superior alternative to other solutions. It is more cost effective than battery backup for SRAM and provides better write attributes than EEPROM.

2. Configuration. Any nonvolatile memory can retain a configuration. However if the configuration changes and power failure is a possibility, the higher write endurance of FRAM allows changes to be recorded without restriction. Any time the system state is altered, the change can be written. This avoids writing to memory on power down when the available time is short and power scarce.

3. High noise environments. Writing to EEPROM in a noisy environment can be challenging. When severe noise or power fluctuations are present, the long write time of EEPROM creates a window of vulnerability during which the write can be corrupted. The fast write of FRAM is completed within a microsecond. This time is typically too short for noise or power fluctuation to disturb it.

4. Time to market. In a complex system, multiple software routines may need to access the nonvolatile memory. In this environment the time delay associated with programming EEPROM adds undue complexity to the software development. Each software routine must wait for complete programming before allowing access to the next routine. When time to market is critical, FRAM can eliminate this simple obstacle. As soon as a write is issued to the FM24C04, it is effectively done -- no waiting.

5. RF/ID. In the area of contactless memory, FRAM provides an ideal solution. Since RF/ID memory is powered by an RF field, the long programming time and high current consumption needed to write EEPROM is unattractive. FRAM provides a superior solution. The FM24C04 is suitable for multi-chip RF/ID products.

6. Maintenance tracking. In sophisticated systems, the operating history and system state during a failure is important knowledge. Maintenance can be expedited when this information has been recorded. Due to the high write endurance, FRAM makes an ideal system log. In addition, the convenient 2-wire interface of the FM24C04 allows memory to be distributed throughout the system using minimal additional resources.

Electrical Specifications

Absolute Maximum Ratings

Description	*Ratings*
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
D.C. output current on any pin	5 mA
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability

DC Operating Conditions TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Main Power Supply	4.5	5.0	5.5	V	1
IDD	VDD Supply Current @ SCL = 100 kHz		115	150	µA	2
IDD	VDD Supply Current @ SCL = 400 kHz		400	500	µA	2
ISB	Standby Current		1	10	µA	3
ILI	Input Leakage Current			10	µA	4
ILO	Output Leakage Current			10	µA	4
VIL	Input Low Voltage	-0.3		VDD x 0.3	V	1
VIH	Input High Voltage	VDD x 0.7		VDD + 0.5	V	1
VOL	Output Low Voltage @ IOL = 3 mA			0.4	V	1
VOL	Output Low Voltage @ IOL = 6 mA			0.6	V	1,5
VHYS	Input Hysteresis	VDD x .05			V	1, 5

Notes

1. Referenced to VSS.
2. SCL toggling between VDD-0.3V and VSS, other inputs VSS or VDD-0.3V
3. SCL = SDA = VDD. All inputs VSS or VDD. Stop command issued.
4. VIN or VOUT = VSS to VDD
5. This parameter is periodically sampled and not 100% tested.

AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
fSCL	SCL Clock Frequency	0	100	0	400	kHz	
tSP	Noise Suppression Time Constant on SCL, SDA		50		50	ns	
tAA	SCL Low to SDA Data Out Valid		3		0.9	µs	
tBUF	Bus Free Before New Transmission	4.7		1.3		µs	
tHD:STA	Start Condition Hold Time	4.0		0.6		µs	
tLOW	Clock Low Period	4.7		1.3		µs	
tHIGH	Clock High Period	4.0		0.6		µs	
tSU:STA	Start Condition Setup for Repeated Start	4.7		0.6		µs	
tHD:DAT	Data In Hold	0		0		ns	
tSU:DAT	Data In Setup	250		100		ns	
tRISE	SDA and SCL Rise Time		1000	20 + 0.1 Cb	300	ns	1,2
tFALL	SDA and SCL Fall Time		300	20 + 0.1 Cb	300	ns	1,2
tSU:STO	Stop Condition Setup	4.0		0.6		µs	
tDH	Data Output Hold (from SCL @ VIL)	0		0		ns	
tOF	Output Fall Time (VIH min to VIL Max)		250	20 + 0.1 Cb	250	ns	1,2

Notes : All SCL specifications as well as start and stop conditions apply to both read and write operations.

1 This parameter is periodically sampled and not 100% tested.

2 Cb = Total capacitance of one bus line in pF.

Capacitance TA = 25° C , f=1.0 MHz, VDD = 5V

Symbol	Parameter	Max	Units	Notes
CI/O	Input/output capacitance (SDA)	8	pF	1
CIN	Input capacitance	6	pF	1

Notes

1 This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	VDD * 0.1 to VDD * 0.9
Input rise and fall times	10 ns
Input and output timing levels	VDD*0.5

Equivalent AC Load Circuit

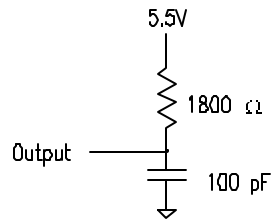
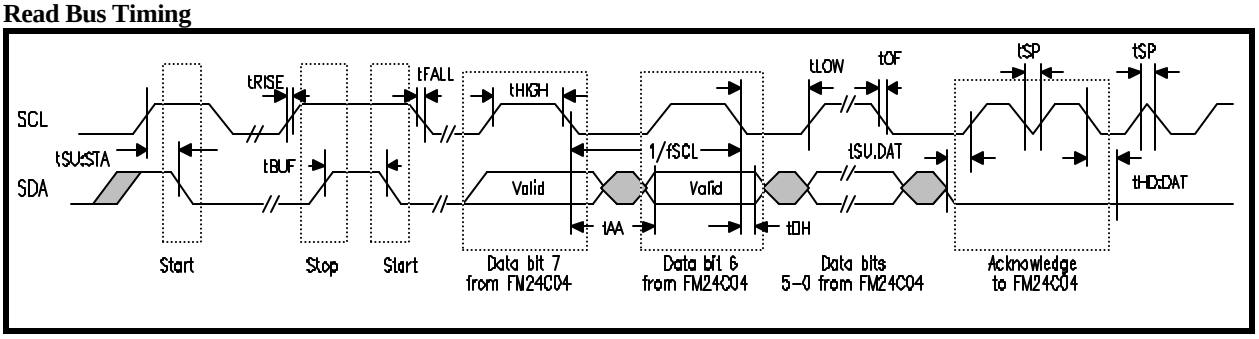


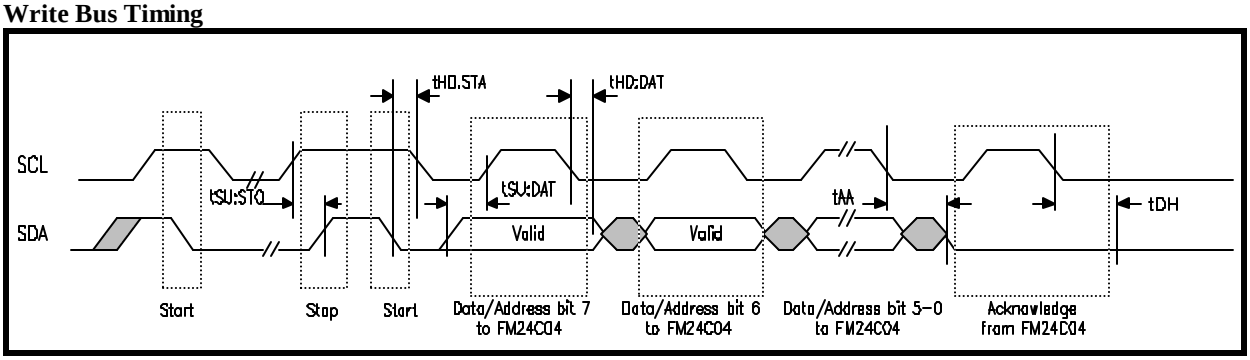
Diagram Notes

All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

Read Bus Timing



Write Bus Timing



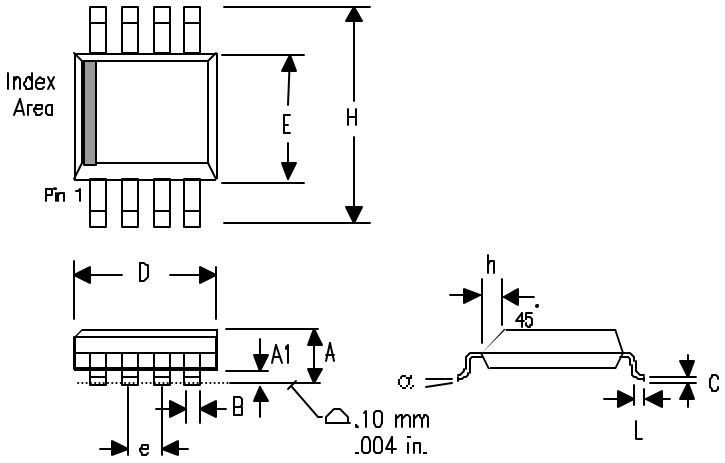
Data Retention TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Parameter	Min	Units	Notes
Data Retention	10	Years	1

Notes

1. Data retention is specified at 85° C. The relationship between retention, temperature, and the associated reliability level is characterized separately.

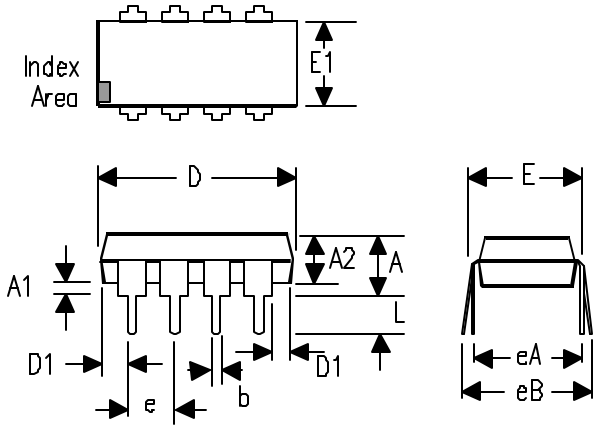
8-pin SOP (JEDEC)



Controlling dimensions is in millimeters. Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	1.35 .053		1.75 .069
A1	mm in.	.10 .004		.25 .010
B	mm in.	.33 .013		.51 .020
C	mm in.	.19 .007		.25 .010
D	mm in.	4.80 .189		5.00 .197
E	mm in.	3.80 .150		4.00 .157
e	mm in.		1.27 BSC .050 BSC	
H	mm in.	5.80 .228		6.20 .244
h	mm in.	.25 .010		.50 .197
L	mm in.	.40 .016		1.27 .050
α		0°		8°

8-pin DIP (JEDEC)



Controlling dimensions is in inches. Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in.			.210
	mm			5.33
A1	in.	0.015		
	mm	.381		
A2	in.	0.115	0.130	0.195
	mm	2.92	3.30	4.95
b	in.	0.014	0.018	0.022
	mm	.356	.457	.508
D	in.	0.355	0.365	0.400
	mm	9.02	9.27	10.2
D1	in.	0.005		
	mm	.127		
E	in.	0.300	0.310	0.325
	mm	7.62	7.87	8.26
E1	in.	0.240	0.250	0.280
	mm	6.10	6.35	7.11
e	in.		.100 BSC	
	mm		2.54 BSC	
eA	in.		.300 BSC	
	mm		7.62 BSC	
eB	in.			0.430
	mm			10.92
L	in.	0.115	0.130	0.150
	mm	2.92	3.30	3.81