Winbond Electronics Corp.

256K ´ 8 CMOS FLASH MEMORY

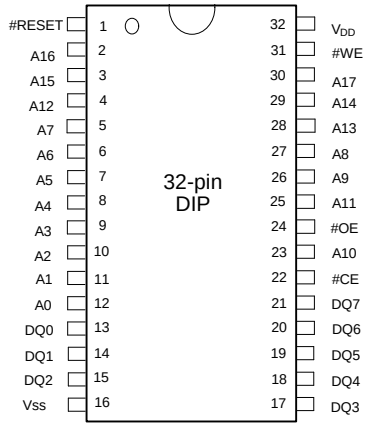
GENERAL DESCRIPTION

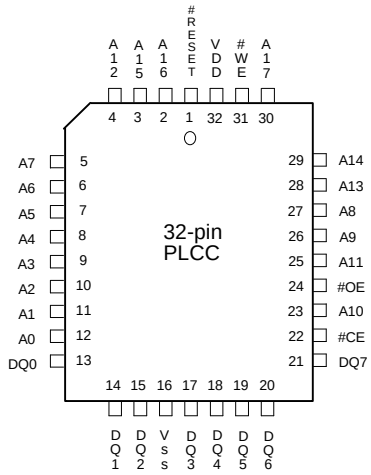
The W49F002A is a 2-megabit, 5-volt only CMOS flash memory organized as 256K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49F002A results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

FEATURES

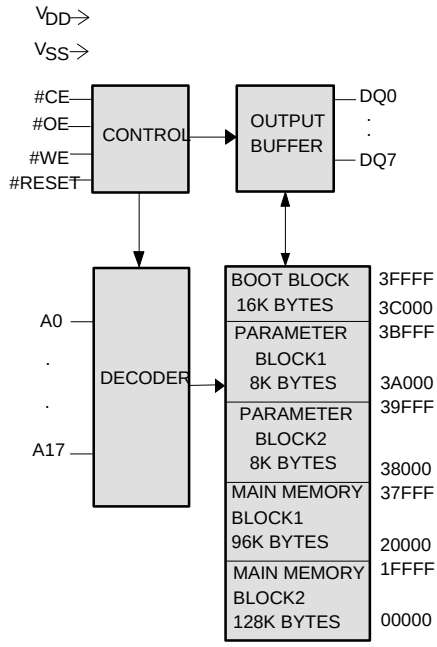
- Single 5-volt operations:
  - 5-volt Read
  - 5-volt Erase
  - 5-volt Program
- Fast program operation:
  - Byte-by-byte programming: 35 μS (typ.)
- Fast erase operation: 100 mS (typ.)
- Fast read access time: 120 nS
- Ten-year data retention
- Hardware data protection
- One 16K byte Boot Block with Lockout protection
- Typical page write (erase/program) cycles: 10 – 100
- Two 8K byte parameter blocks
- Two main memory blocks (96K, 128K) Bytes
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin DIP and PLCC

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
#RESET	Reset
A0–A17	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
VSS	Ground

FUNCTIONAL DESCRIPTION

Device Operation

Read Mode

The read operation of the W49F002A is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for details.

Write Mode

Device erase and program are accomplished via the command register. The content of the register serves as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to bring #WE to logic low state when #CE is at logic low state and #OE is at logic high state. Addresses are latched on the falling edge of #WE or #CE, whichever happens later; while data is latched on the rising edge of #WE or #CE, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Standby Mode

There are two ways to implement the standby mode on the W49F002A device, both using the #CE pin.

A CMOS standby mode is achieved with the #CE input held at V_{DD} -0.3V. Under this condition the current is typically reduced to less than 100 μA. A TTL standby mode is achieved with the #CE pin held at V_{IH}.

Under this condition the current is typically reduced to less than 3 mA.

In the standby mode the outputs are in the high impedance state, independent of the #OE input.

Output Disable Mode

With the #OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Auto-select Mode

The auto-select mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended to be used by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5V to 12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1 (see "Auto-select Codes").

The manufacturer and device codes may also be read via the command register; i.e., the W49F002A is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in "Auto-select Codes".

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (Winbond = DAh) and byte 1 (A0 = V_{IH}) the device identifier code (W49F002A = 0Bh). All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Auto-select, A1 must be V_{IL}.

Reset Mode: Hardware Reset

The #RESET pin provides a hardware method of resetting the device to reading array data. When the system drives the #RESET pin low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tri-states all data output pins, and ignores all read/write attempts for the duration of the #RESET pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the #RESET pulse. When #RESET is held at V_{IL}, the device enters the TTL standby mode; if #RESET is held at V_{SS}, the device enters the CMOS standby mode.

The #RESET pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Data Protection

The W49F002A is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from V_{DD} power-up and power-down transitions or system noise.

Low V_{DD} Write Inhibit

To avoid initiation of a write cycle during V_{DD} power-up and power-down, the W49F002A locks out write cycles for V_{DD} < 2.5V. When V_{DD} < 2.5V, all internal program/erase circuits are disabled, and the device resets to the read mode. The W49F002A ignores all writes until V_{DD} > 2.5V. The user must ensure that the control pins are in the correct logic state when V_{DD} > 2.5V to prevent unintentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 nS (typical) on #OE, #OE, or #WE will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of #OE = V_{IL}, #CE = V_{IH}, or #WE = V_{IH}. To initiate a write cycle #CE and #WE must be a logical zero while #OE is a logical one.

Power-up Write Inhibit

Power-up of the device with #WE = #CE = V_{IL} and #OE = V_{IH} will not accept commands on the rising edge of #WE. The internal state machine is automatically reset to the read mode on power-up.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences. Moreover, both Reset/Read commands are functionally equivalent, resetting the device to the read mode.

Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition.

The device will automatically returns to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Auto-select Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an auto-select command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the auto-select command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of DAh. A read cycle from address XX01H returns the device code (W49F002A = 0Bh).

Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded program algorithm. Addresses are latched on the falling edge of #CE or #WE, whichever happens later and the data is latched on the rising edge of #CE or #WE, whichever happens first. The rising edge of #CE or #WE (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags"). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Only erase operations can convert "0"s to "1"s.

Refer to the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed sequentially on each sector at the same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last #WE pulse in the command sequence and terminates when the data on DQ7 is "1" at which time the device returns to read the mode.

Refer to the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of #WE, while the command (30H) is latched on the rising edge of #WE.

Sector erase does not require the user to program the device prior to erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the rising edge of the #WE pulse for the last sector erase command pulse and terminates when the data on DQ7, Data Polling, is "1."

Refer to the Embedded Erase Algorithm using typical command strings and bus operations.

Write Operation Status

DQ7: Data Polling

The W49F002A device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a "1" at the DQ7 output.

The flowchart for Data Polling (DQ7) is shown in "Data Polling Algorithm".

For chip erase, the Data Polling is valid after the rising edge of the sixth pulse in the six #WE write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase #WE pulse.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable (#OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0 – DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see "Command Definitions").

See "#DATA Polling During Embedded Algorithm Timing Diagrams".

DQ6: Toggle Bit

The W49F002A also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (#OE toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth #WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth #WE pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase #WE pulse. The Toggle Bit is active during the sector erase time-out.

TABLE OF OPERATING MODES

Device Bus Operations

MODE	PIN					
	#CE	#OE	#WE	#RESET	A0 – A17	DQ0 – DQ7
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ain	Dout
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ain	Din
Write Inhibit	V_{IH}	X	V_{IL}	X	X	High Z/DOUT
	V_{IH}	X	X	V_{IH}	X	High Z/DOUT
Standby	V_{IH}	X	X	V_{IH}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	High Z
Reset	X	X	X	V_{IL}	X	High Z

Auto-select Codes (High Voltage Method)

DESCRIPTION	#CE	#OE	#WE	OTHER ADD	A9	A1	A0	DQ7 TO DQ0
Manufacturer ID: Winbond	V_{IL}	V_{IL}	V_{IH}	X	V_{ID}	V_{IL}	V_{IL}	DAh
Device ID: W49F002A (Top Boot Block)	V_{IL}	V_{IL}	V_{IH}	X	V_{ID}	V_{IL}	V_{IH}	0Bh

Notes:

1. SA = Sector Address, X = Don't Care. Sector Protection Verification: 01h (protected); 00h (unprotected).
2. The hardware SID read function is not included in all parts; please refer to Ordering Information for details.

Hardware Sequence Flags

OPERATION		DQ7 (Note*)	DQ6
Standard Mode	Embedded Program Algorithm	#DQ7	Toggle
	Embedded Erase Algorithm	0	Toggle

Note*: DQ7 require a valid address when reading status information. Refer to the appropriate subsection for further details.

Command Defination[1]

COMMAND DESCRIPTION	No. of Cycles	1th Cycle Addr. Data	2nd Cycle Addr. Data	3rd Cycle Addr. Data	4th Cycle Addr. Data	5th Cycle Addr. Data	6th Cycle Addr. Data
Read	1	AIN DOUT					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Sector Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA[3] 30
Byte Program	4	5555 AA	2AAA 55	5555 A0	AIN DIN		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit [2]	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit [2]	1	XXXX F0					

Notes:

1. Address Format: A14 – A0 (Hex); Data Format: DQ7 – DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. SA means: Sector Address

   If SA is within 3C000 to 3FFFF (Boot Block address range), and the Boot Block programming lockout feature is activated, nothing will happen and the device will go back to read mode after 100 nS.

   If the Boot Block programming lockout feature is not activated, this command will erase Boot Block.

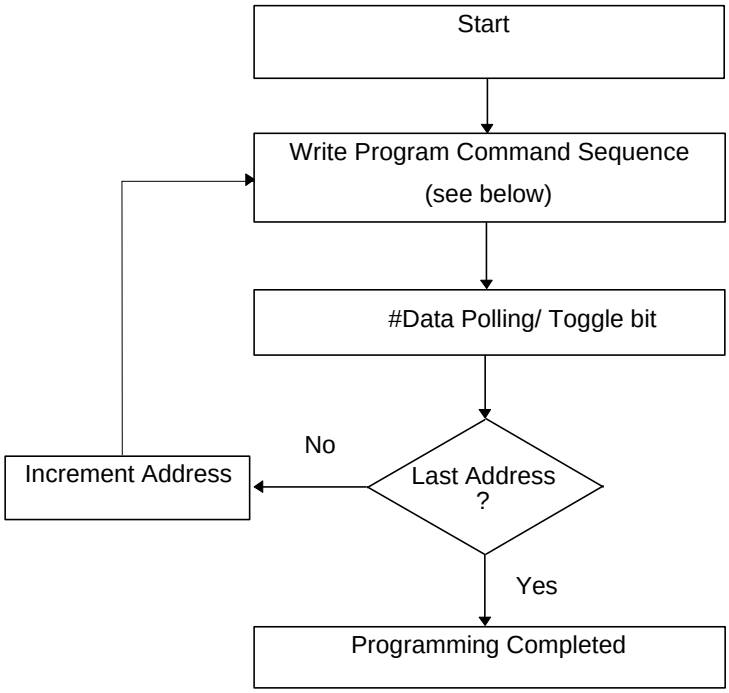
   If SA is within 3A000 to 3BFFF (Parameter Block1 address range), this command will erase PB1.

   If SA is within 38000 to 39FFF (Parameter Block2 address range), this command will erase PB2.

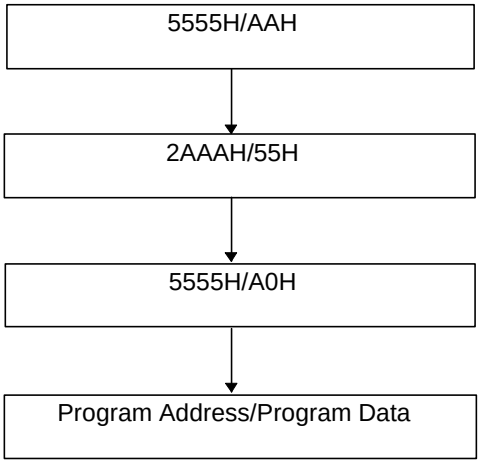
   If SA is within 20000 to 37FFF (Main Memory Block1 address range), this command will erase MMB1.

   If SA is within 00000 to 1FFFF (Main Memory Block2 address range), this command will erase MMB2.

EMBEDDED ALGORITHMS

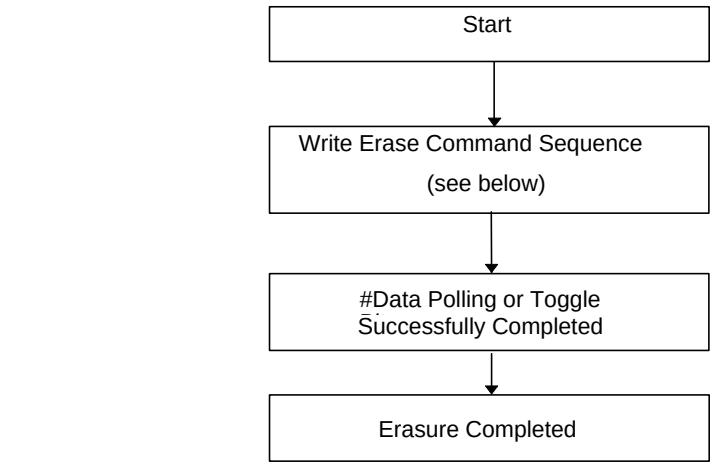


Program Command Sequence (Address/Command):

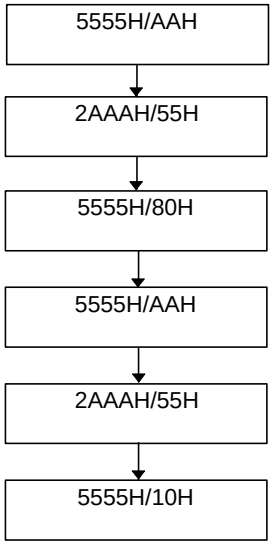


Embedded Programming Algorithm

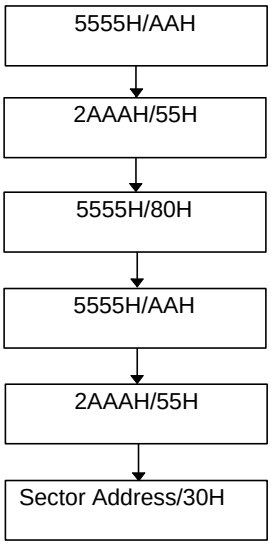
Embedded Algorithms, continued



Chip Erase Command Sequence (Address/Command):

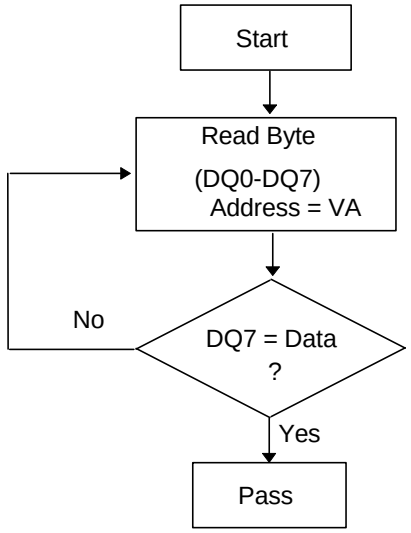


Individual Sector Erase Command Sequence (Address/Command):



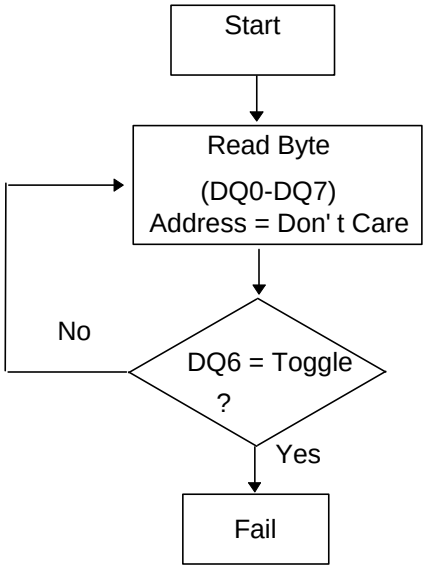
Embedded Erase Algorithm

Embedded Algorithms, continued



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= Valid address equals any sector group address during chip erase

#Data Polling Algorithm



Toggle Bit Algorithm

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	#CE = #OE = V_{IL}, #WE = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	25	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	#CE = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	#CE = V_{DD} -0.3V, all DQs open Other inputs = V_{DD} -0.3V/ V_{SS}	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	µS
Power-up to Write Operation	TPU. WRITE	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

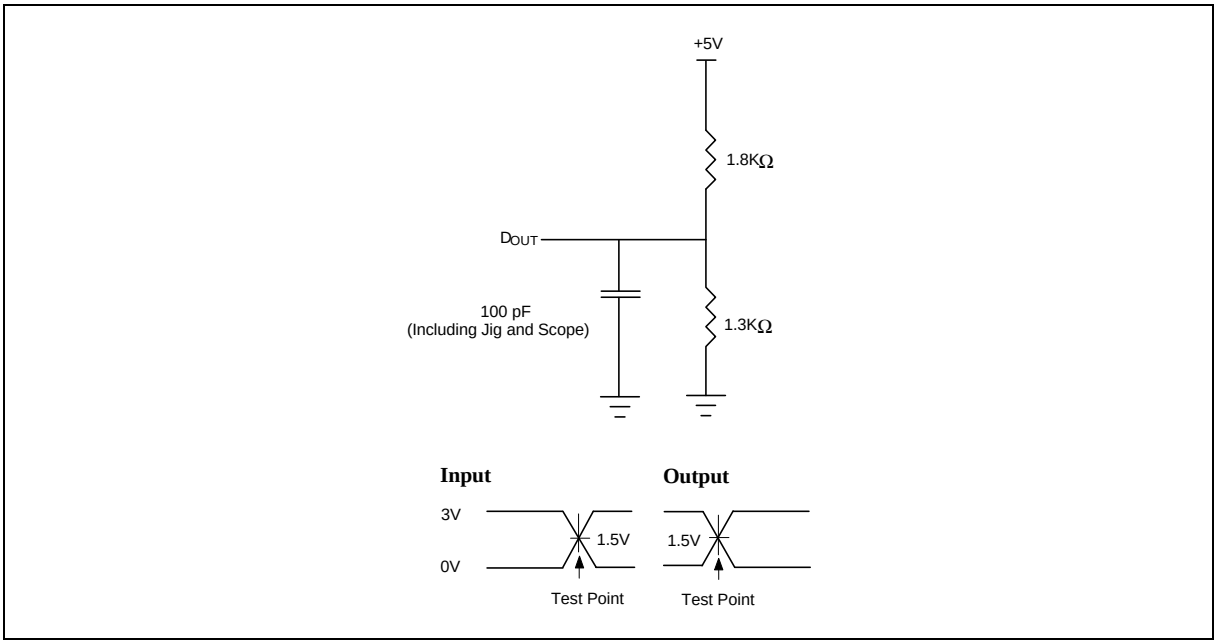
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V / 1.5V
Output Load	1 TTL Gate and C_L = 100 pF

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10%, V_{DD} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	T_{RC}	120	-	nS
Chip Enable Access Time	T_{CE}	-	120	nS
Address Access Time	T_{AA}	-	120	nS
Output Enable Access Time	T_{OE}	-	50	nS
#CE Low to Active Output	T_{CLZ}	0	-	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#CE High to High-Z Output	T_{CHZ}	-	30	nS
#OE High to High-Z Output	T_{OHZ}	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
#WE and #CE Setup Time	T_{CS}	0	-	-	nS
#WE and #CE Hold Time	T_{CH}	0	-	-	nS
#OE High Setup Time	T_{OES}	0	-	-	nS
#OE High Hold Time	T_{OEH}	0	-	-	nS
#CE Pulse Width	T_{CP}	100	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Byte Programming Time	T_{BP}	-	35	50	µS
Erase Cycle Time	T_{EC}	-	0.1	0.2	S

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

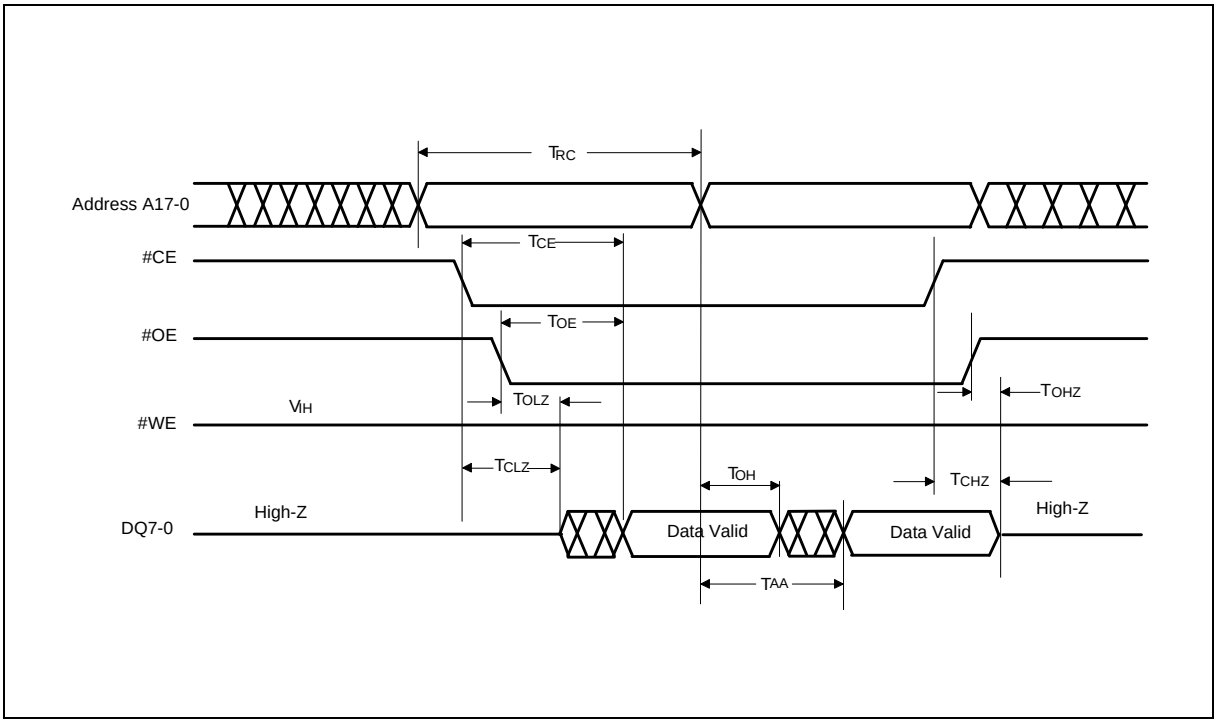
AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
#OE to Data Polling Output Delay	T_{OEP}	-	50	nS
#CE to Data Polling Output Delay	T_{CEP}	-	120	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	50	nS
#CE to Toggle Bit Output Delay	T_{CET}	-	120	nS

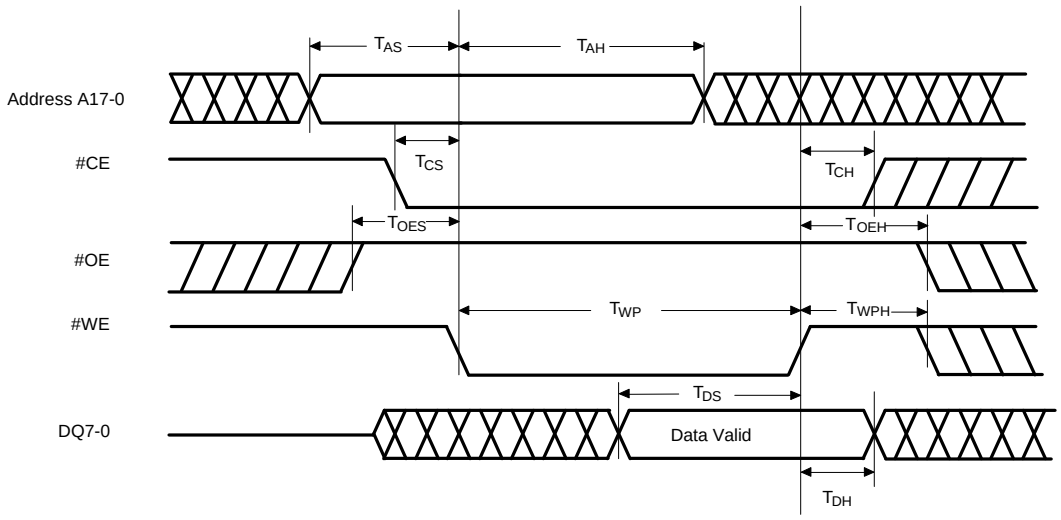
TIMING WAVEFORMS

Read Cycle Timing Diagram

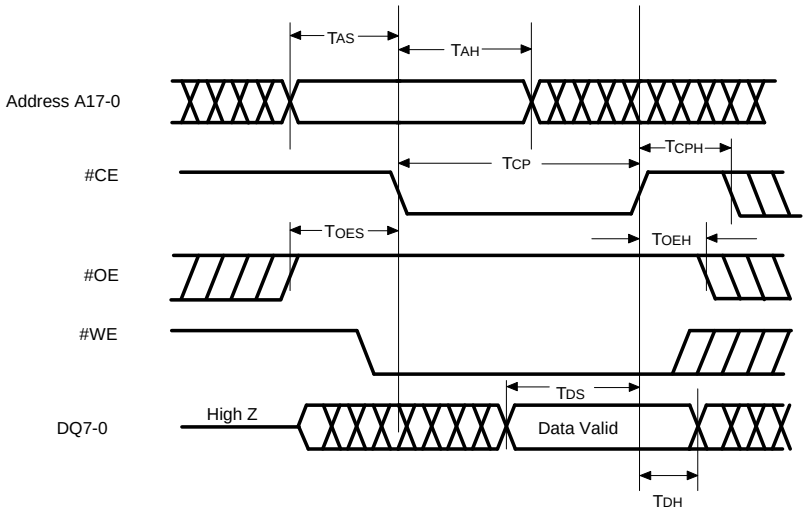


Timing Waveforms, continued

#WE Controlled Command Write Cycle Timing Diagram

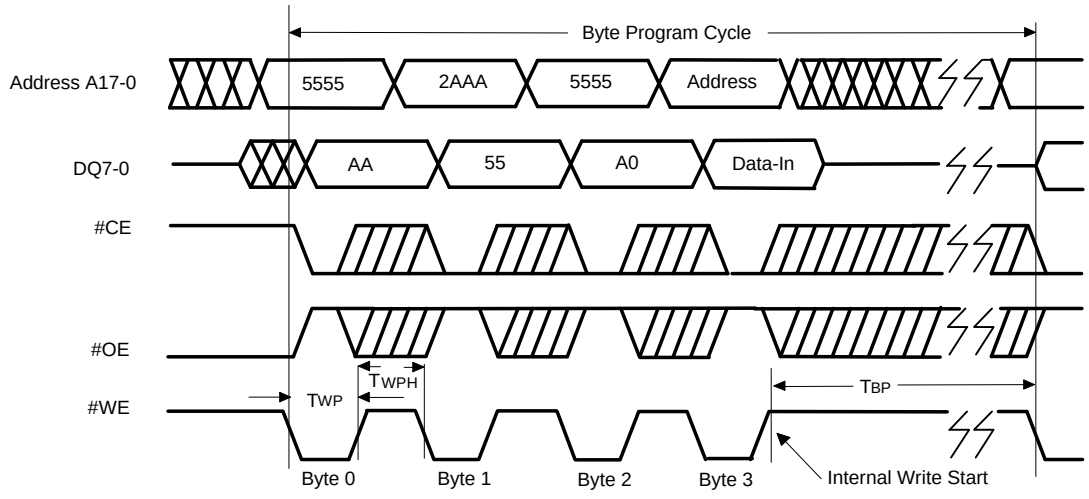


#CE Controlled Command Write Cycle Timing Diagram

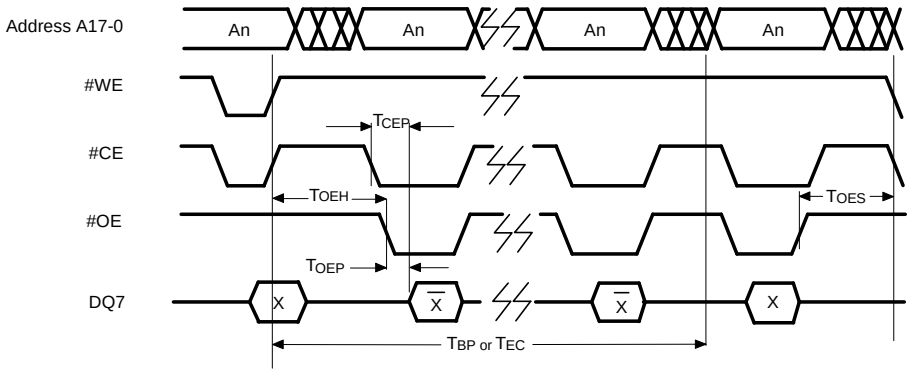


Timing Waveforms, continued

Program Cycle Timing Diagram

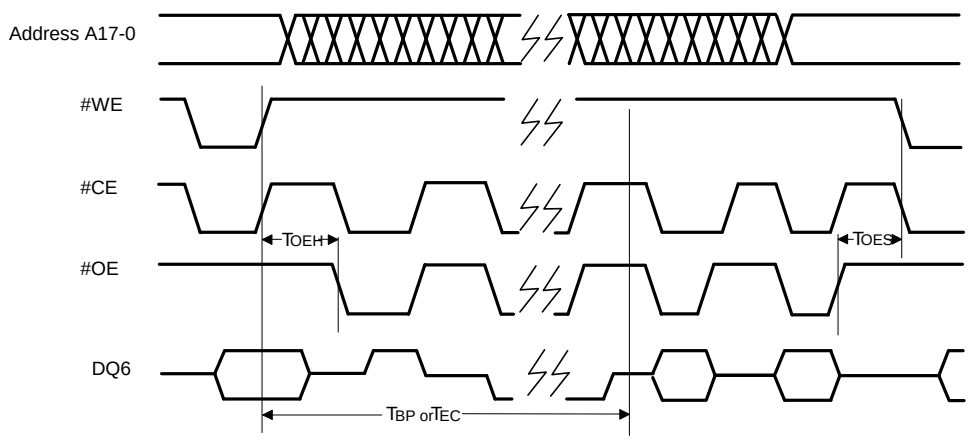


#DATA Polling Timing Diagram

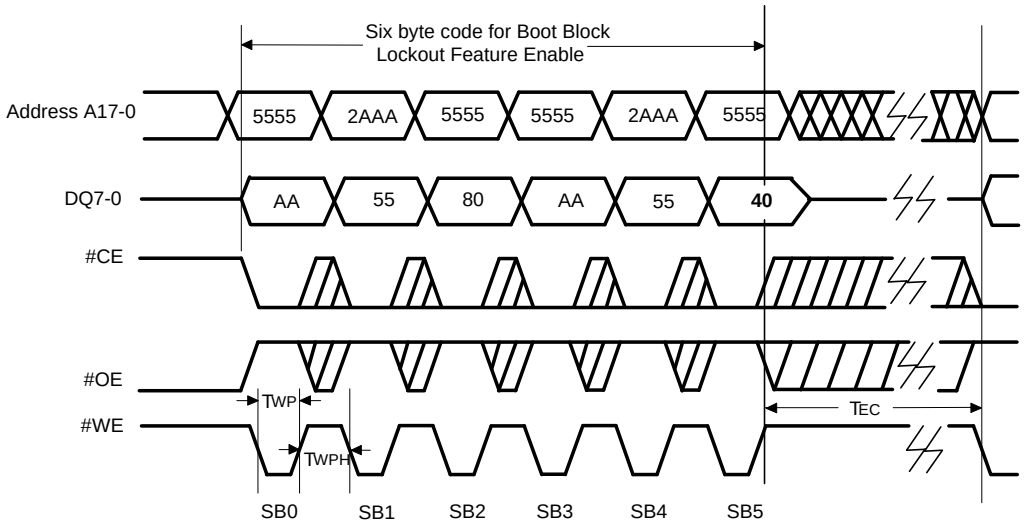


Timing Waveforms, continued

Toggle Bit Timing Diagram

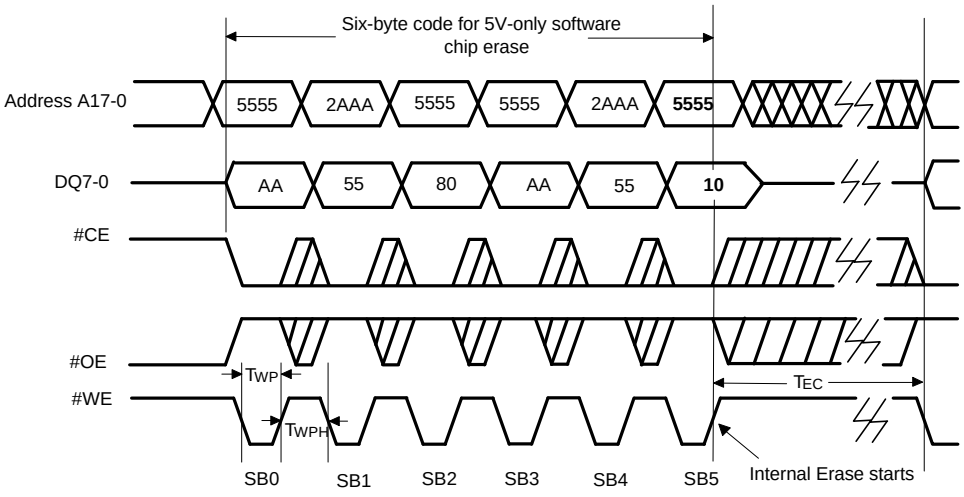


Boot Block Lockout Enable Timing Diagram

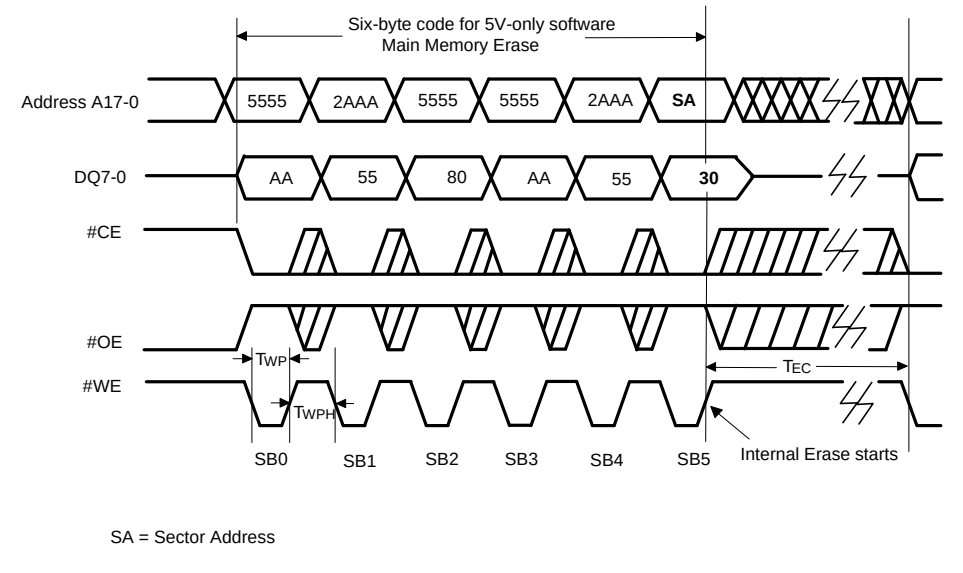


Timing Waveforms, continued

Chip Erase Timing Diagram



Sector Erase Timing Diagram



SA = Sector Address

ORDERING INFORMATION

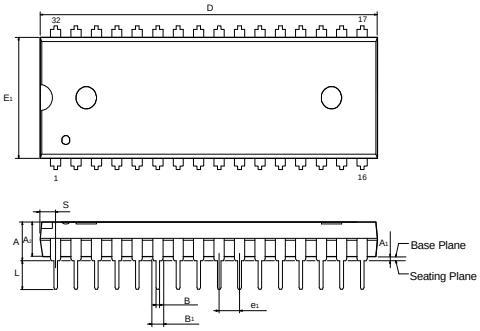
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (μA)	CYCLING	PACKAGE
W49F002A-12	120	50	100 (CMOS)	10 – 100	32-pin DIP
W49F002AP-12	120	50	100 (CMOS)	10 – 100	32-pin PLCC

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. Winbond offers Top Boot Block device, if any of Bottom Boot Block devices is required, please contact Winbond FAEs.

PACKAGE DIMENSIONS

32-pin P-DIP

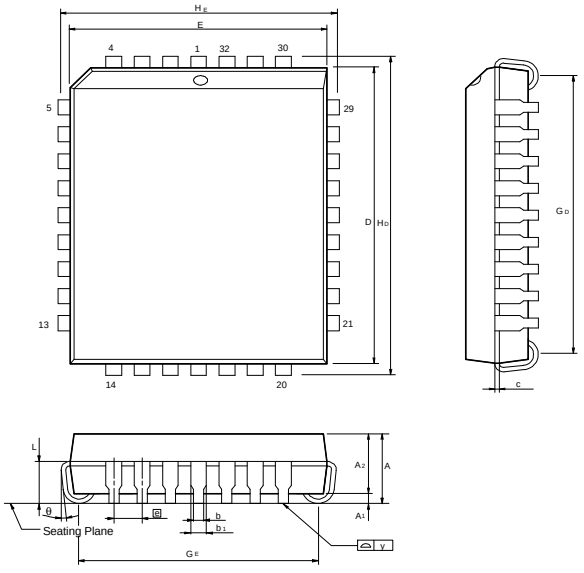


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

32-pin PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.51	0.530	12.45	12.9	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.49	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0 °	—	10 °	0 °	—	10 °

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Sep. 12, 2001	-	Initial Issued

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