

HD6321/HD6821

PIA (Peripheral Interface Adapter)

The HD6321/HD6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the HD6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

FEATURES

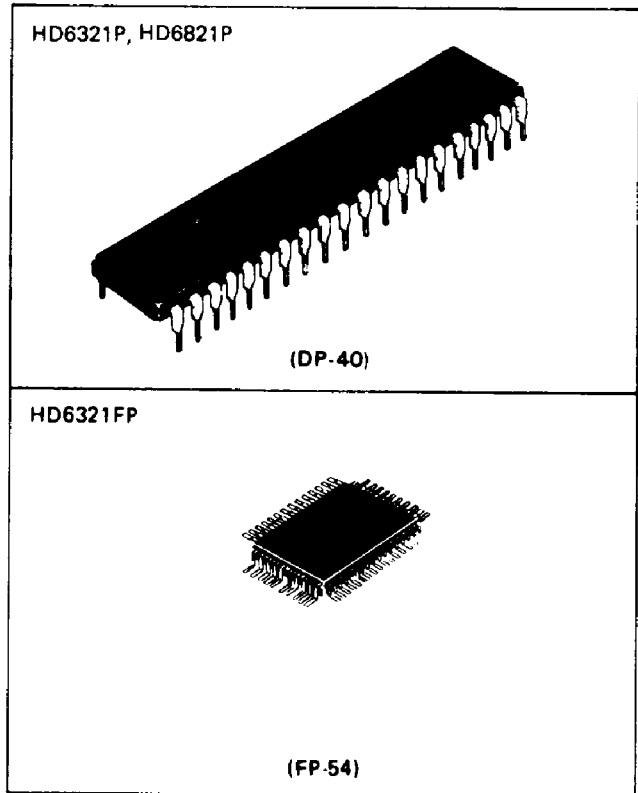
- Two Bi-directional 8-bit Peripheral Data Bus for interface to Peripheral devices
- Two programmable control, Data Direction Registers
- Four Individually Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
 - CA₁, CA₂ Port A (PA₀ ~ PA₇)
 - CA₂, CB₂ Port B (PB₀ ~ PB₇)
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers

—HD6321—

- Low-Power, High-Speed, High-Density CMOS
- Wide Range Operating Voltage (V_{cc} = 5V ± 10%)
- Compatible with NMOS PIA (HD6821) (Refer to Electrical Specification as to Minor difference)

—HD6821—

- Compatible with MC6821, MC68A21 and MC68B21



The specifications of the HD6321 are for preliminary and may change hereafter. Please make an inquire at sales office upon adoption of the HD6321.

■ TYPE OF PRODUCTS

Type No.	Process	Clock Frequency	Package
HD6321P	CMOS	1.0 MHz	DP-40
HD63A21P		1.5 MHz	
HD63B21P		2.0 MHz	
HD6321FP	CMOS	1.0 MHz	FP-54
HD63A21FP		1.5 MHz	
HD63B21FP		2.0 MHz	
HD6821P	NMOS	1.0 MHz	DP-40
HD68A21P		1.5 MHz	
HD68B21P		2.0 MHz	
HD6821	NMOS	1.0 MHz	DC-40
HD68A21		1.5 MHz	
HD68B21		2.0 MHz	



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value		Unit
		HD6321	HD6821	
Supply Voltage	V_{cc}^*	-0.3 ~ +7.0	-0.3 ~ +7.0	V
Input Voltage	V_{in}^*	-0.3 ~ +7.0	-0.3 ~ +7.0	V
Maximum Output Current	$ I_O ^{**}$	10	-	mA
Maximum Total Output Current	$ \Sigma I_O ^{***}$	100	-	mA
Operating Temperature	T_{opr}	-20 ~ +75	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +150	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

** Maximum output current is the maximum current which can flow in or flow out from one output terminal and I/O common terminal, (PA₀~PA₇, CA₂, PB₀~PB₇, CB₂, D₀~D₇)

*** Maximum total output current is the total sum of output current which can flow in or flow out simultaneously from output terminals and I/O common terminals. (PA₀~PA₇, CA₂, PB₀~PB₇, CB₂, D₀~D₇)

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	HD6321			HD6821			Unit
		min.	typ	max.	min.	typ	max.	
Supply Voltage	V_{cc}^*	4.5	5.0	5.5	4.75	5.0	5.25	V
Input "Low" Voltage	V_{IL}^*	0	-	0.8	-0.3	-	0.8	V
Input "High" voltage	V_{IH}^* D ₀ ~D ₇ , PA ₀ ~PA ₇ , CA ₁ , CA ₂ , PB ₀ ~PB ₇ , CB ₁ , CB ₂ , E, R/W, CS ₀ , CS ₂ , CS ₁ , RS ₀ , RS ₁ , RES	2.2	-	V_{cc}	2.0	-	V_{cc}	V
		3.0**	-	V_{cc}				
Operating Temperature	T_{opr}	-20	25	75	-20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

** Characteristics will be improved.

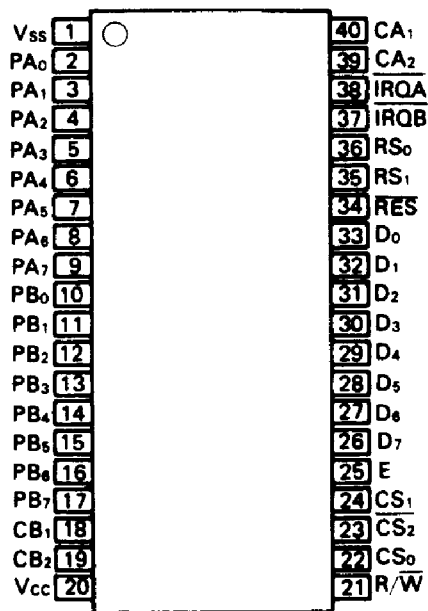


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HD6321/HD6821

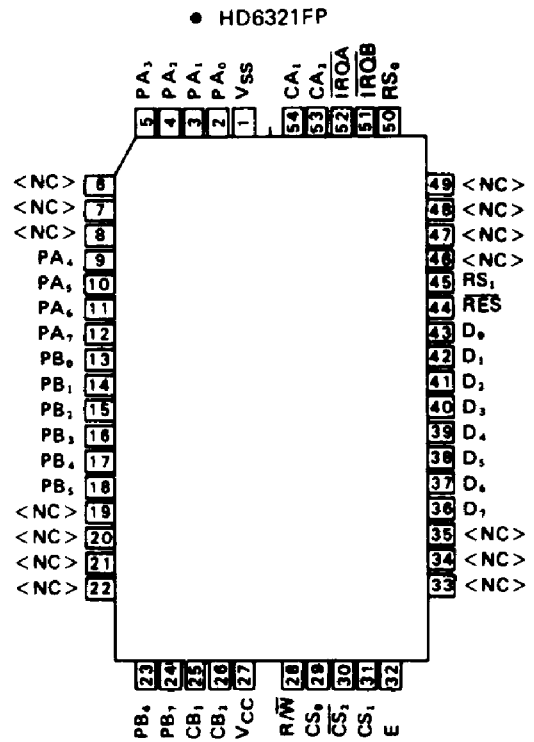
■ PIN ARRANGEMENT

- HD6321P, HD6821P



(Top View)

(DP-40, DC-40)

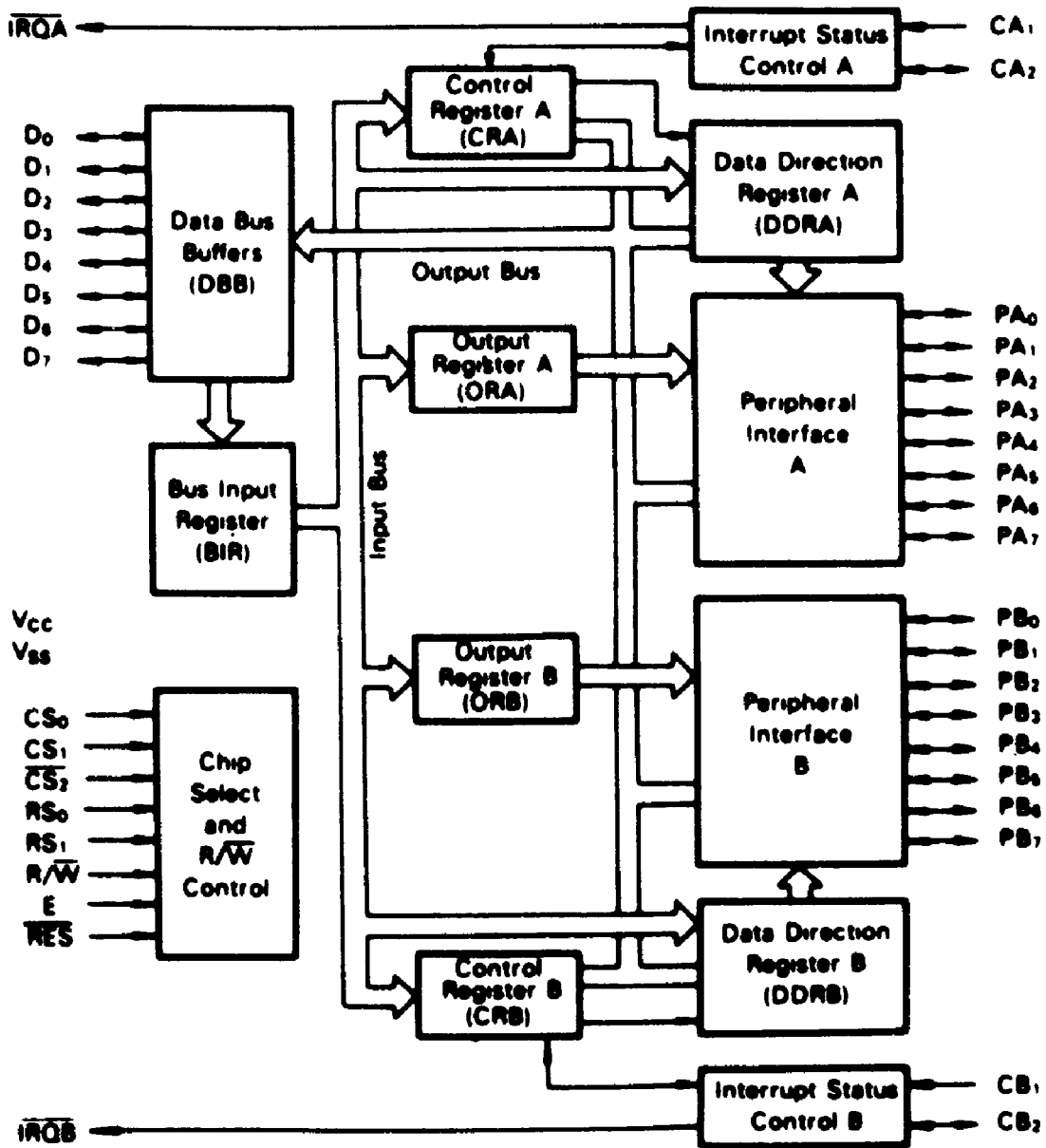


(Top View)

(FP-54)



■ BLOCK DIAGRAM



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663

HD6321/HD6821

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (HD6321; $V_{CC} = 5V \pm 10\%$, HD6821; $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$, unless otherwise noted.)

Item	Symbol	HD6321			HD6821			Unit					
		Test Condition	min.	typ*	max	Test Condition	min		typ*	max			
Input "High" Voltage	V_{IH}	$D_0 \sim D_7, PA_0 \sim PA_7, CA_1, CA_2, PB_0 \sim PB_7, CB_1, CB_2$		2.2	—	V_{CC}		2.0	—	V_{CC}	V		
		$E, R/\overline{W}, CS_0, \overline{CS}_2, CS_1, RS_0, RS_1, \overline{RES}$			—								
Input "Low" Voltage	V_{IL}	All Inputs		-0.3	—	0.8		-0.3	—	0.8	V		
Input Leakage Current	I_{in}	$R/\overline{W}, \overline{RES}, RS_0, RS_1, CS_0, CS_1, \overline{CS}_2, CA_1, CB_1, E$	$V_{in} = 0 \sim V_{CC}$	-2.5	—	2.5	$V_{in} = 0 \sim V_{CC}$	-2.5	—	2.5	μA		
Three State (Off State) Input Current	ITSI	$PA_0 \sim PA_7, CA_2$	$V_{in} = 0.4 \sim V_{CC}$	-10	—	10	$V_{in} = 0.4 \sim 2.4V$	-10	—	10	μA		
		$D_0 \sim D_7, PB_0 \sim PB_7, CB_2$											
Input "High" Current	I_{IH}	$PA_0 \sim PA_7, CA_2$		/			$V_{IH} = 2.4V$	-200	—	—	μA		
Input "Low" Current	I_{IL}	$PA_0 \sim PA_7, CA_2$		/			$V_{IL} = 0.4V$	—	—	-2.4	mA		
Output "High" Voltage	V_{OH}	$D_0 \sim D_7$		$I_{OH} = -400\mu A$	4.1	—	—	$I_{OH} = -205\mu A$	2.4	—	—	V	
				$I_{OH} \leq -10\mu A$	$V_{CC} - 0.1$	—	—						
		$PA_0 \sim PA_7, CA_2, PB_0 \sim PB_7, CB_2$		$I_{OH} = -400\mu A$	4.1	—	—						
				$I_{OH} < -10\mu A$	$V_{CC} - 0.1$	—	—						
$PA_0 \sim PA_7, CA_2, PB_0 \sim PB_7, CB_2$							$I_{OH} = -200\mu A$	2.4***	—	—			
							$I_{OH} = -10\mu A$	$V_{CC} - 0.1$	—	—			
							$I_{OH} = -200\mu A$	2.4	—	—			
Output "Low" Voltage	V_{OL}	$D_0 \sim D_7, \overline{IRQA}, \overline{IROB}$		$I_{OL} = 1.6mA$	—	—	0.4	$I_{OL} = 1.6mA$	—	—	0.4	V	
				$I_{OL} = 3.2mA$	—	—	0.6						
		$PA_0 \sim PA_7, CA_2, PB_0 \sim PB_7, CB_2$											
Output "High" Current	I_{OH}	$D_0 \sim D_7, PA_0 \sim PA_7, CA_2, PB_0 \sim PB_7, CB_2$						$V_{OH} = 2.4V$	-205	—	—	μA	
								$V_{OH} = 2.4V^{**}$	-200	—	—	μA	
								$V_{OH} = 1.5V$	-1.0	—	-10	mA	
Output Leakage Current (Off State)	I_{LOH}	$\overline{IRQA}, \overline{IROB}$	$V_{OH} = V_{CC}$	—	—	10	$V_{OH} = 2.4V$	—	—	10	μA		
Input Capacitance	C_{in}	$PA_0 \sim PA_7, PB_0 \sim PB_7, CA_2, CB_2, D_0 \sim D_7$	$V_{in} = 0V$ $T_a = 25^\circ C$ $f = 1.0MHz$	—	—	12.5	$V_{in} = 0V$ $T_a = 25^\circ C$ $f = 1.0MHz$	—	—	12.5	pF		
		$R/\overline{W}, \overline{RES}, RS_0, RS_1, CS_0, CS_1, \overline{CS}_2, CA_1, CB_1, E$		—	—	10		—	—	10			
Output Capacitance	C_{out}	$\overline{IRQA}, \overline{IROB}$	$V_{in} = 0V$ $T_a = 25^\circ C$ $f = 1.0MHz$	—	—	10	$V_{in} = 0V$ $T_a = 25^\circ C$ $f = 1.0MHz$	—	—	10	pF		
Supply Current ****	I_{CC}	<ul style="list-style-type: none"> • $PA_0 \sim PA_7, CA_2, PB_0 \sim PB_7, CB_2$ are specified as input. • Chip is not selected. • Input level $V_{IH} \text{ min} = V_{CC} - 0.8V$ $V_{IL} \text{ max} = 0.8V$ • $PA_0 \sim PA_7, CA_2$ and $PB_0 \sim PB_7, CB_2$ are specified as input. • Under Data Bus R/\overline{W} operation. 		$E = 1.0MHz$	—	—	300	/			μA		
				$E = 1.5MHz$	—	—	400						
				$E = 2.0MHz$	—	—	500						
				$E = 1.0MHz$	—	—	4				mA		
				$E = 1.5MHz$	—	—	5						
				$E = 2.0MHz$	—	—	6						
Power Dissipation	P_D			/				—	260	550	mW		

* $T_a = 25^\circ C, V_{CC} = 5.0V$

*** HD6821; $V_{OH} = 2.2V \text{ min} (PA_0 \sim PA_7, CA_2)$

**** Supply current is defined on the condition that there is no current flow from output terminals. Supply current will be increased when the current from output terminal exists. Also the current will be increased for charging and discharging the capacitive load. Please take this case into consideration in estimating system power.



• AC CHARACTERISTICS (HD6321; $V_{CC} = 5V \pm 10\%$, HD6821; $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$ unless otherwise noted)

1. PERIPHERAL TIMING

Item	Symbol	Test Condition	HD6321		HD63A21		HD63B21		HD6821		HD68A21		HD68B21		Unit			
			min	max	min	max	min	max	min	max	min	max	min	max				
Peripheral Data Setup Time	t_{PDSU}	Fig. 1	100	—	100	—	100	—	200	—	135	—	100	—	ns			
Peripheral Data Hold Time	t_{PDH}	Fig. 1	0	—	0	—	0	—	0	—	0	—	0	—	ns			
Delay Time, Enable negative Transition to CA ₂ negative transition	Enable → CA ₂ Negative	t_{CA2}	Fig. 2, Fig. 3	—	200	—	200	—	200	—	1000	—	670	—	500	ns		
Delay Time, Enable negative transition to CA ₂ positive transition	Enable → CA ₂ Positive	t_{RS1}	Fig. 2	—	200	—	200	—	200	—	1000	—	670	—	500	ns		
Rise and Fall Times for CA ₁ and CA ₂ input signals	CA ₁ , CA ₂	t_r, t_f	Fig. 3	—	100	—	100	—	100	—	1000	—	1000	—	1000	ns		
Delay Time from CA ₁ active transition to CA ₂ positive transition	CA ₁ → CA ₂	t_{RS2}	Fig. 3	—	300	—	300	—	300	—	2000	—	1350	—	1000	ns		
Delay Time, Enable negative transition to Peripheral Data Valid	Enable → Peripheral Data	t_{PDW}	Fig. 4, Fig. 5	—	300	—	300	—	300	—	1000	—	670	—	500	ns		
Delay Time, Enable negative transition to Peripheral CMOS Data Valid	Enable → Peripheral Data PA ₀ ~ PA ₇ , CA ₂	t_{CMOS}	$V_{CC} - 30\% V_{CC}$ Fig. 4	/								—	2000	—	1350	—	1000	ns
Delay Time, Enable positive transition to CB ₂ negative position	Enable → CB ₂	t_{CB2}	Fig. 6, Fig. 7	—	200	—	200	—	200	—	1000	—	670	—	500	ns		
Delay Time, Peripheral Data Valid to CB ₂ negative transition	Peripheral Data → CB ₂	t_{DC}	Fig. 5	20	—	20	—	20	—	20	—	20	—	20	—	ns		
Delay Time, Enable positive transition to CB ₂ positive transition	Enable → CB ₂	t_{RS1}	Fig. 6	—	200	—	200	—	200	—	1000	—	670	—	500	ns		
Peripheral Control Output Pulse Width, CA ₂ /CB ₂	CA ₂ , CB ₂	PW_{CT}	Fig. 2, Fig. 6	550	—	375	—	250	—	550	—	550	—	500	—	ns		
Rise and Fall Time for CB ₁ and CB ₂ input signals	CB ₁ , CB ₂	t_r, t_f	Fig. 7	—	100	—	100	—	100	—	1000	—	1000	—	1000	ns		
Delay Time, CB ₁ active transition to CB ₂ positive transition	CB ₁ → CB ₂	t_{RS2}	Fig. 7	—	300	—	300	—	300	—	2000	—	1350	—	1000	ns		
Interrupt Release Time, \overline{IROA} , \overline{IROB}	\overline{IROA} , \overline{IROB}	t_{IR}	Fig. 9	—	800	—	800	—	800	—	1800	—	1100	—	850	ns		
Interrupt Response Time	\overline{IROA} , \overline{IROB}	t_{RS3}	Fig. 8	—	400	—	400	—	400	—	1000	—	1000	—	1000	ns		
Interrupt Input Pulse Width	CA ₁ , CA ₂ , CB ₁ , CB ₂	PWI	Fig. 8	1E cycle	—	1E cycle	—	1E cycle	—	500**	—	500**	—	500**	—	ns		
Reset "Low" Time	RES*	t_{RL}	Fig. 10	200	—	200	—	200	—	1000	—	680	—	500	—	ns		

* The Reset line must be "High" a minimum of 1.0μs before addressing the PIA.

** At least one Enable "High" pulse should be included in this period.



HD6321/HD6821

2. BUS TIMING

1) READ

Item	Symbol	Test Condition	HD6321		HD63A21		HD63B21		HD6821		HD68A21		HD68B21		Unit
			min	max	min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 11	1000	—	666	—	500	—	1000	—	666	—	500	—	ns
Enable Pulse Width, "High"	PW_{EH}	Fig. 11	450	—	280	—	220	—	450	—	280	—	220	—	ns
Enable Pulse Width, "Low"	PW_{EL}	Fig. 11	430	—	280	—	210	—	430	—	280	—	210	—	ns
Enable Pulse Rise and Fall Times	t_{Er}, t_{Ef}	Fig. 11	—	25	—	25	—	20	—	25	—	25	—	25	ns
Setup Time	Address, R/W-Enable	t_{AS}	80	—	60	—	40	—	140	—	140	—	70	—	ns
Address Hold Time		t_{AH}	10	—	10	—	10	—	10	—	10	—	10	—	ns
Data Delay Time		t_{DDR}	—	290	—	180	—	150	—	320	—	220	—	180	ns
Data Hold Time		t_{DHR}	20	100	20	100	20	100	10	—	10	—	10	—	ns

2) WRITE

Item	Symbol	Test Condition	HD6321		HD63A21		HD63B21		HD6821		HD68A21		HD68B21		Unit
			min	max	min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 11	1000	—	666	—	500	—	1000	—	666	—	500	—	ns
Enable Pulse Width, "High"	PW_{EH}	Fig. 11	450	—	280	—	220	—	450	—	280	—	220	—	ns
Enable Pulse Width, "Low"	PW_{EL}	Fig. 11	430	—	280	—	210	—	430	—	280	—	210	—	ns
Enable Pulse Rise and Fall Times	t_{Er}, t_{Ef}	Fig. 11	—	25	—	25	—	20	—	25	—	25	—	25	ns
Setup Time		t_{AS}	80	—	60	—	40	—	140	—	140	—	70	—	ns
Address Hold Time	Address, R/W-Enable	t_{AH}	10	—	10	—	10	—	10	—	10	—	10	—	ns
Data Setup Time		t_{DSW}	165	—	80	—	60	—	195	—	80	—	60	—	ns
Data Hold Time		t_{DHW}	10	—	10	—	10	—	10	—	10	—	10	—	ns



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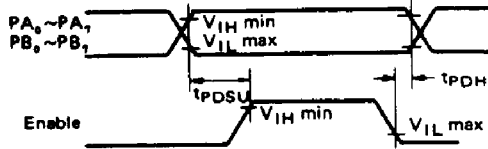


Figure 1 Peripheral Data Setup and Hold Times (Read Mode)

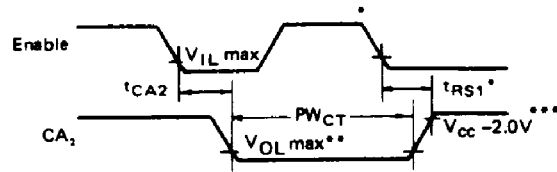


Figure 2 CA₂ Delay Time (Read Mode; CRA5=CRA3=1, CRA4=0)

* Assumes part was deselected during the previous E pulse.

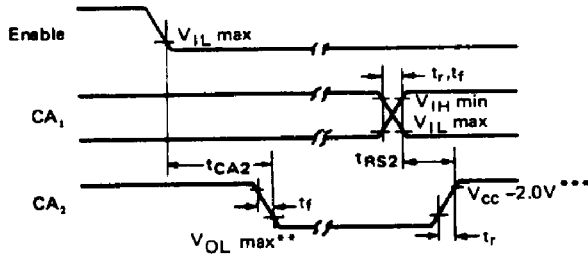


Figure 3 CA₂ Delay Time (Read Mode; CRA5=1, CRA3=CRA4=0)

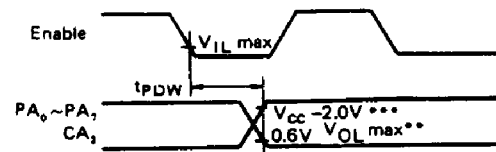


Figure 4 Peripheral Data Delay Times (Write Mode; CRA5=CRA3=1, CRA4=0)

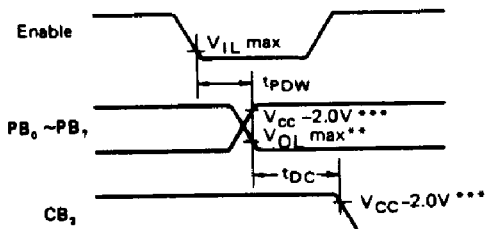


Figure 5 Peripheral Data and CB₂ Delay Times (Write Mode; CRB5=CRB3=1, CRB4=0)

(Note) CB₂ goes "Low" as a result of the positive transition of Enable.

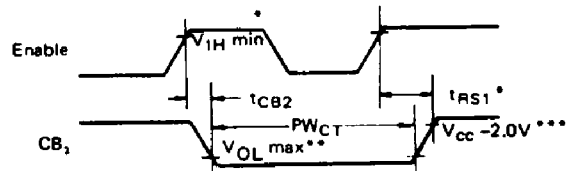


Figure 6 CB₂ Delay Time (Write Mode; CRB5=CRB3=1, CRB4=0)

* Assumes part was deselected during the previous E pulse.

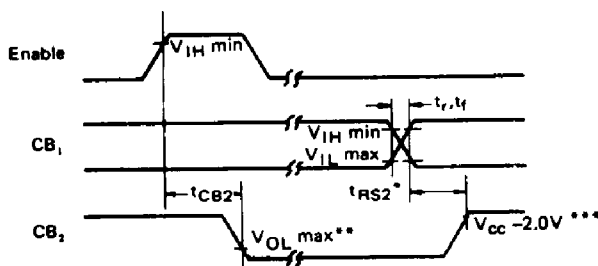


Figure 7 CB₂ Delay Time (Write Mode; CRB5=1, CRB3=CRB4=0)

** 0.6V for HD6321, 0.4V for HD6821
*** 2.4V for HD6821

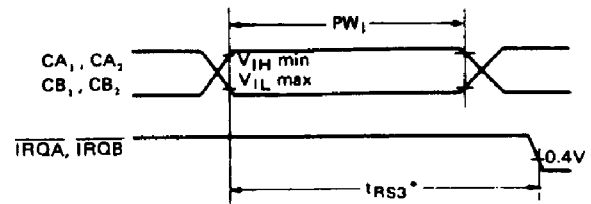


Figure 8 Interrupt Pulse Width and \overline{IRQ} Response

* Assumes Interrupt Enable Bits are set.



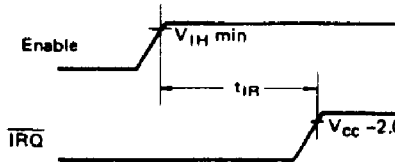


Figure 9 $\overline{\text{IRQ}}$ Release Time

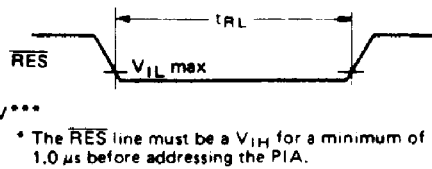


Figure 10 $\overline{\text{RES}}$ Low Time

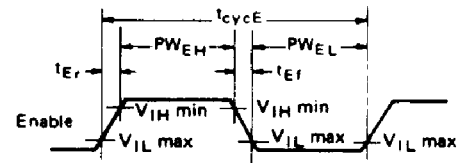


Figure 11 Enable Signal Characteristics

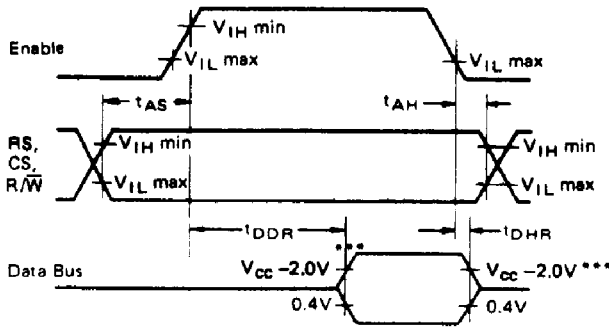


Figure 12 Bus Read Timing Characteristics (Read Information from PIA)

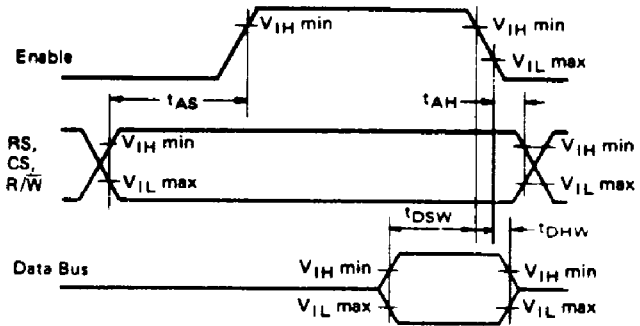
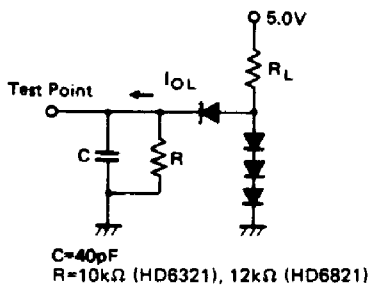


Figure 13 Bus Write Timing Characteristics (Write Information into PIA)

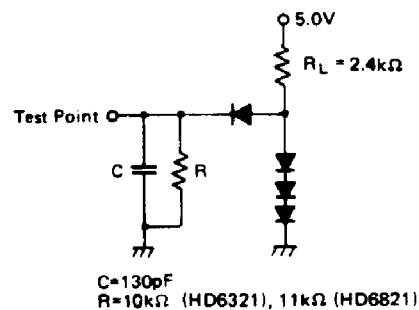
** 0.6V for HD6321, 0.4V for HD6821.
 *** 2.4V for HD6821.

LOAD A
 ($\text{PA}_0 \sim \text{PA}_7, \text{PB}_0 \sim \text{PB}_7, \text{CA}_2, \text{CB}_2$)

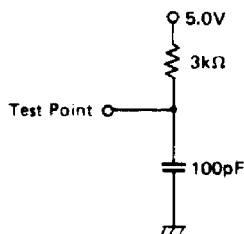


All diodes are 1S2074 or equivalent.
 Adjust R_L so that $I_{OL} = 1.8\text{mA}$, then test V_{OL}
 Adjust R_L so that $I_{OL} = 3.2\text{mA}$, then test V_{OL}

LOAD B
 ($\text{D}_0 \sim \text{D}_7$)



LOAD C
 ($\overline{\text{TRQ}}$ Only)



LOAD D (HD6821)

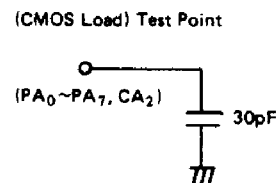


Figure 14 Bus Timing Test Loads



PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the HD6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the HD6800 VMA output, permit the MPU to have complete control over the PIA. VMA should be utilized in conjunction with an MPU address line into a chip select of the PIA.

- Bi-Directional Data ($D_0 \sim D_7$)

Input	Pin No. 33 ~ 26 (DP-40) Pin No. 43 ~ 36 (FP-54)
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The bi-directional data lines ($D_0 \sim D_7$) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The R/\bar{W} line is in the Read ("High") state when the PIA is selected for a Read operation.

- Enable (E)

Input/Output	Pin No. 25 (DP-40) Pin No. 32 (FP-54)
--------------	--

The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the HMCS6800 System ϕ_2 Clock. This signal must be continuous clock pulse.

- Read/Write (R/\bar{W})

Input	Pin No. 21 (DP-40) Pin No. 28 (FP-54)
-------	--

This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A "Low" state on the PIA line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A "High" on the R/\bar{W} line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

- Reset (\bar{RES})

Input	Pin No. 34 (DP-40) Pin No. 44 (FP-54)
-------	--

The active "Low" \bar{RES} line is used to reset all register bits in the PIA to a logical zero "Low". This line can be used as a power-on reset and as a master reset during system operation.

- Chip Select (CS_0 , CS_1 and \bar{CS}_2)

Input	Pin No. 22, 24, 23 (DP-40) Pin No. 29, 31, 30 (FP-54)
-------	--

These three input signals are used to select the PIA. CS_0 and CS_1 must be "High" and \bar{CS}_2 must be "Low" for selection of the device. Data transfers are then performed under the control of the E and R/\bar{W} signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

- Register Select (RS_0 and RS_1)

Input	Pin No. 36, 35 (DP-40) Pin No. 50, 45 (FP-54)
-------	--

The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

- Interrupt Request (\bar{IRQA} and \bar{IRQB})

Input	Pin No. 38, 37 (DP-40) Pin No. 52, 51 (FP-54)
-------	--

The active "Low" Interrupt Request lines (\bar{IRQA} and \bar{IRQB}) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each \bar{IRQ} line has two internal interrupt flag bits that can cause the \bar{IRQ} line to go "Low". Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA_1 , CA_2 , CB_1 , CB_2). When these lines are used as interrupt inputs at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.



PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

There is difference between HD6821 and HD6321 in Port structure. Fig. 15 shows the block diagram of Port A and Port B in HD6321. The output drivers of Port A and Port B consist of three-state drivers, allowing them to enter a High-impedance state when the peripheral data line is used as an input. Port A and Port B have the same output buffer. But the circuit configuration is slightly different and this makes the difference on data flow when MPU reads Port A and Port B in the case each

Port is specified as output. As shown in Fig. 15, the output of the peripheral data A is transferred to internal data bus when used as output. On the other hand, in the case of Port B the contents of output register (ORB) is directly transferred to internal data bus through the multiplexor.

Secondly the equivalent circuit of the port in HD6821 is shown in Fig. 16. The output circuits of A port is different from that of B port. When the port is used as input, the input is pullup to V_{CC} side through load MOS in A port and B port becomes "Off" (high impedance).

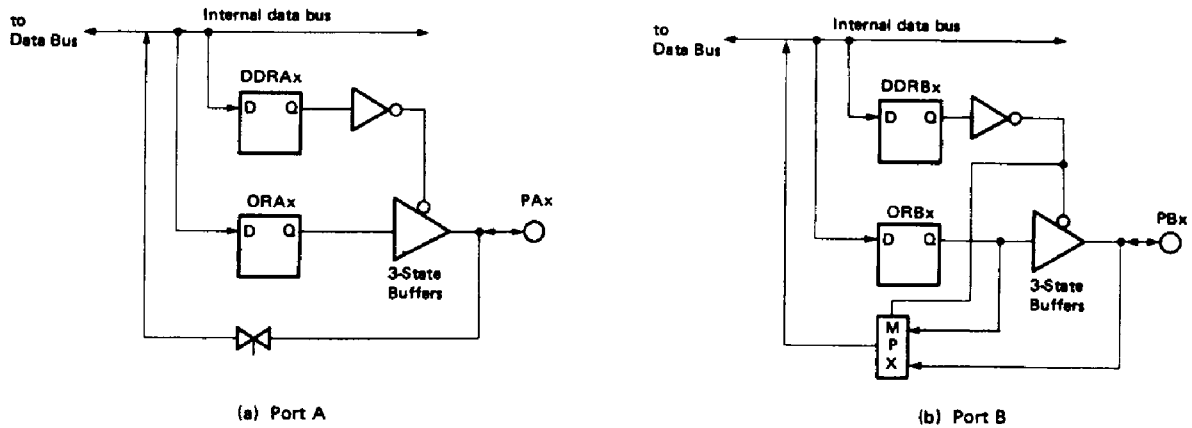


Figure 15 Block Diagram of Port A and Port B (HD6321)

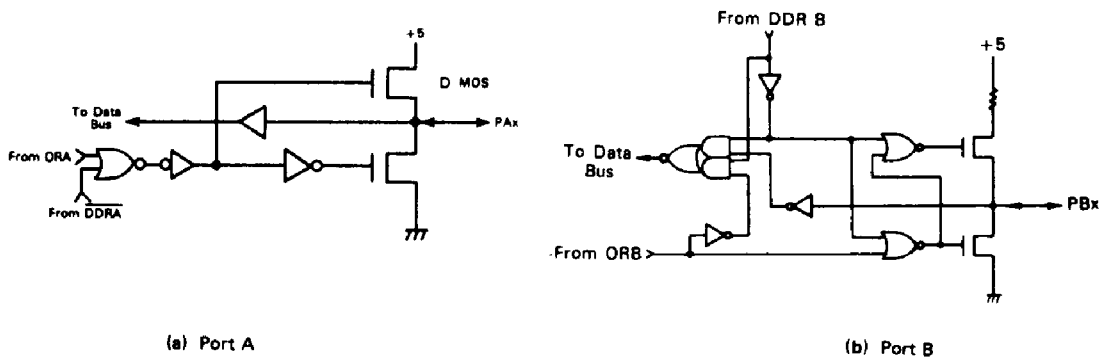


Figure 16 Circuit of Port A and Port B (HD6821)



● Port A Peripheral Data (PA₀~PA₇)

Input/Output Pin No. 2~ 9 (DP-40)
Pin No. 2~ 5, 9~ 12 (FP-54)

Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines.

The data in Output Register A will appear on the peripheral data lines that are programmed to be outputs. A logical "1" written into the register will cause a "High" on the corresponding peripheral data line while a "0" results in a "Low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs.

But concerning HD6821, this data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

● Port B Peripheral Data (PB₀ ~ PB₇)

Input/Output Pin No. 10 ~ 17 (DP-40)
Pin No. 13 ~ 18, 23 ~ 24 (FP-54)

Each of the Port B peripheral data bus can be programmed to act as an input or output like PA₀ ~ PA₇.

PB₀ ~ PB₇ are in High-impedance condition because they are three-state outputs just like PA₀ ~ PB₀ when the peripheral buses are used as inputs, when programmed as outputs, MPU read of Port B make it possible to read the output register regardless of PB₀ ~ PB₇ loads and concerning HD6821, these line may be used as a source of up to 2.5 milliampere (typ.) at 1.5 volt to directly drive the base of transistor switch.

● Interrupt Input (CA₁ and CB₁)

Input Pin No. 40, 18 (DP-40)
Pin No. 54, 25 (FP-54)

The peripheral Input lines CA₁ and CB₁ are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

● Peripheral Control (CA₂)

Input/Output Pin No. 39 (DP-40)
Pin No. 53 (FP-54)

The peripheral control line CA₂ can be programmed to act as an interrupt input or as a peripheral control output.

The function of this signal is programmed by the Control Register A. When used as an input, this signal is in High-impedance state.

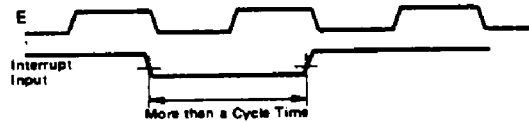
● Peripheral Control (CB₂)

Input/Output Pin No. 19 (DP-40)
Pin No. 26 (FP-54)

The peripheral Control line CB₂ may also be programmed to act as an interrupt input or peripheral control output.

This line is programmed by Control Register B. When used as an input, this signal is in High-impedance.

(NOTE) 1. Pulse width of interrupt inputs CA₁, CA₂, CB₁ and CB₂ shall be greater than a E cycle time. In the case that "High" time of E signal is not contained in interrupt pulse, an interrupt flag may not be set.



Electrical Characteristics

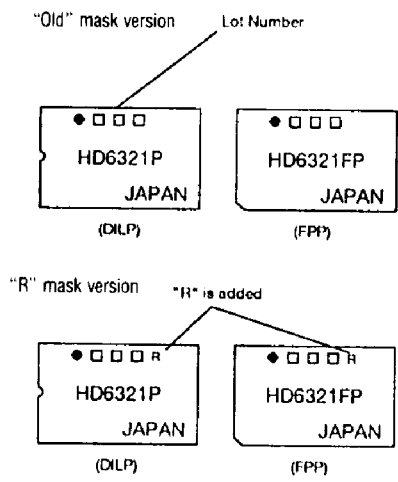
(1) DC Characteristics

Item	Symbol	old mask		R mask		Unit	
		min.	max.	min.	max.		
Input "High" Voltage	D ₀ -D ₇ , PA ₀ -PA ₇ , PB ₀ -PB ₇ , CA ₁ , CA ₂ , CB ₁ , CB ₂	V _{IH}	2.2	V _{CC}	2.2	V _{CC}	V
	E, R/W, CS ₀ , CS ₁ , CS ₂ , RS ₀ , RS ₁ , RES		3.0	V _{CC}			

(2) AC Characteristics (Only for HD63B21)

Item	Symbol	old mask		R mask		Unit
		min.	max.	min.	max.	
Bus Timing (READ) Setup Time (Address, R/W-Enable)	t _{AS}	60		40		ns
Bus Timing (WRITE) Setup time (Address, R/W-Enable)	t _{AS}	60		40		ns





INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS_0 and RS_1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Table 1 Internal Addressing

RS_1	RS_0	Control Register Bit		Location Selected
		CRA2	CRB2	
0	0	1	x	Peripheral Register A*
0	0	0	x	Data Direction Register A
0	1	x	x	Control Register A
1	0	x	1	Peripheral Register B*
1	0	x	0	Data Direction Register B
1	1	x	x	Control Register B

x = Don't Care
 * Peripheral interface register is a generic term containing peripheral data bus and output register.

Initialization
 A "Low" reset line has the effect of zeroing all PIA registers. This will set $PA_0 \sim PA_7$, $PB_0 \sim PB_7$, CA_2 and CB_2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.
 Details of possible configurations of the Data Direction and Control Register are as follows.

Data Direction Registers (DDRA and DDRB)
 The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the

corresponding peripheral data line as an input; a "1" results in an output.

Control Registers (CRA and CRB)
 The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA_1 , CA_2 , CB_1 and CB_2 . In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA_1 , CA_2 , CB_1 or CB_2 . The format of the control words is shown in Table 2.

Table 2 Control Word Format

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA ₁ Control		DDRA Access	CA ₁ Control		
CRB	IRQB1	IRQB2	CB ₁ Control		DDRB Access	CB ₁ Control		

Data Direction Access Control Bit (CRA2 and CRB2)
 Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS_0 and RS_1 .

Interrupt Flags (CRA6, CRA7, CRB6, and CRB7)
 The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Control of CA₁ and CB₁ Interrupt Lines (CRA0, CRB0, CRA1, and CRB1)

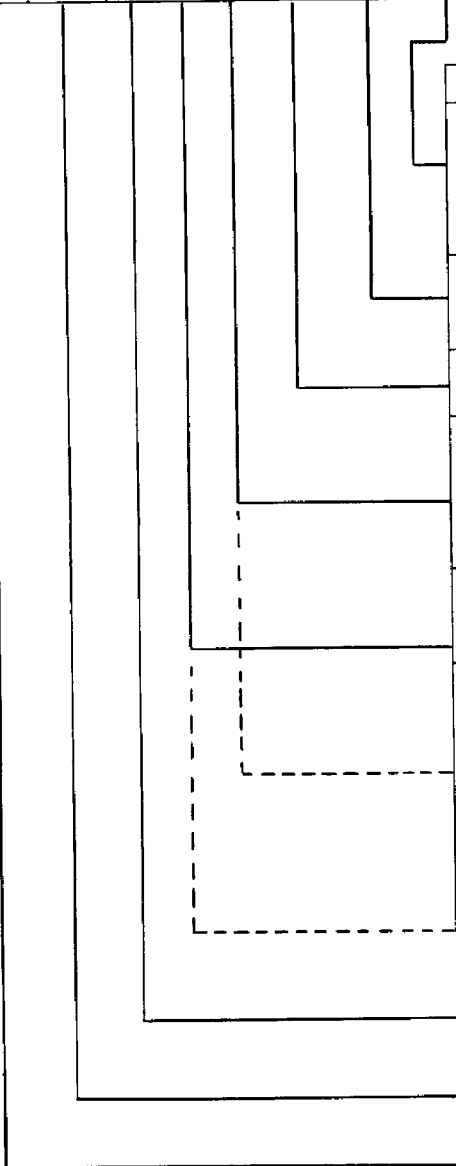
The two lowest order bits of the control registers are used to control the interrupt input lines CA_1 and CB_1 . Bits CRA0 and CRB0 are used to enable the MPU interrupt signals \overline{IRQA} and \overline{IRQB} , respectively. Bits CRA1 and CRB1 determine the active transition of the interrupt input signals CA_1 and CB_1 (Table 3)
Control of CA₂ and CB₂ Peripheral Control Lines (CRA3, CRA4, CRA5, CRB3, CRB4, and CRB5)

Bits 3, 4 and 5 of the two control registers are used to control the CA_2 and CB_2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA5 (CRB5) is "0" CA_2 (CB_2) is an interrupt input line similar to CA_1 (CB_1) (Table 4). When CRA5 (CRB5) is "1", CA_2 (CB_2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA_2 and CB_2 have slightly different characteristics (Table 5 and 6).



Control Register A (CRA)

7	6	5	4	3	2	1	0
IRQA ₁	IRQA ₂	Control CA ₂	DDRA	Control CA ₁			



Bit	0	1
CRA0 (CA ₁ Peripheral Control Lines)	CA ₁ interrupt output mask bit CRA7 (IRQA ₁) is set according to the interrupt signal CA ₁ , but \overline{IRQA} is masked and not output (in short, $\overline{IRQA} = \text{'high'}$).	CA ₁ interrupt output mask bit CRA7 (IRQA ₁) is set according to the interrupt signal CA ₁ , and \overline{IRQA} changes 'low'.
CRA1 (CA ₁ active edge bit)	CRA7 (IRQA ₁) is set when CA ₁ is fallen.	CRA7 (IRQA ₁) is set when CA ₁ is risen.
CRA2	Data direction register A (DDRA)	Peripheral interface register A
CRA3 CA ₂ (Peripheral Control Line)	CA ₂ interrupt output mask bit CRA6 (IRQA ₂) is set according to the interrupt signal CA ₂ , but \overline{IRQA} is masked and not output (in short, $\overline{IRQA} = \text{'high'}$).	CA ₂ interrupt output mask bit CRA6 (IRQA ₂) is set according to the interrupt signal CA ₂ . And \overline{IRQA} changes 'low'.
CRA4 CA ₂ (active edge bit)	CRA6 is set when CA ₂ is fallen	CRA6 is set when CA ₂ is risen.
CRA3	CRA4 = 0 Handshake mode bit The output CA ₂ is 'low' when 'E' pulse is fallen on MPU is read the data from Peripheral Interface Register A and CA ₂ is 'high' when CB ₁ is active (edge).	CRA4 = 0 Handshake mode bit After reading, CA ₂ is 'high' when next 'E' pulse is fallen on MPU is read the data from Interface Register A and, after reading, CA ₂ is 'high' when next 'E' pulse is fallen.
CRA4	CRA3 is the handshake mode bit.	The content of CRA3 is out to CA ₂ .
CRA5 CA ₂ input/output select bit	CA ₂ is input mode	CA ₂ is output mode
CRA6 (IRQA ₂)	No interrupt request from CA ₂ or CA ₂ is output (Reset Mode)	Interrupt request from CA ₂ is occurred.
CRA7 (IRQA ₁)	No interrupt request from CA ₁ .	Interrupt request from CA ₁ is occurred.



Control Register B (CRB)

7	6	5	4	3	2	1	0
IRQB ₁	IRQB ₂	Control CB ₂		DDRB	Control CB ₁		

Bit	0	1
CRB0 (CB ₁ Peripheral Control Lines)	CB ₁ , interrupt output mask bit CRB7 (IRG B ₁) is set according to the interrupt signal CB ₁ , but \overline{IRQB} is masked and not output (in short, $\overline{IRQB} = \text{'high'}$).	CB ₁ interrupt output mask bit CRB7 (IRQB ₁) is set according to the interrupt signal CB ₁ , and \overline{IRQB} changes 'low'.
CRB1 (CB ₁ active edge bit)	CRB7 (IRQB ₁) is set when CA ₁ is fallen.	CRB7 (IRQB ₁) is set when CA ₁ is risen.
CRB2	Data direction register B (DDRB)	Peripheral interface register B
CRB3 CB ₂ (Peripheral Control Line)	CB ₂ CB ₂ interrupt output mask bit CBR6 (IRQB ₂) is set according to the interrupt signal CB ₂ , but \overline{IRQB} is masked and not output (in short, $\overline{IRQB} = \text{'high'}$).	CB ₂ interrupt output mask bit CBR6 (IRQB ₂) is set according to the interrupt signal CB ₂ . And \overline{IRQB} changes 'low'.
CRB4 CB ₂ (active edge bit)		
CRB3	CRB4 = 0 Handshake mode bit The output CB ₂ is 'low' when 'E' pulse is fallen on MPU is read the data from Peripheral Interface Register B and CB ₂ is 'high' when CB ₁ is active (edge).	CRB4 = 0 Handshake mode bit After reading, CB ₂ is 'high' when next 'E' pulse is fallen on MPU is read the data from Interface Register B and, after reading, CB ₂ is 'high' when next 'E' pulse is fallen.
CRB4	CRB3 is the handshake mode bit.	The content of CRB3 is out to CB ₂ .
CRB5 CB ₂ input/output select bit	CB ₂ is input mode	CB ₂ is output mode
CRB6 (IRQB ₂)	No interrupt request from CB ₂ or CB ₂ is output (Reset Mode)	Interrupt request from CB ₂ is occurred.
CRB7 (IRQB ₁)	No interrupt request from CB ₁ .	Interrupt request from CB ₁ is occurred.



Table 3 Control of Interrupt Inputs CA₁ and CB₁

CRA1 (CRB1)	CRA0 (CRB0)	Interrupt Input CA ₁ (CB ₁)	Interrupt Flag CRA7 (CRB7)	MPU Interrupt Request IROA (IROB)
0	0	↓ Active	Set "1" on ↓ of CA ₁ (CB ₁)	Disabled – IRO remains "High"
0	1	↓ Active	Set "1" on ↓ of CA ₁ (CB ₁)	Goes "Low" when the interrupt flag bit CRA7 (CRB7) goes "1"
1	0	↑ Active	Set "1" on ↑ of CA ₁ (CB ₁)	Disabled – IRO remains "High"
1	1	↑ Active	Set "1" on ↑ of CA ₁ (CB ₁)	Goes "Low" when the interrupt flag bit CRA7 (CRB7) goes "1"

- (Notes)
- ↑ indicates positive transition ("Low" to "High")
 - ↓ indicates negative transition ("High" to "Low")
 - The Interrupt flag bit CRA7 is cleared by an MPU Read of the A Peripheral Register and CRB7 is cleared by an MPU Read of the B Peripheral Register.
 - If CRA0 (CRB0) is "0" when an interrupt occurs (Interrupt disabled) and is later brought "1", IROA (IROB) occurs after CRA0 (CRB0) is written to a "1".

Table 4 Control of CA₂ and CB₂ as Interrupt Inputs – CRA5 (CRB5) is "0"

CRA5 (CRB5)	CRA4 (CRB4)	CRA3 (CRB3)	Interrupt Input CA ₂ (CB ₂)	Interrupt Flag CRA6 (CRB6)	MPU Interrupt Request IROA (IROB)
0	0	0	↓ Active	Set "1" on ↓ of CA ₂ (CB ₂)	Disabled – IRO remains "High"
0	0	1	↓ Active	Set "1" on ↓ of CA ₂ (CB ₂)	Goes "Low" when the interrupt flag bit CRA6 (CRB6) goes "1"
0	1	0	↑ Active	Set "1" on ↑ of CA ₂ (CB ₂)	Disabled – IRO remains "High"
0	1	1	↑ Active	Set "1" on ↑ of CA ₂ (CB ₂)	Goes "Low" when the interrupt flag bit CRA6 (CRB6) goes "1"

- (Notes)
- ↑ indicates positive transition ("Low" to "High")
 - ↓ indicates negative transition ("High" to "Low")
 - The interrupt flag bit CRA6 is cleared by an MPU Read of the A Peripheral Register and CRB6 is cleared by an MPU Read of the B Peripheral Register.
 - If CRA3 (CRB3) is "0" when an interrupt occurs (Interrupt disabled) and is later brought "1", IROA (IROB) occurs after CRA3 (CRB3) is written to a "1".

Table 5 Control of CB₂ as an Output – CRB5 is "1"

CRB5	CRB4	CRB3	CB ₂	
			Cleared	Set
1	0	0	"Low" on the positive transition of the first E pulse after MPU Write "B" Data Register operation.	"High" when the interrupt flag bit CRB7 is set by an active transition of the CB ₁ signal. (See Figure 16)
1	0	1	"Low" on the positive transition of the first E pulse after an MPU Write "B" Data Register operation.	"High" on the positive edge of the first "E" pulse following an "E" pulse which occurred while the part was deselected. (See Figure 16)
1	1	0	"Low" (The content of CRB3 is output on CB ₂)	
1	1	1	"High" (The content of CRB3 is output on CB ₂)	



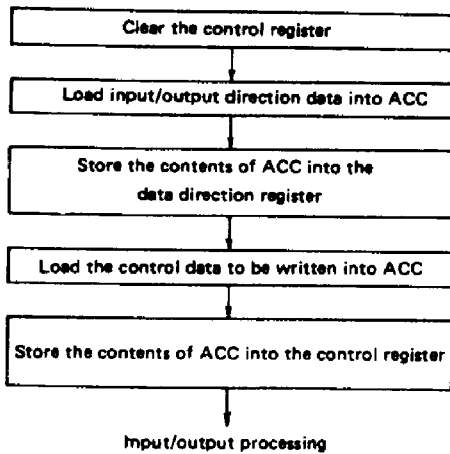
Table 6 Control of CA₂ as an Output – CRA5 is "1"

CRA5	CRA4	CRA3	CA ₂	
			Cleared	Set
1	0	0	"Low" on negative transition of E after an MPU Read "A" Data Operation.	"High" when the interrupt flag bit CRA7 is set by an active transition of the CA ₁ signal. (See Figure 16)
1	0	1	"Low" on negative transition of E after an MPU Read "A" Data operation.	"High" on the negative edge of the first "E" pulse which occurs during a deselect. (See Figure 16)
1	1	0	"Low" (The content of CRA3 is output on CA ₂)	
1	1	1	"High" (The content of CRA3 is output on CA ₂)	

PIA OPERATION

Initialization

When the external reset input \overline{RES} goes "Low", all internal registers are cleared to "0". Peripheral data port (PA₀~PA₇, PB₀~PB₇) is defined to be input and control lines (CA₁, CA₂, CB₁ and CB₂) are defined to be the interrupt input lines. PIA is also initialized by software sequence as follows.

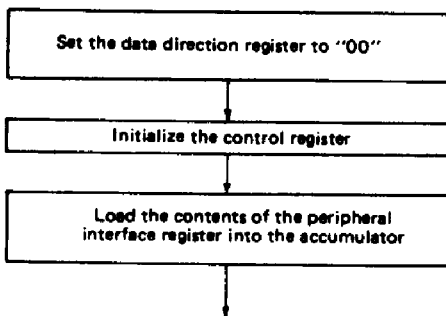


- Program the data direction register access bit of the control register to "0" to allow to access the data direction register.

- The data of the control line function is set into the accumulator, of which Data Direction Register Access Bit shall be programmed to "1".
- Transfer the control data from the accumulator into the control register.

Read/Write Operation Not Using Control Lines

<Read Operation>

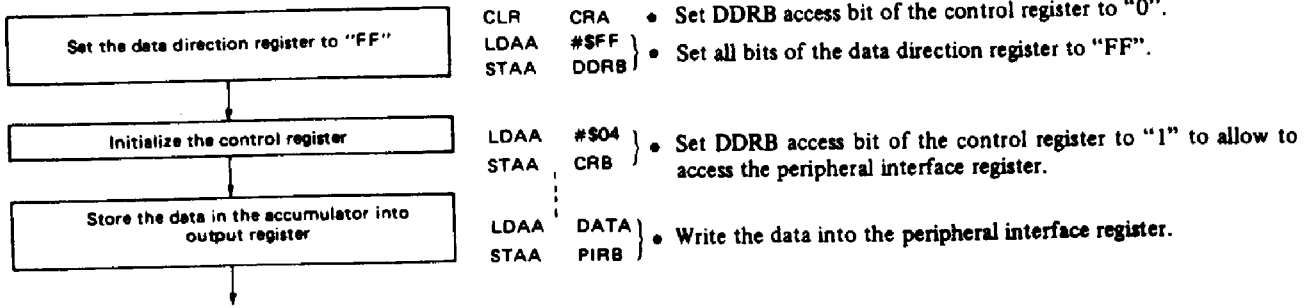


CLR CRA
CLR DDRA
LDAA #04
STAA CRA
LDAA PIRA

- Clear the DDRA access bit of the control register to "0".
- Clear all bits of the data direction register.
- Set DDRA access bit of the control register to "1" to allow to access the peripheral interface register.



<Write Operation>

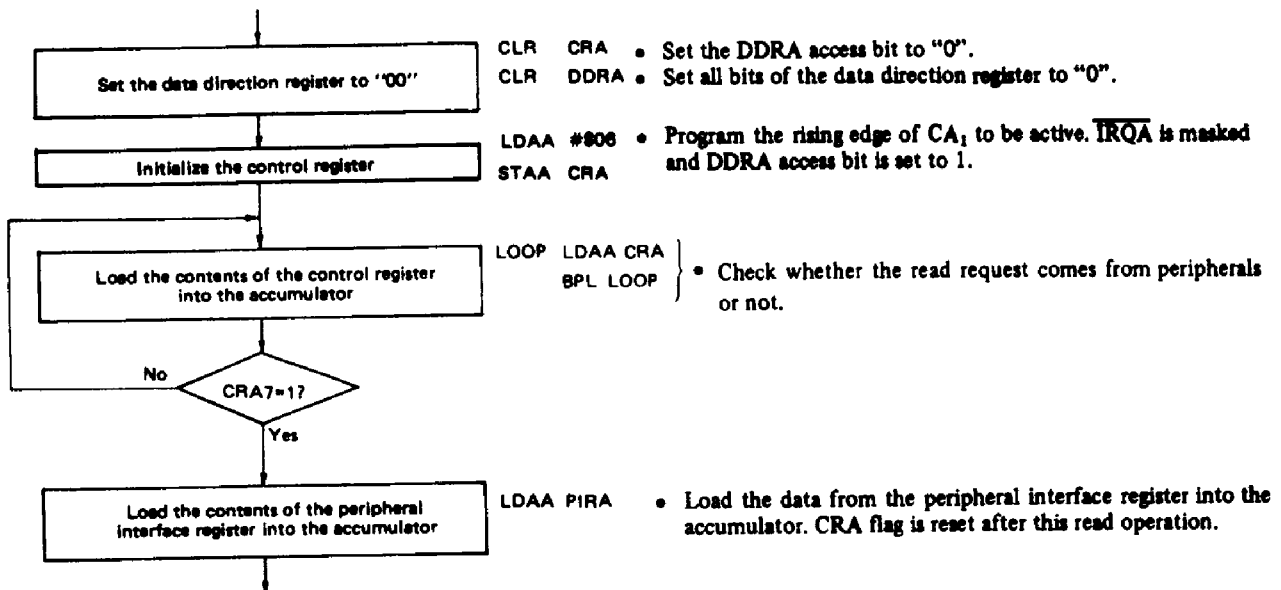


• Read/Write Operating Using Control Lines

Read/write request from peripherals shall be put into the control lines as an interrupt signal, and then MPU reads or writes after detecting interrupt request.

< Read >

The following case is that Port A is used and that the rising edge of CA₁ indicates the request for read from peripherals.



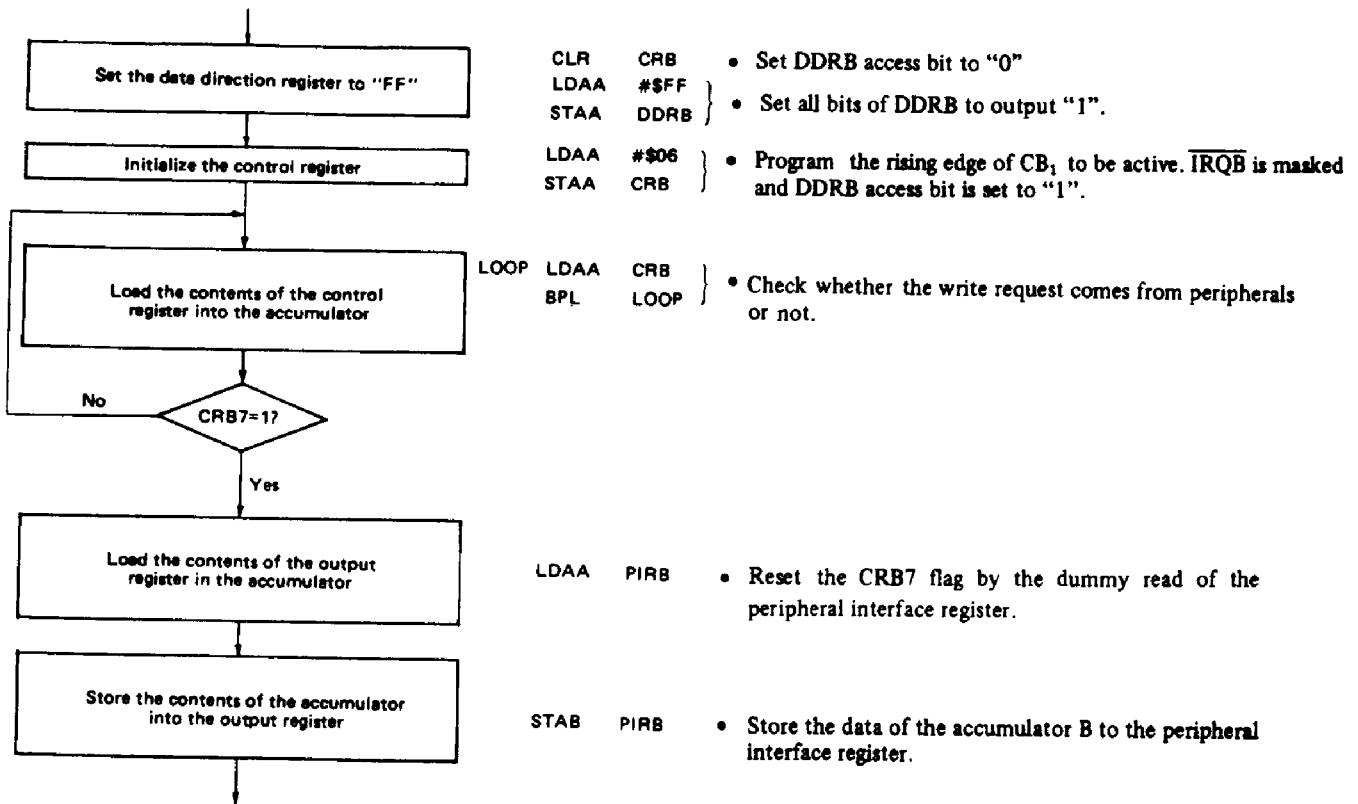
To read the peripheral data, the data is directly transferred to the data buses D₀~D₇ through PA₀~PA₇ or PB₀~PB₇, and they are not latched in the PIA. If necessary, the data should be held in the external latch until MPU completes reading it.

When initializing the control register, interrupt flag bit (CRA7, CRA6, CRB7, CRB6) cannot be written from MPU. If necessary the interrupt flag must be reset by dummy read of Peripheral Register A and B.

<Write>

Write operation using the interrupt signal is as follows. In this case, B port is used and interrupt request is input to CB₁. And the IRQ flag is set at the rising edge of CB₁.





Interrupt request flag bits (CRA7, CRA6, CRB7 and CRB6) cannot be written and they cannot be also reset by write operation to the peripheral interface register. So dummy read of peripheral interface register is needed to reset the flags.

To accept the next interrupt, it is essential to reset indirectly the interrupt flag by dummy read of peripheral interface register.

Software polling method mentioned above requires MPU to continuously monitor the control register to detect the read/write request from peripherals. So other programs cannot run at the same time. To avoid this problem, hardware interrupt may be used. The MPU is interrupted by \overline{IRQA} or \overline{IRQB} when the read/write request is occurred from peripherals and then MPU analyzes cause of the interrupt request during interrupt processing.

• Handshake Mode

The functions of CRA and CRB are similar but not identical in the hand-shake modes. Port A is used for read hand-shake operation and Port B is used for write hand-shake mode.

CA₁ and CB₁ are used for interrupt input requests and CA₂ and CB₂ are control outputs (answer) in hand-shake mode.

Fig. 17, Fig. 18 and Fig. 19 show the timing of hand-shake mode.

< Read Hand-shake Mode >

CRA5="1", CRA4="0" and CRA3="0"

- ① A peripheral device puts the 8-bit data on the peripheral data lines after the control output CA₂ goes "Low".
- ② The peripheral requests MPU to read the data by using CA₁ input.

- ③ CRA7 flag is set and CA₂ becomes "High" (CA₂ automatically becomes "High" by the interrupt CA₁). This indicates the peripheral to maintain the current data and not to transfer the next data.
- ④ MPU accepts the read request by \overline{IRQA} hardware interrupt or CRA read. Then MPU reads the peripheral register A.
- ⑤ CA₂ goes "Low" on the following edge of read Enable pulse. This informs that the peripheral can set the next data to port A.

< Write Hand-shake >

CRB5 = "1", CRB4 = "0" and CRB3 = "0"

- ① A peripheral device requests MPU to write the data by using CB₁ input. CB₂ output remains "High" until MPU write data to the peripheral interface register.
- ② CRB7 flag is set and MPU accepts the write request.
- ③ MPU reads the peripheral interface register to reset CRB7 (dummy read).
- ④ Then MPU write data to the peripheral interface register. The data is output to port B through the output register.
- ⑤ CB₂ automatically becomes "Low" to tell the peripheral that new data is on port B.
- ⑥ The peripheral read the data on Port B peripheral data lines and set CB₁ to "Low" to tell MPU that the data on the peripheral data lines has been taken and that next data can be written to the peripheral interface register.

< Pulse mode >

CRA5 = "1", CRA4 = "0" and CRA3 = "1"

CRB5 = "1", CRB4 = "0" and CRB3 = "1"

This mode is shown in Figure 17, Figure 20 and Figure 21.



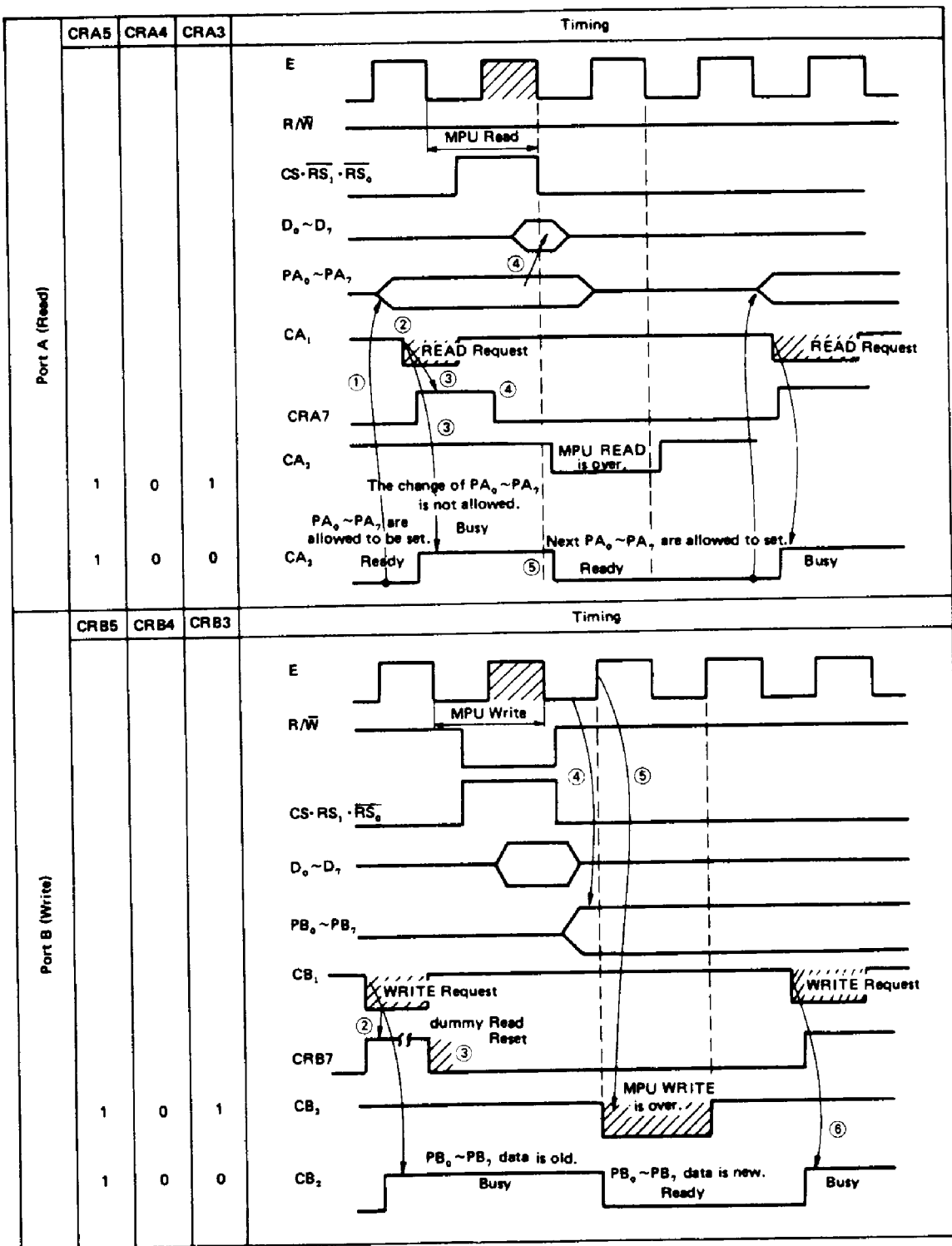


Figure 17 Timing of Hand-shake Mode and Pulse Mode



4

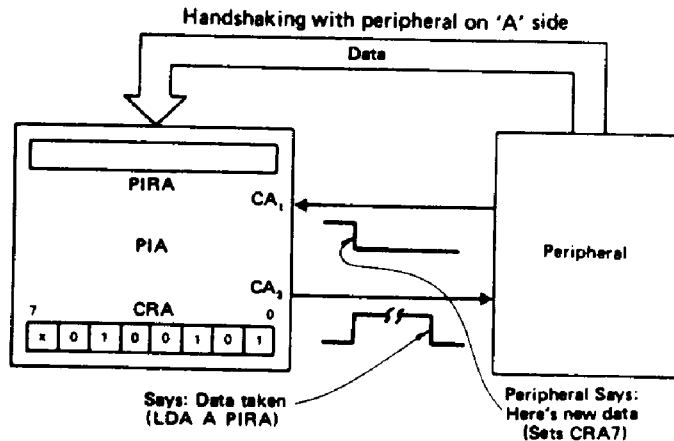
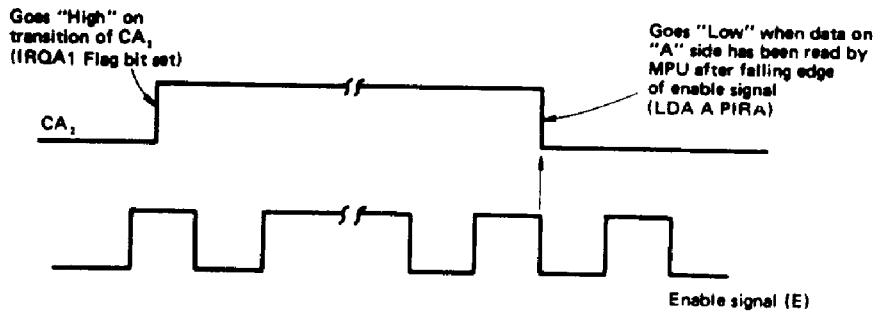


Figure 18 Bits 5, 4, 3 of CRA = 100 (Hand-shake Mode)

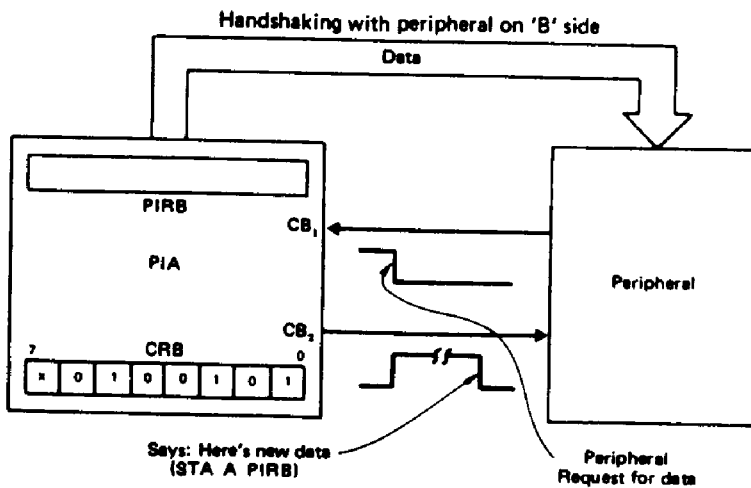
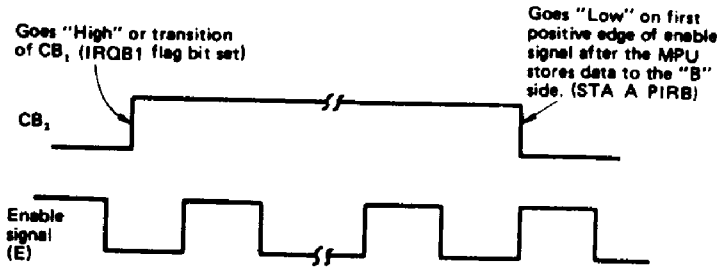


Figure 19 Bits 5, 4, 3 of CRB = 100 (Hand-shake Mode)



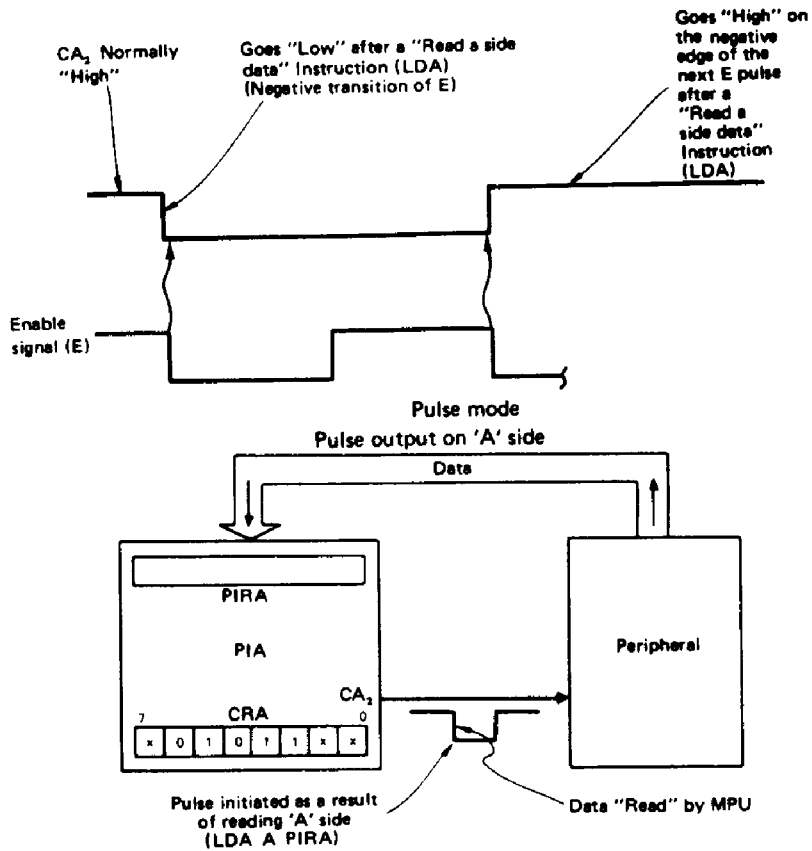


Figure 20 Bits 5, 4, 3 of CRA = 101 (Pulse Mode)

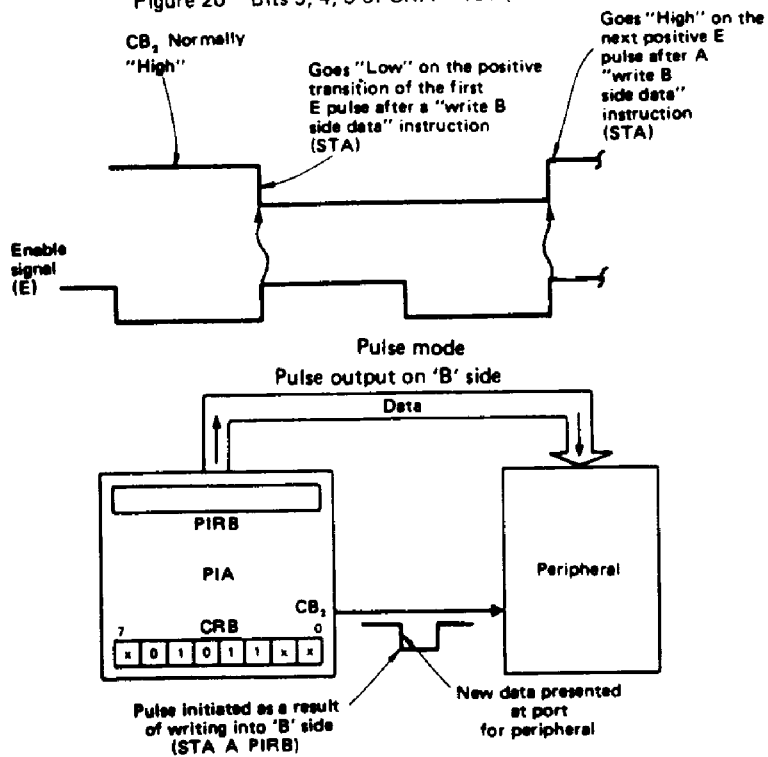


Figure 21 Bits 5, 4, 3 of CRB = 101 (Pulse Mode)



■ SUMMARY OF CONTROL REGISTERS CRA AND CRB

Control registers CRA and CRB have total control of CA₁, CA₂, CB₁, and CB₂ lines. The status of eight bits of the control registers may be read into the MPU. However, the MPU can only write into Bit 0 through Bit 5 (6 bits), since Bit 6 and Bit 7 are set only by CA₁, CA₂, CB₁, or CB₂.

● Addressing PIAs

Before addressing PIAs, the data direction (DDR) must first be loaded with the bit pattern that defines how each line is to function, i.e., as an input or an output. A logic "1" in the data direction register defines the corresponding line as an output while a logic "0" defines the corresponding line as an input. Since the DDR and the peripheral interface register have the same address, the control register bit 2 determines which register is being addressed. If Bit 2 in the control register is a logic "0", then the DDR is addressed. If Bit 2 in the control register is a logic "1", the peripheral interface register is addressed. Therefore, it is essential that the DDR be loaded first before setting Bit 2 of the control register.

<Example>

Given a PIA with an address of 4004, 4005, 4006, and 4007. 4004 is the address of the A side peripheral interface register. 4005 is the address of the A side control register. 4006 is the address of the B side peripheral interface register. 4007 is the address of the B side control register. On the A side, Bits 0, 1, 2, and 3 will be defined as inputs, while Bits 4, 5, 6, and 7 will be used as outputs. On the B side, all lines will be used as outputs.

PIA1AD = 4004 (DDRA, PIRA)
 PIA1AC = 4005 (CRA)
 PIA1BD = 4006 (DDRB, PIRB)
 PIA1BC = 4007 (CRB)

1. LDA A #%11110000 (4 outputs, 4 inputs)
2. STA A PIA1AD (Loads A DDR)
3. LDA A #%11111111 (All outputs)
4. STA A PIA1BD (Loads B DDR)
5. LDA A #%00000100 (Sets Bit 2)
6. STA A PIA1AC (Bit 2 set in A control register)
7. STA A PIA1BC (Bit 2 set in B control register)

Statement 2 addresses the DDR, since the control register (Bit 2) has not been loaded. Statements 6 and 7 load the control registers with Bit 2 set, so addressing PIA1AD or PIA1BD accesses the peripheral interface register.

● PIA Programming Via The Index Register

The program shown in the previous section can be accomplished using the Index Register.

1. LDX #F004
2. STX PIA1AD \$F0→PIA1AD;\$04→PIA1AC
3. LDX #FF04
4. STX PIA1BD \$FF→PIA1BD;\$04→PIA1BC

Using the index register in this example has saved six bytes of program memory as compared to the program shown in the previous section.

● Active Low Outputs

When all the outputs of given PIA port are to be active "Low" (True \leq 0.4 volts), the following procedure should be used.

- a) Set Bit 2 in the control register.
- b) Store all 1s (\$FF) in the peripheral interface register.
- c) Clear Bit 2 in the control register.
- d) Store all 1s (\$FF) in the data direction register.
- e) Store control word (Bit 2 = 1) in control register.

<Example>

The B side of PIA1 is set up to have all active low outputs. CB₁ and CB₂ are set up to allow interrupts in the HAND-SHAKE MODE and CB₁ will respond to positive edges ("Low"-to-"High" transitions). Assume reset conditions. Addresses are set up and equated to the same labels as previous example.

1. LDA A #4
2. STA A PIA1BC Set Bit 2 in PIA1BC (control register)
3. LDA B #\$FF
4. STA B PIA1BD All 1s in peripheral interface register
5. CLR PIA1BC Clear Bit 2
6. STA B PIA1BD All 1s in data direction register
7. LDA A #\$27
8. STA A PIA1BC 00100111→ control register

The above procedure is required in order to avoid outputs going "Low", to the active "Low" TRUE STATE, when all 1s are stored to the data direction register as would be the case if the normal configuration procedure were followed.

● Interchanging RS₀ And RS₁

Some system applications may require movement of 16 bits of data to or from the "outside world" via two PIA ports (A side + B side). When this is the case it is an advantage to interconnect RS₁ and RS₀ as follows.

RS₀ to A1 (Address Line A1)
 RS₁ to A0 (Address Line A0)

This will place the peripheral interface registers and control registers side by side in the memory map as follows.

Table	Example Address	
PIA1AD	\$4004	(DDRA, PIRA)
PIA1BD	\$4005	(DDRB, PIRB)
PIA1AC	\$4006	(CRA)
PIA1BC	\$4007	(CRB)

The index register or stackpointer may be used to move the 16-bit data in two 8-bit bytes with one instruction. As an example:

LDX PIA1AD PIA1AD → IX_H; PIA1BD → IX_L

● PIA - After Reset

When the \overline{RES} (Reset Line) has been held "Low" for a minimum of one microsecond, all registers in the PIA will be cleared.

Because of the reset conditions, the PIA has been defined as



follows.

1. All I/O lines to the "outside world" have been defined as inputs.
2. CA₁, CA₂, CB₁, and CB₂ have been defined as interrupt input lines that are negative edge sensitive.
3. All the interrupts on the control lines are masked. Setting of interrupt flag bits will not cause IRQA or IRQB to go "Low".

■ SUMMARY OF CA₁-CB₁ PROGRAMMING

Bits 1 and 0 of the respective control registers are used to program the interrupt input control lines CA₁ and CB₁.

b1	b0	
0	0	b1 = Edge (0 = -, 1 = +)
0	1	b0 = Mask (0 = Mask, 1 = Allow)
1	0	
1	1	

■ SUMMARY OF CA₂-CB₂ PROGRAMMING

Bits 5, 4, and 3 of the control registers are used to program the operation of CA₂-CB₂.

	b5	b4	b3	
CA ₂ -CB ₂ Input Mode →	0	0(-)	0	(Mask) CA ₂ -CB ₂ Input Mode
	0	0(-)	1	(Allow) b4 = Edge (0 = -, 1 = +)
	0	1(+)	0	(Mask) b3 = Mask (0 = Mask, 1 = Allow)
	0	1(+)	1	(Allow)
CA ₂ -CB ₂ Output Mode →	1	0	0	0 - Handshake Mode
	1	0	1	1 - Pulse Mode
	1	1	0	} b3 Following Mode
	1	1	1	

Note that this is the same logic as Bits 4 and 3 for CA₂-CB₂ when CA₂-CB₂ are programmed as inputs.

I/O As Follow:

Control Lines:

- CA₁ - Positive Edge, Allow Interrupt
- CA₂ - Pulse Mode
- CB₁ - Negative Edge, Mask Interrupt
- CB₂ - Hand Shake Mode

Assume Reset Condition

- PIA1AD
- PIA1AC
- PIA1BD
- PIA1BC

PIA Configuration Solution

```

LDA A #$BC      10111100
STA A PIA1AD    I/O to DDRA
LDA A #$FF      1111 1111
STA A PIA1BD    I/O to DDRB
LDA A #$2F      0010 1111
STA A PIA1AC    To "A" Control
LDA A #$24      0010 0100
STA A PIA1BC    To "B" Control
    
```

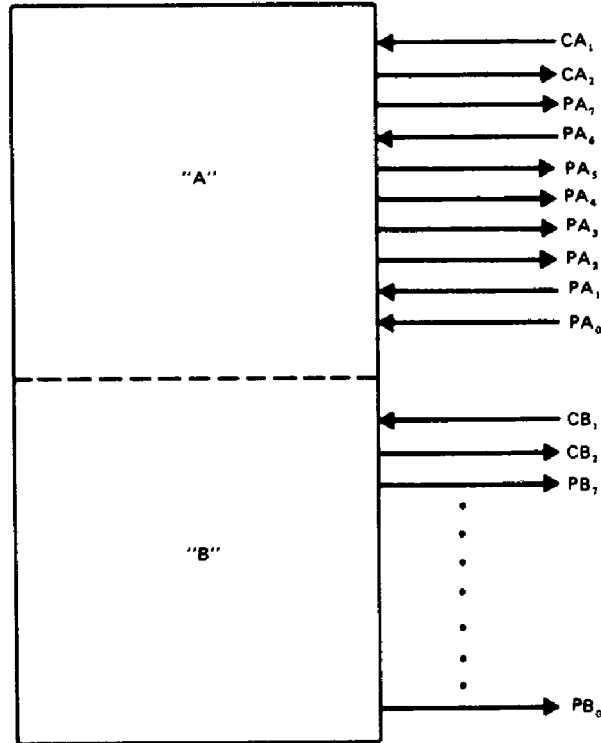


Figure 22 PIA Configuration Problem



HD6321/HD6821

■ NOTE FOR USE

Compatibility with NMOS PIA (HD6821)

Table 7 Comparison CMOS PIA (HD6321) with NMOS PIA (HD6821)

Item	CMOS PIA (HD6321)	NMOS PIA (HD6821)
Port A Output Buffer	<p>Three-state output</p>	<p>Pull-up output</p>
Port B Output Buffer	<p>Three-state output</p>	<p>Three-state output</p>

There is no difference between CMOS PIA and NMOS PIA in pin arrangement.

