FAIRCHILD
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F6821/F68A21/F68B21 Peripheral Interface Adapter (PIA)

Microprocessor Product

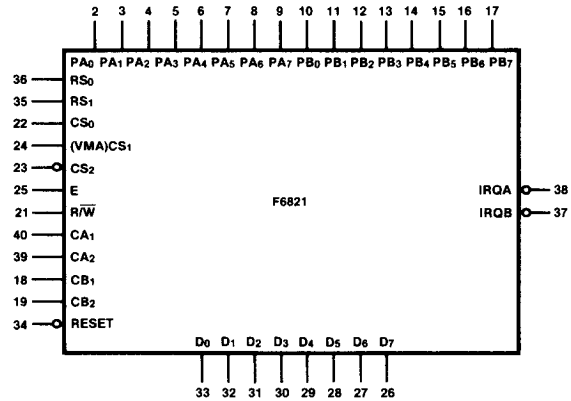
Description

The F6821 Peripheral Interface Adapter (PIA) provides a universal means of interfacing peripheral equipment to the F6800 microprocessing unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional data buses and four control lines, in three speed ranges: 1.0 MHz (F6821), 1.5 MHz (F68A21), and 2.0 MHz (F68B21). No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

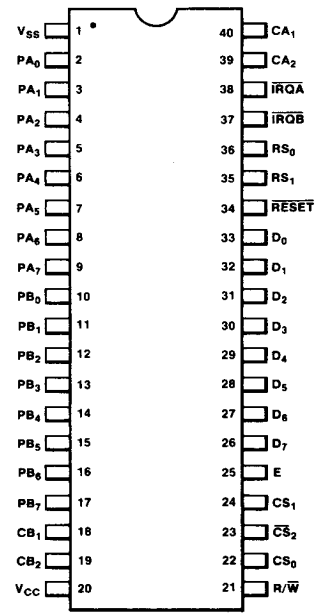
- **8-Bit Bidirectional Data Bus for Communication with the MPU**
- **Two Bidirectional 8-Bit Buses for Interface to Peripherals**
- **Two Programmable Control Registers**
- **Two Programmable Data Direction Registers**
- **Four Individually Controlled Interrupt Input Lines, Two Usable as Peripheral Control Outputs**
- **Handshake Control Logic for Input and Output Peripheral Operation**
- **High-Impedance 3-State and Direct Transistor Drive Peripheral Lines**
- **Program-Controlled Interrupt and Interrupt Disable Capability**
- **CMOS Drive Capability on Section A Peripheral Lines**
- **Two-TTL Drive Capability on All A- and B-Section Buffers**
- **TTL-Compatible**
- **Static Operation**

Logic Symbol



VCC = Pin 20
VSS = Pin 1

Connection Diagram
40-Pin DIP



(Top View)

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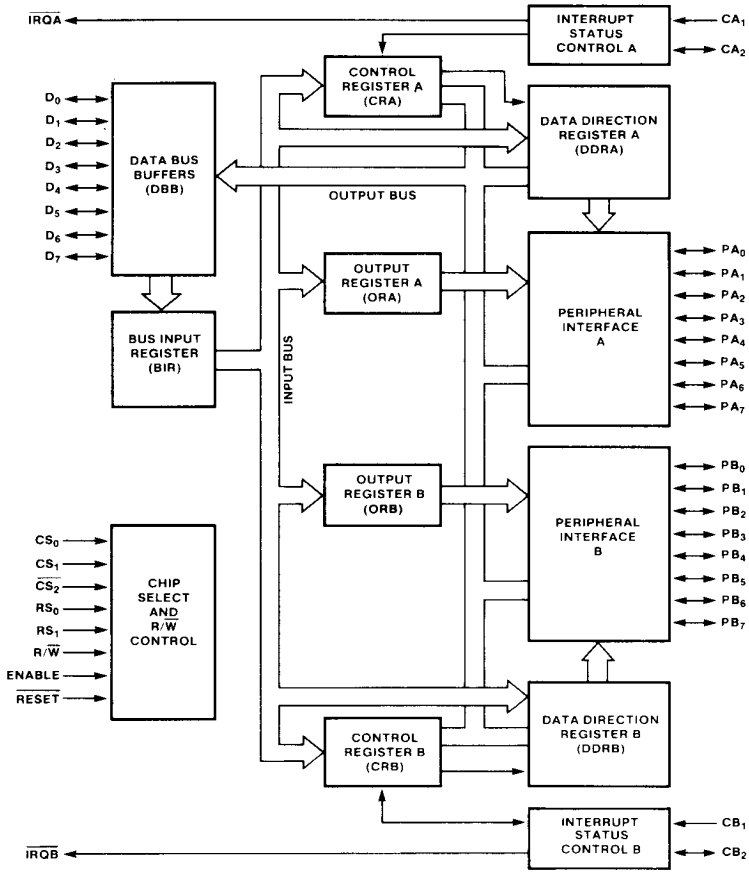
Block Diagram



PIA/MPU Interface Signals

The PIA interfaces to the F6800 MPU with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line, and a reset line (see *Figure 1*). These signals, in conjunction with the F6800 VMA output, permit the MPU to have complete control over the PIA. The VMA output should be utilized in conjunction with an MPU address line into a chip select of the PIA.

Data Bus (D_0 - D_7), Pins 26-33

The bidirectional data lines allow the transfer of data between the MPU and the PIA. The data bus output drivers are 3-state devices that remain in the high-impedance (OFF) state, except when the MPU performs a PIA read operation. The read/write (R/$\overline{W}$) line is in the read (HIGH) state when the PIA is selected for a read operation.

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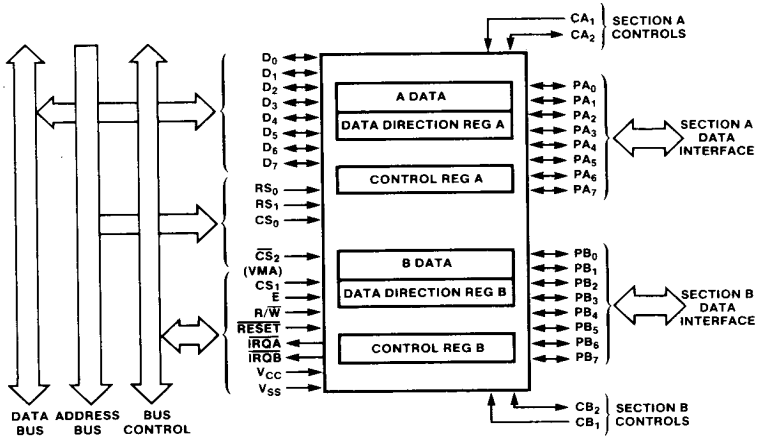
Fig. 1 PIA Bus Interface



Enable (E), Pin 25
The enable input pulse is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal is normally a derivative of the $\phi 2$ F6800 clock.

Read/Write (R/$\overline{W}$), Pin 21
This input signal is generated by the MPU to control the direction of data transfer on the data bus. A LOW on the R/$\overline{W}$ line enables the input buffers and allows data transfer from the MPU to the PIA on the E signal if the device has been selected. A HIGH on the R/$\overline{W}$ line sets up the PIA for a transfer of data to the bus; the PIA output buffers are enabled when the proper address and the E pulse are present.

Reset ($\overline{RESET}$), Pin 34
The active-LOW $\overline{RESET}$ input is used to reset all register bits in the PIA to a logic 0 (LOW) state. This line can be used as a power-on reset and as a master reset during system operation.

Chip Select (CS_0 - $\overline{CS_2}$), Pins 22-24
These three input signals are used to select the PIA. The CS_0 and CS_1 lines must be HIGH and $\overline{CS_2}$ must be LOW for selection of the device. Data transfers are then performed under control of the enable and read/write signals. The device is "deselected" when any of the chip select lines is in the inactive state.

The chip select lines should be stable for the duration of the E pulse.

Register Select (RS_0, RS_1), Pins 35, 36
The two register select inputs are used to select the various registers within the PIA. These two lines are used in conjunction with internal control registers to select a particular register that is to be written to or read from.

The register select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$), Pins 37, 38
The active-LOW interrupt request inputs act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are open drain (no load device on the chip). This permits all interrupt request lines to be tied together in a wired-OR configuration.

Each interrupt request line has two internal interrupt flag bits that can cause either line to go LOW. Each flag bit is associated with a particular peripheral interrupt line. Four interrupt enable bits are also provided in the PIA; these may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a priority basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (set to 0) as a result of an MPU read peripheral data operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled until the PIA is "deselected" during an E pulse. The E pulse is used to condition the interrupt control lines (CA_1, CA_2, CB_1, CB_2). When these

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lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been conditioned properly, the interrupt flag is set on the next active transition of the interrupt input pin.

PIA/Peripheral Interface Signals

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA_0 - PA_7), Pins 2-9
Each of the peripheral data lines is programmed to act as an input or output. This is accomplished by setting a 1 in the corresponding data direction register (DDR) bit for those lines that are to be outputs. A 0 in a bit of the DDR causes the corresponding peripheral data line to act as an input. During an MPU read peripheral data operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU data bus lines. In the input mode, the internal pull-up resistor on these lines represents a maximum of one standard TTL load.

The data in output register A (ORA) appears on the data lines that are programmed to be outputs. A logic 1 written into the register causes a HIGH on the corresponding data line, while a 0 results in a LOW. Data in ORA may be read by an MPU read peripheral data A operation when the corresponding lines are programmed as outputs. This data is read properly if the voltage on the peripheral data lines is greater than 2.0 V for a logic 1 output and less than 0.8 V for a logic 0 output. Loading the output lines in such a way that the voltage on these lines does not reach full voltage causes the data transferred into the MPU during a read operation to differ from that contained in the respective bit of output register A.

Section B Peripheral Data (PB_1 - PB_7), Pins 10-17
The peripheral data lines in the B section of the PIA can be programmed to act as either inputs or outputs in a manner similar to the A section lines. However, the output buffers driving these lines differ from those driving the A section lines, having a 3-state capability that allows them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on peripheral data lines PB_0 through PB_7 is read properly from those lines programmed as outputs even if the voltages are below 2.0 V for a HIGH. As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 mA at 1.5 V to drive the base of a transistor switch directly.

Interrupt Input (CA_1, CB_1), Pins 18 and 40
The interrupt input lines are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA_2, CB_2), Pins 39, 19
Peripheral control line CA_2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input, the internal pull-up resistor on this line represents one standard TTL load. The function of this signal line is programmed by control register A (CRA).

Peripheral control line CB_2 may also be programmed to act as in interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output, it is compatible with standard TTL and may also be used as a source of up to 1 mA at 1.5 V to drive the base of a transistor switch directly. This line is programmed by control register B (CRB).

It is recommended that the control lines (CA_1, CB_1, CA_2, CB_2) be held in a logic 1 state when the $\overline{RESET}$ line is active to prevent setting of corresponding interrupt flags in the control register when $\overline{RESET}$ goes to an inactive state. Subsequent to $\overline{RESET}$ going inactive, a read of the data registers may be used to clear any undesired interrupt flags.

Internal Controls

There are six locations within the PIA that are accessible to the MPU data bus: two peripheral registers, two data direction registers, and two control registers. Selection of these locations is controlled by the register select inputs, together with bit 2 in the control register, as shown in *Table 1*.

Table 1 Internal Addressing

		Control Register Bit		
RS_1	RS_0	CRA-2	CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

Initialization
A LOW on the $\overline{RESET}$ line has the effect of zeroing all PIA registers. This sets PA_0 - PA_7, PB_0 - PB_7, CA_2, and CB_2

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as inputs and disables all interrupts. The PIA must be configured during the restart program that follows the reset.

Register Operation

Possible configurations of the data direction and control registers are as follows:

Data Direction Registers (DDRA, DDRB)
The two data direction registers allow the MPU to control the direction of data through each corresponding peripheral data line. A DDR bit set to 0 configures the corresponding peripheral data line as an input; a 1 results in an output.

Control Registers (CRA, CRB)
The two control registers allow the MPU to control the operation of the four peripheral control lines (CA_1, CB_1, CA_2, and CB_2). In addition, they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written to or read from by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read-only and are modified by external interrupts occurring on the peripheral control lines. The format of the control words is shown in *Table 2*.

Table 2 Control Word Format

	7	6	5	4	3	2	1	0
CRA	$IRQA_1$	$IRQA_2$	CA_2 Control			DDRA Access	CA_1 Control	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRB	$IRQB_1$	$IRQB_2$	CB_2 Control			DDRB Access	CB_1 Control	

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Table 3 Interrupt Input Line Control Bits

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA_1 (CB_1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set HIGH on ↓ of CA_1 (CB_1).	Disabled; $\overline{IRQ}$ remains HIGH.
0	1	↓ Active	Set HIGH on ↓ of CA_1 (CB_1).	Goes LOW when interrupt flag bit CRA-7 (CRB-7) goes HIGH.
1	0	↑ Active	Set HIGH on ↑ of CA_1 (CB_1).	Disabled; $\overline{IRQ}$ remains HIGH.
1	1	↑ Active	Set HIGH on ↑ of CA_1 (CB_1).	Goes LOW when interrupt flag bit CRA-7 (CRB-7) goes HIGH.

Table 4 Peripheral Control Line Control Bits (CRA-5/CRB-5 LOW)

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA_2 (CB_2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set HIGH on ↓ CA_2 (CB_2).	Disabled; $\overline{IRQ}$ remains HIGH.
0	0	1	↓ Active	Set HIGH on ↓ of CA_2 (CB_2).	Goes LOW when interrupt flag bit CRA-6 (CRB-6) goes HIGH.
0	1	0	↑ Active	Set HIGH on ↑ of CA_2 (CB_2).	Disabled; $\overline{IRQ}$ remains HIGH.
0	1	1	↑ Active	Set HIGH on ↑ CA_2 (CB_2).	Goes LOW when interrupt flag bit CRA-6 (CRB-6) goes HIGH.

Notes
1. ↓ indicates negative transition (HIGH-to-LOW).
2. ↑ indicates positive transition (LOW-to-HIGH).
3. The interrupt flag bit, CRA-7, is cleared by an MPU read of the A data register, and CRB-7 is cleared by an MPU read of the B data register.
4. If CRA-0 (CRB-0) is LOW when an interrupt occurs (interrupt disabled) and is later brought HIGH, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a 1.

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Data Direction Access Control Bit (CRA-2, CRB-2)
Bit 2 in each control register allows selection of either a peripheral interface register (PIR) or the DDR when the proper register select signals are applied to RS_0 and RS_1.

Interrupt Flag Control Bits (CRA-6, CRA-7, CRB-6, CRB-7)
The four interrupt flag bits are set by active transitions of signals on the four interrupt and peripheral control lines when those lines are programmed to be input lines. These bits cannot be set directly from the MPU data bus and are reset indirectly by a read peripheral data operation on the appropriate section.

Interrupt Input Line Control Bits (CRA-0, CRA-1, CRB-0, CRB-1)
The two lowest-order bits of the control registers are used to control interrupt input lines CA_1 and CB_1. Bits CRA-0 and CRB-0 are used to enable MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals (see *Table 3*).

Peripheral Control Line Control Bits (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, CRB-5)
Bits 3, 4, and 5 of the two control registers are used to control the CA_2 and CB_2 peripheral control lines. These bits determine if the control lines act as interrupt inputs or as control outputs. If bit CRA-5 (CRB-5) is LOW, CA_2 (CB_2) is an interrupt input line similar to CA_1 (CB_1) (see *Table 4*). When CRA-5 (CRB-5) is HIGH, CA_2 (CB_2) becomes an output that may be used to control peripheral data transfers. When in the output mode, CA_2 and CB_2 have slightly different characteristics (see *Table 5* and *Table 6*).

Table 5 Control of CA_2 as an Output

CRA-5	CRA-4	CRA-3	CA_2 Cleared	CA_2 Set
1	0	0	LOW on the negative transition of E after an MPU read data register A operation.	HIGH when interrupt flag bit CRA-7 is set by an active transition of the CA_1 signal.
1	0	1	LOW on the negative transition of E after an MPU read data register A operation.	HIGH on the negative edge of the first E pulse that occurs while the device is deselected.
1	1	0	LOW when CRA-3 goes LOW as a result of an MPU write control register A operation.	Always LOW as long as CRA-3 is LOW. Goes HIGH on an MPU write control register A operation that changes CRA-3 to 1.
1	1	1	Always HIGH as long as CRA-3 is HIGH. Cleared on an MPU write control register A operation that clears CRA-3 to 0.	HIGH when CRA-3 goes HIGH as a result of an MPU write control register A operation.

Table 6 Control of CB_2 as an Output

CRB-5	CRB-4	CRB-3	CB_2 Cleared	CB_2 Set
1	0	0	LOW on the positive transition of the first E pulse following an MPU write data register B operation.	HIGH when interrupt flag bit CRB-7 is set by an active transition of the CB_1 signal.
1	0	1	LOW on the positive transition of the first E pulse after an MPU write data register B operation.	HIGH on the positive edge of the first E pulse following an E pulse that occurred while the device was deselected.
1	1	0	LOW when CRB-3 goes LOW as a result of an MPU write control register B operation.	Always LOW as long as CRB-3 is LOW. Goes HIGH on an MPU write control register B operation that changes CRB-3 to 1.
1	1	1	Always HIGH as long as CRB-3 is HIGH. Cleared when an MPU write control register B operation results in clearing CRB-3 to 0.	HIGH when CRB-3 goes HIGH as a result of an MPU write control register B operation.

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Absolute Maximum Ratings

Supply Voltage	-0.3 V, +7.0 V
Input Voltage	-0.3 V, +7.0 V
Operating Temperature — T_L to T_H	
F6821, F68A21, F68B21	0° C, +70° C
F6821C, F68A21C	-40° C, +85° C
F6821DM	-55° C, +125° C
Storage Temperature Range	-55° C, +150° C
Thermal Resistance	82.5° C/W

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
Bus Control Inputs (R/$\overline{W}$, $\overline{RESET}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$)						
V_{IH}	Input HIGH Voltage	V_{SS} + 2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	V_{SS} - 0.3		V_{SS} + 0.8	V	
I_{IN}	Input Leakage Current		1.0	2.5	μA	V_{IN} = 0 to 5.25 V
C_{IN}	Capacitance			7.5	pF	V_{IN} = 0, T_A = 25° C, f = 1.0 MHz
Interrupt Outputs ($\overline{IRQA}$, $\overline{IRQB}$)						
V_{OL}	Output LOW Voltage			V_{SS} + 0.4	V	I_{Load} = 3.2 mA
I_{LOH}	Output Leakage Current (OFF-State)		1.0	10	μA	V_{OH} = 2.4 V
C_{OUT}	Capacitance			5.0	pF	V_{IN} = 0, T_A = 25° C, f = 1.0 MHz
Data Bus (D_0-D_7)						
V_{IH}	Input HIGH Voltage	V_{SS} + 2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	V_{SS} - 0.3		V_{SS} + 0.8	V	
I_{TSI}	3-State (OFF-State) Input Current		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
V_{OH}	Output HIGH Voltage	V_{SS} + 2.4			V	I_{LOAD} = -205 μA
V_{OL}	Output LOW Voltage			V_{SS} + 0.4	V	I_{LOAD} = 1.6 mA
C_{IN}	Capacitance			12.5	pF	V_{IN} = 0, T_A = 25° C, f = 1.0 MHz
Peripheral Bus (PA_0-PA_7, PB_0-PB_7, CA_1, CA_2, CB_1, CB_2)						
I_{IN}	Input Leakage Current CA_1, CB_1		1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	3-State (OFF-State) Input Current PB_0-PB_7, CB_2		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
I_{IH}	Input HIGH Current PA_0-PA_7, CA_2	-200	-400		μA	V_{IH} = 2.4 V
I_{OH}	Darlington Dr. Curr. PB_0-PB_7, CB_2	-1.0		-10	mA	V_0 = 1.5 V
I_{IL}	Input LOW Current PA_0-PA_7, CA_2		-1.3	-2.4	mA	V_{IL} = 0.4 V
V_{OH}	Output HIGH Voltage PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 PA_0-PA_7, CA_2	 V_{SS} + 2.4 V_{CC} - 1.0			V	 I_{Load} = -200 μA I_{Load} = -10 μA
V_{OL}	Output LOW Voltage			V_{SS} + 0.4	V	I_{Load} = 3.2 mA
C_{IN}	Capacitance			10	pF	V_{IN} = 0, T_A = 25° C, f = 1.0 MHz
Power Requirements						
P_D	Power Dissipation			550	mW	

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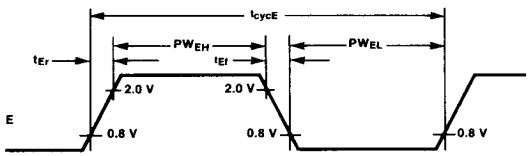
Enable Signal Timing Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	F6821		F68A21		F68B21		Unit	Figure
		Min	Max	Min	Max	Min	Max		
t_{cycE}	Enable Cycle Time	1000		666		500		ns	2
PW_{EH}	Enable Pulse Width, HIGH	450		280		220		ns	2
PW_{EL}	Enable Pulse Width, LOW	430		280		210		ns	2
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns	2

Fig. 2 Enable Signal Timing Characteristics



Bus Timing Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	F6821		F68A21		F68B21		Unit	Figures
		Min	Max	Min	Max	Min	Max		
t_{AS}	Set-Up Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	160		140		70		ns	3, 4
t_{AH}	Address Hold Time	10		10		10		ns	3, 4
t_{DDR}	Data Delay Time, Read		320		220		180	ns	3, 5
t_{DHR}	Data Hold Time, Read	10		10		10		ns	3, 5
t_{DSW}	Data Set-Up Time, Write	195		80		60		ns	4, 5
t_{DHW}	Data Hold Time, Write	10		10		10		ns	4, 5

Fig. 3 Bus Timing Characteristics (Read from PIA)

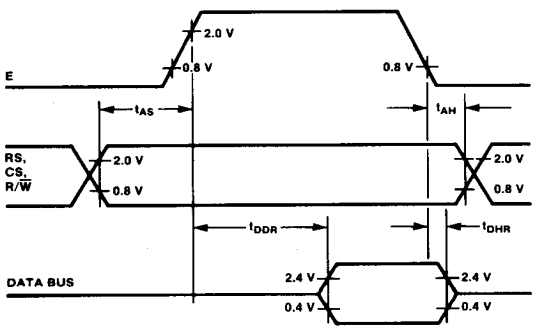
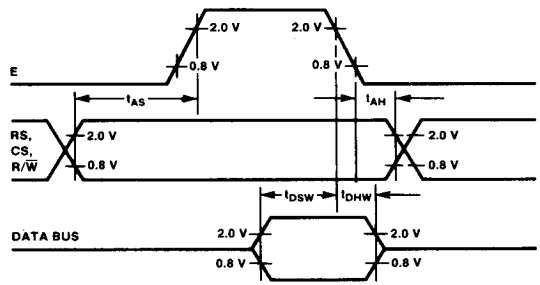


Fig. 4 Bus Timing Characteristics (Write to PIA)



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Peripheral Timing Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	F6821		F68A21		F68B21		Unit	Figures
		Min	Max	Min	Max	Min	Max		
t_{PDSU}	Peripheral Data Set-Up Time	200		135		100		ns	9
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns	9
t_{CA_2}	Delay Time, Enable Negative Transition to CA_2 Negative Transition		1.0		0.670		0.500	μs	6, 10, 11
t_{RS_1}	Delay Time, Enable Negative Transition to CA_2 Positive Transition		1.0		0.670		0.500	μs	6, 10
t_r, t_f	Rise and Fall for CA_1 and CA_2 Input Signals		1.0		1.0		1.0	μs	6, 11
t_{RS_2}	Delay Time from CA_1 Active Transition to CA_2 Positive Transition		2.0		1.35		1.0	μs	6, 11
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs	6, 12, 13
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA_0-PA_7, CA_2		2.0		1.35		1.0	μs	7, 12
t_{CB_2}	Delay Time, Enable Positive Transition to CB_2 Negative Transition		1.0		0.670		0.5	μs	6, 14, 15
t_{DC}	Delay Time, Peripheral Data Valid to CB_2 Negative Transition	20		20		20		ns	6, 13
t_{RS_1}	Delay Time, Enable Positive Transition to CB_2 Positive Transition		1.0		0.670		0.5	μs	6, 14
PW_{CT}	Peripheral Control Output Pulse Width, CA_2/CB_2	550		550		550		ns	6, 10, 14
t_r, t_f	Rise and Fall Time for CB_1 and CB_2 Input Signals		1.0		1.0		1.0	μs	15
t_{RS_2}	Delay Time, CB_1 Active Transition to CB_2 Positive Transition		2.0		1.35		1.0	μs	6, 15
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.60		1.10		0.85	μs	8, 17
t_{RS_3}	Interrupt Response Time		1.0		1.0		1.0	μs	8, 16
PW_I	Interrupt Input Pulse Width	500		500		500		ns	16
t_{RL}	Reset LOW Time*	1.0		0.66		0.5		μs	18

*The $\overline{RESET}$ line must be HIGH a minimum of 1.0 μs before addressing the PIA.

5

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Fig. 5 Bus Timing Test Load

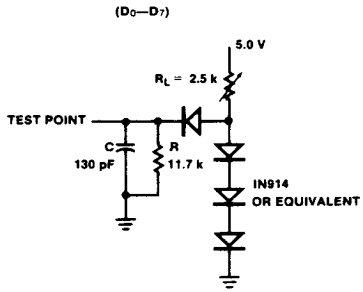
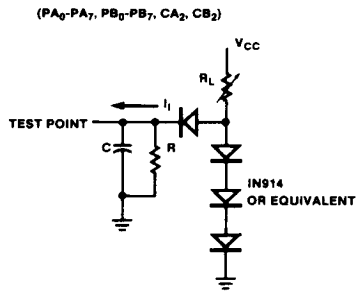


Fig. 6 TTL Equivalent Test Load



C = 40 pF, R = 12 k
Adjust R_L so that I_I = 3.2 mA
with V_I = 0.4 V and V_{CC} = 5.25 V

Fig. 7 CMOS Equivalent Test Load

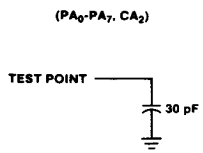


Fig. 8 NMOS Equivalent Test Load

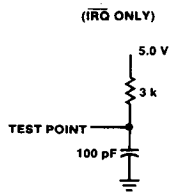


Fig. 9 Peripheral Data Set-Up and Hold Times (Read Mode)

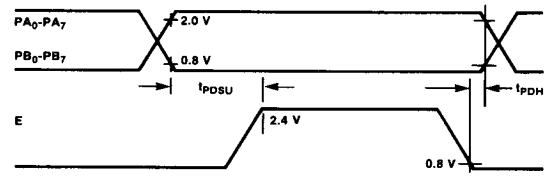
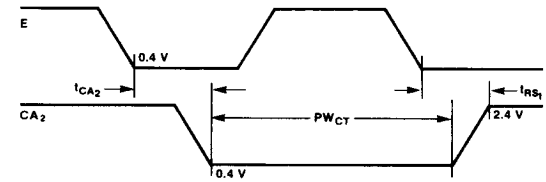


Fig. 10 CA_2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1; CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

Fig. 11 CA_2 Delay Time (Read Mode; CRA-5 = 1; CRA-3 = CRA-4 = 0)

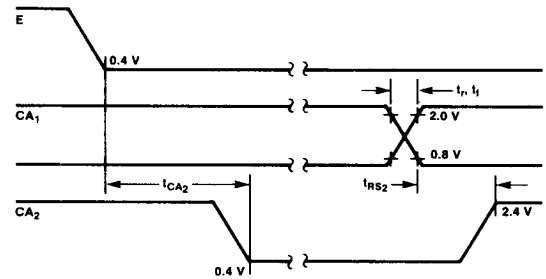


Fig. 12 Peripheral CMOS Data Delay Times (Write Mode; CRA-5 = CRA-3 = 1; CRA-4 = 0)

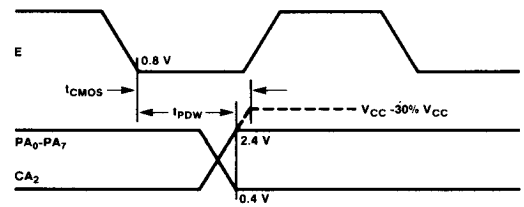


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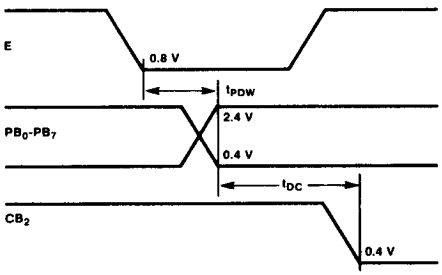
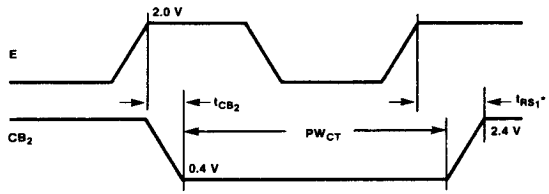
Fig. 13 Peripheral Data and CB_2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1; CRB-4 = 0)



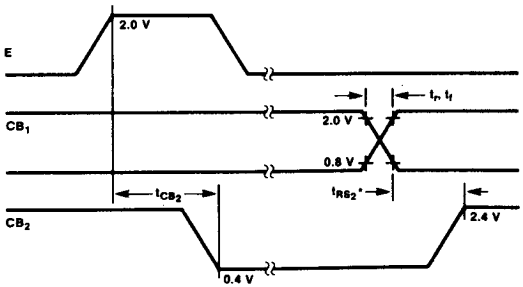
Note: CB_2 goes LOW as a result of the positive transition of the E pulse.

Fig. 14 CB_2 Delay Time (Write Mode; CRB-5 = CRB-3 = 1; CRB-4 = 0)



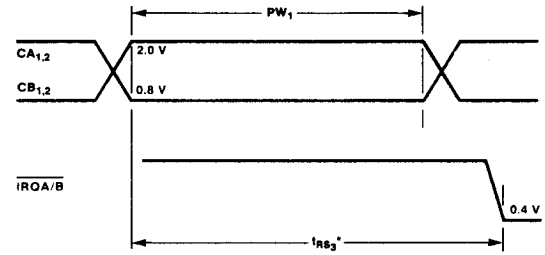
*Assumes part was deselected during the previous E pulse.

Fig. 15 CB_2 Delay Time (Write Mode; CRB-5 = 1; CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Fig. 16 Interrupt Pulse Width and $\overline{IRQ}$ Response



*Assumes interrupt enable bits are set.

Fig. 17 $\overline{IRQ}$ Release Time

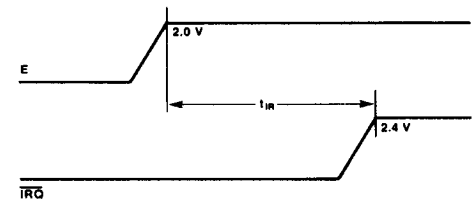
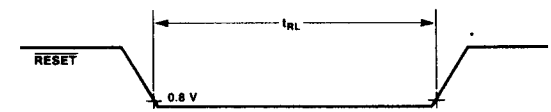


Fig. 18 $\overline{RESET}$ LOW Time



*The $\overline{RESET}$ line must be at V_{IH} for a minimum of 1.0 μs before addressing the PIA.

Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F6821P, S	0°C to +70°C
	F6821CP, CS	-40°C to +85°C
	F6821DM	-55°C to +125°C
1.5 MHz	F68A21P, S	0°C to +70°C
	F68A21CP, CS	-40°C to +85°C
2.0 MHz	F68B21P, S	0°C to +70°C
	F68B21DM (Waivers)	-55°C to +125°C

P = Plastic package, S = Ceramic package

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