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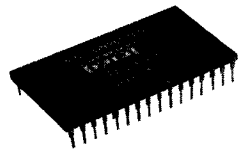


ADC80H*

AVAILABLE IN DIE FORM

***Not Recommended for New Designs. Use ADC80AG.**

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- PIN-COMPATIBLE WITH INDUSTRY STANDARD ADC80
- <600mW POWER DISSIPATION
- 15μsec CONVERSION TIME WITH EXTERNAL CLOCK
- 25μSEC MAXIMUM CONVERSION TIME
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES −25°C TO +85°C
- PARALLEL AND SERIAL OUTPUTS
- 32-PIN HERMETIC PACKAGE

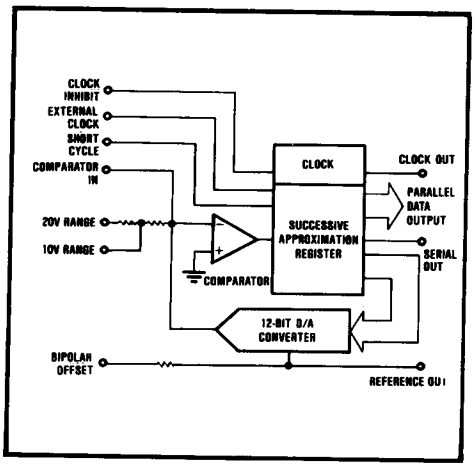
DESCRIPTION

The ADC80H is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). Like the industry standard ADC80, the ADC80H is completely specified for −25°C to +85°C operation.

The maximum conversion time of 25μsec makes the ADC80H ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80H may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80H operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike other ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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PDS-577B

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

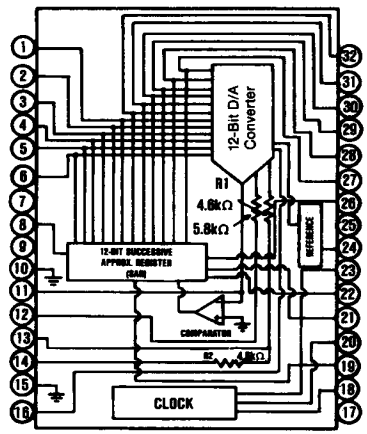
MODEL	ADC80H-AH-12			UNITS
	MIN	TYP	MAX	
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V		2.3		kΩ
0 to +10V, +5V		4.6		kΩ
±10V		9.2		kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			−150	µA
I_{IL} (V_{IN} =+0.4V)			500	µA
Convert Command Pulse Width[1]	100		2000	nsec
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0.1	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error			±3/4	LSB
Inherent Quantization Error		1/2		LSB
POWER SUPPLY SENSITIVITY				
+13.5V ≤ +V_{CC} ≤ +16.5V or +11.4V ≤ +V_{CC} ≤ +12.6V		±0.003	±0.009	% of FSR/%V_{CC}
−16.5V ≤ −V_{CC} ≤ −13.5V or −12.6V ≤ −V_{CC} ≤ −11.4V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]	15	22	25	µsec
OUTPUT				
DIGITAL(Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels: Logic 0 (I_{sink} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{source} ≤ 80µA)	+2.4V			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.2	+6.3	+6.4	
Source Current Available for External Loads[8]	200			µA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Voltage, ±V_{CC}	±11.4	±15	±16.5	V
V_{DD}	+4.5	+5.0	+5.5	V
Current, +I_{CC}		5	8.5	mA
−I_{CC}		21	26	mA
I_{DD}		11	15	mA
Power Dissipation (±V_{CC} = 15V)		450	595	mW
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Storage	−65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100nsec; however, it must be limited to 2μsec (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means non-return-to-zero coding. (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification.

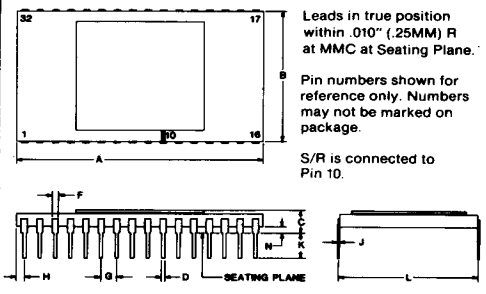
CONNECTION DIAGRAM

Pin 1 - Bit 6	Pin 32 - Bit 7
Pin 2 - Bit 5	Pin 31 - Bit 8
Pin 3 - Bit 4	Pin 30 - Bit 9
Pin 4 - Bit 3	Pin 29 - Bit 10
Pin 5 - Bit 2	Pin 28 - Bit 11
Pin 6 - Bit 1(MSB)	Pin 27 - Bit 12 (LSB)
Pin 7 - N/C	Pin 26 - Serial Out
Pin 8 - Bit 1 (MSB)	Pin 25 - $-V_{CC}$
Pin 9 - +5V Digital Supply	Pin 24 - Ref. Out (+6.3V)
Pin 10 - Digital Common	Pin 23 - Clock Out
Pin 11 - Comparator In	Pin 22 - Status
Pin 12 - Bipolar Offset	Pin 21 - Short Cycle
Pin 13 - R1 10V Range	Pin 20 - Clock Inhibit
Pin 14 - R2 20V Range	Pin 19 - External Clock
Pin 15 - Analog Common	Pin 18 - Convert Command
Pin 16 - Gain Adjust	Pin 17 - $+V_{CC}$

TOP VIEW



MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.136	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

CASE: Ceramic, hermetic
MATING CONNECTOR: 2302MC
WEIGHT: 7.3gm (0.26oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to −16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	−0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation	1000mW
Lead Temperature, Soldering	+300°C, 10sec
Thermal Resistance, θ_{JA}	60°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

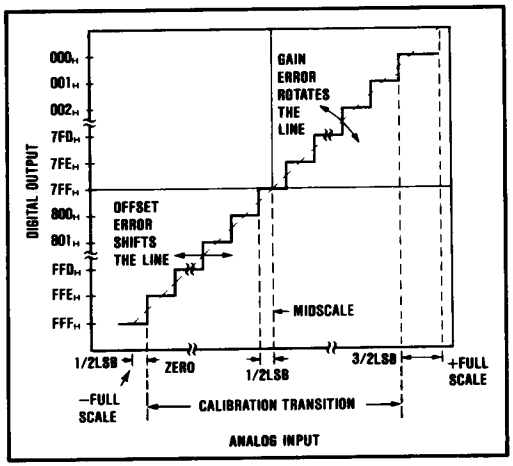


FIGURE 1. ADC80H Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80H analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80H input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80H is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80H connected for uniplolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80H follows this convention. Thus, bipolar offset error for the ADC80H is

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	FSR/2ⁿ n = 8 n = 10 n = 12	20V/2ⁿ 78.13mV 19.53mV 4.88mV	10V/2ⁿ 39.06mV 9.77mV 2.44mV	5V/2ⁿ 19.53mV 4.88mV 1.22mV	10V/2ⁿ 39.06mV 9.77mV 2.44mV	5V/2ⁿ 19.53mV 4.88mV 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	 +Full Scale Mid Scale –Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 + 10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB + 2.5V 0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary

defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

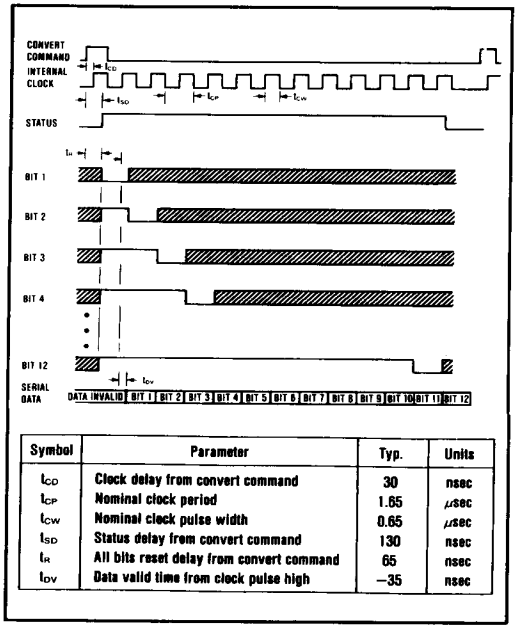
Electrical specifications for the ADC80H assume the application of the rated power supply voltages of+5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80H are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 2μsec to obtain the specified conversion time with internal clock, the ADC80H will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50nsec after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.65	μsec
t_{CW}	Nominal clock pulse width	0.65	μsec
t_{SD}	Status delay from convert command	130	nsec
t_R	All bits reset delay from convert command	65	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC80H Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80H parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80H; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80H have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80H, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80H as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80H will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80H offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by the decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80H Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

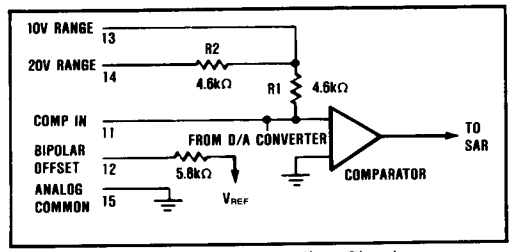


FIGURE 3. ADC80H Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80H as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These

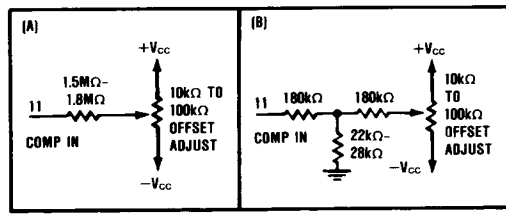


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

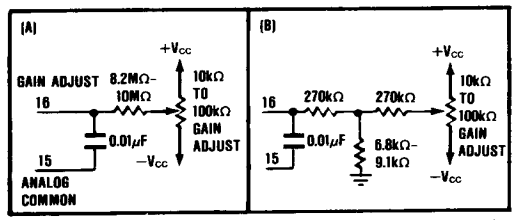


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC80H is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μsec (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80H. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applica-

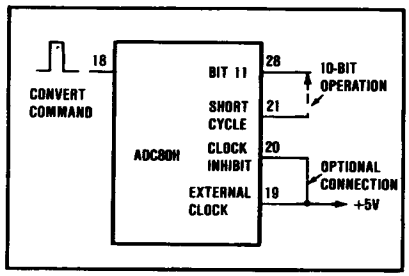


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

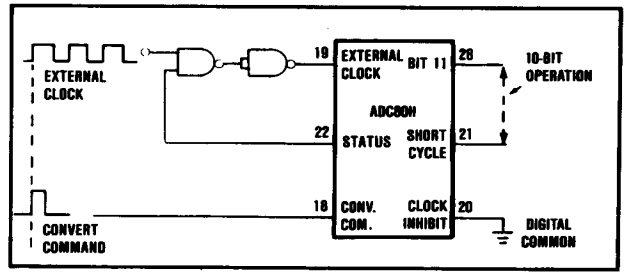


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

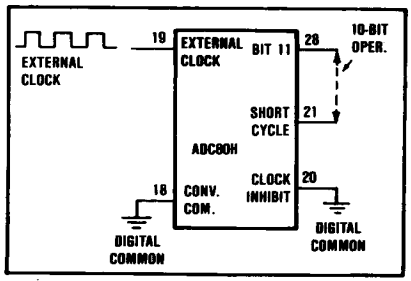


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

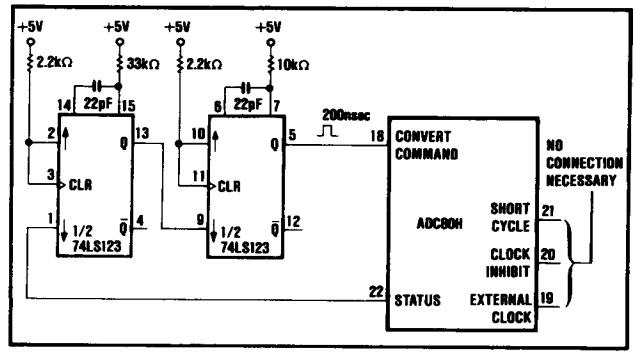


FIGURE 9. Continuous Conversion with 600nsec between Conversions. (Circuit insures that conversion will start when power is applied.)

tions not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80H is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80H.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μsec)	25	22	18
Minimum Conversion Time[1] External Clock (μsec)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80H-AH-12Q

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	