
HD74HC393

Dual 4-bit Binary Counters

HITACHI

Description

The HD74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

The HD74HC393 is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. when clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

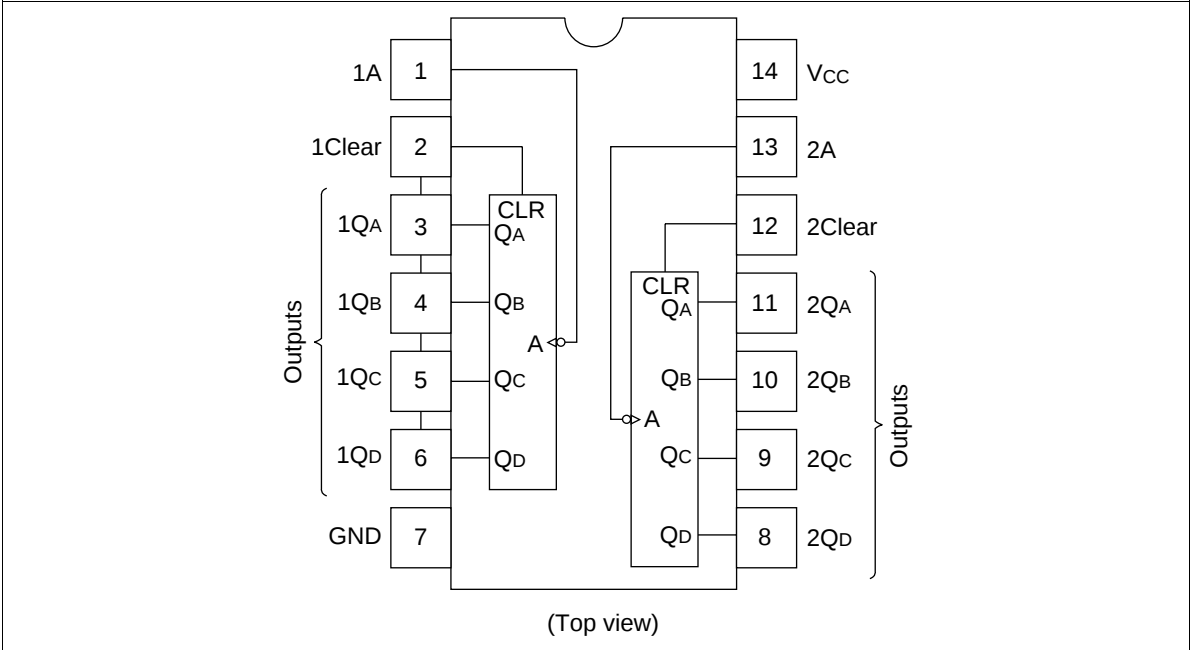
Features

- High Speed Operation: t_{pd} (A to Q_A) = 16 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

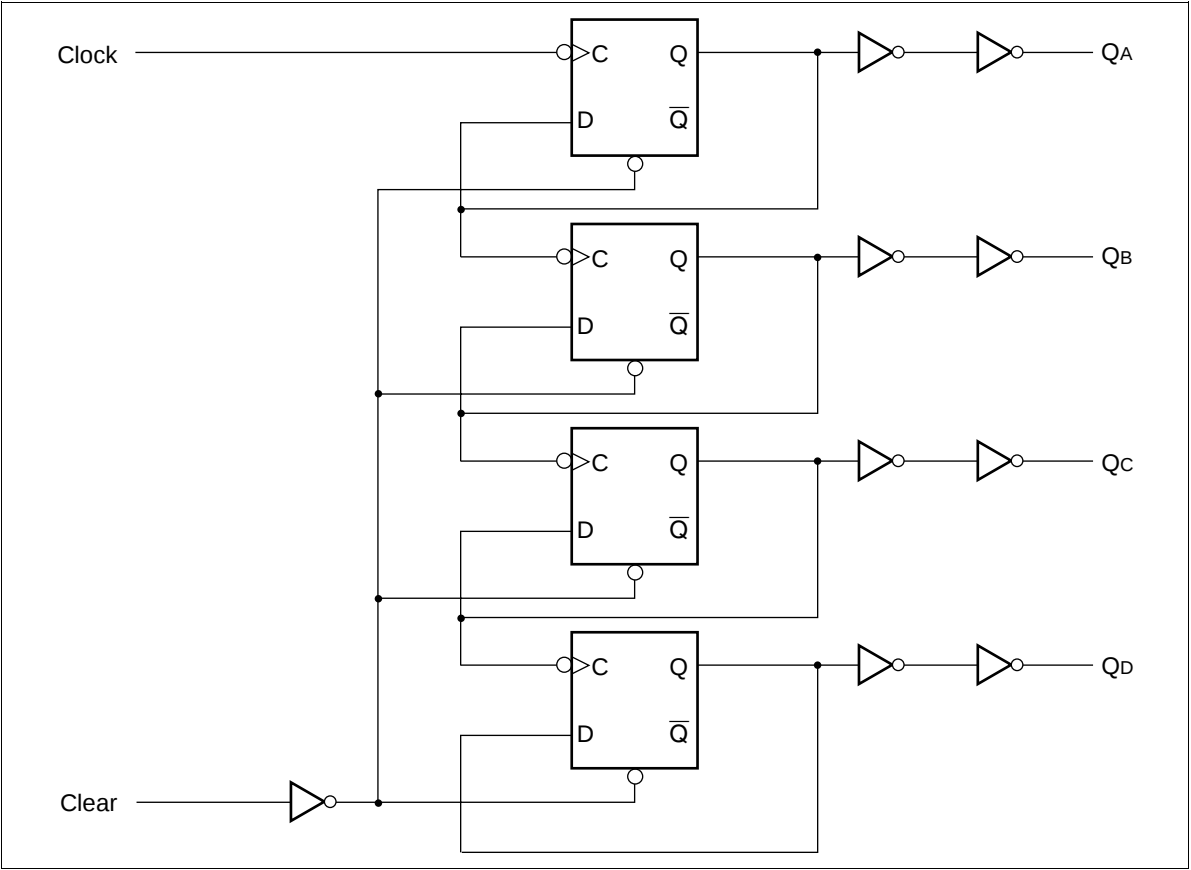
Function Table

Clock	Clear	Outputs
X	H	L
H	L	No change
L	L	No change
	L	No change
	L	Advance to next state

Pin Arrangement



Block Diagram (1/2)

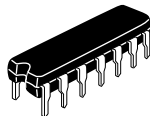
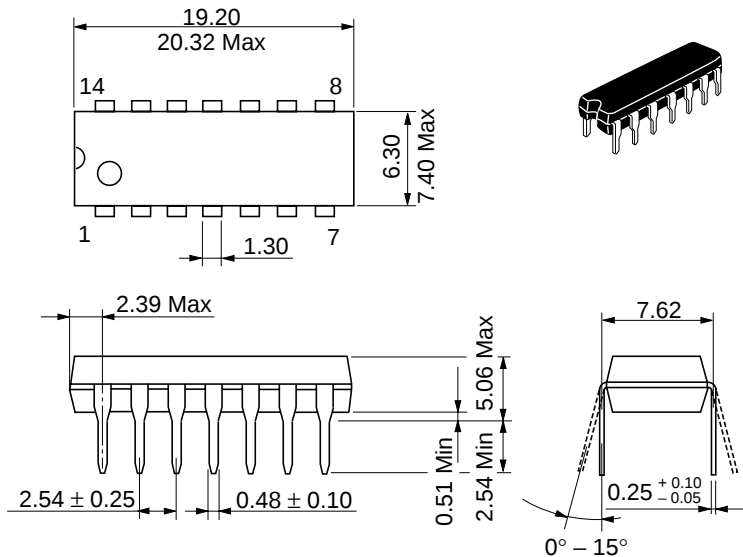


DC Characteristics

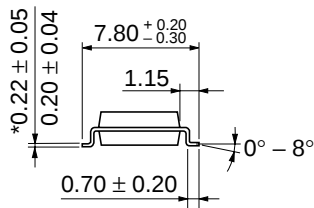
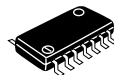
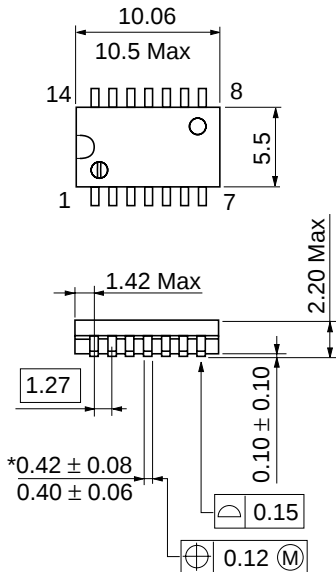
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		
		6.0	5.68	—	—	5.63	—		
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		
		6.0	—	—	0.26	—	0.33		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	120	—	150	ns	Clock to Q_A
		4.5	—	16	24	—	30		
		6.0	—	—	20	—	26		
	t_{PHL}	2.0	—	—	185	—	230	ns	Clock to Q_B
		4.5	—	20	37	—	46		
		6.0	—	—	31	—	39		
	t_{PLH}	2.0	—	—	220	—	275	ns	Clock to Q_C
		4.5	—	24	44	—	55		
		6.0	—	—	37	—	47		
	t_{PHL}	2.0	—	—	260	—	325	ns	Clock to Q_D
		4.5	—	28	52	—	65		
		6.0	—	—	44	—	55		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q_A, Q_B, Q_C, Q_D
		4.5	—	21	30	—	38		
		6.0	—	—	28	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, clear
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_h	2.0	50	—	—	65	—	ns	Clear to clock
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

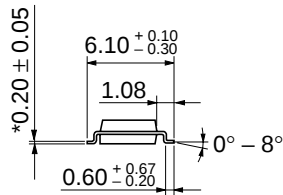
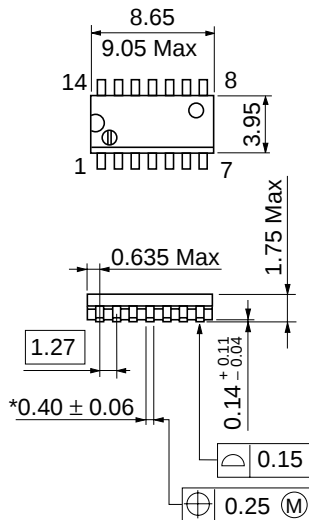


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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