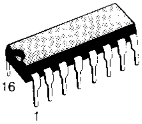
DUAL 1-OF-4 DECODER/DEMULTIPLEXER

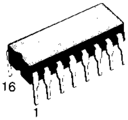
DESCRIPTION

The TTL/MSI T54LS155/T74LS155 and T54LS156/T74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one input of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

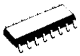
The LS155 and LS156 are fabricated withe the Schottky barrier diode process for high speed and are completely compatible with all SGS TTL families.



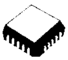
B1
Plastic Package



D1/D2
Ceramic Package



M1
Micro Package



C1
Plastic Chip Carrier

ORDERING NUMBERS:
T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

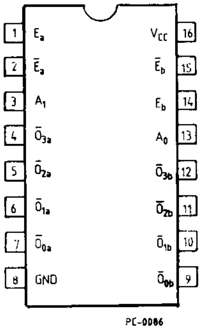
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTIONAL CAPABILITY
- COMMON ADDRESS INPUTS
- TRUE OR COMPLEMENT DATA DEMULTIPLEXING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

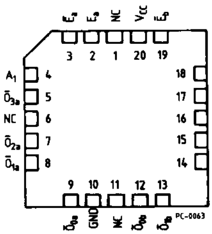
A_0-A_1	Address Inputs
$\overline{E}_a$-$\overline{E}_b$	Enable (Active LOW) Inputs
E_a	Enable (Active HIGH) Input
$\overline{O}_0$-$\overline{O}_3$	Active LOW Outputs

PIN CONNECTION
(top view)

DUAL IN LINE

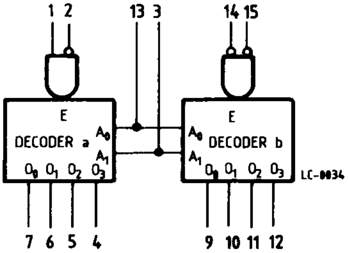


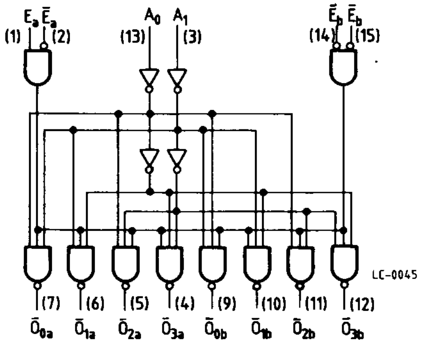
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
V_{CC}		Supply Voltage	−0.5 to 7	V
V_I	155	Input Voltage, Applied to Input	−0.5 to 15	V
	156		−1.5 to 5.5	
V_O		Output Voltage, Applied to Output	−0.5 to 10	V
I_I		Input Current, Into Inputs	−30 to 5	mA
I_O		Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS155/156D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS155/156XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs (O_0-O_3). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

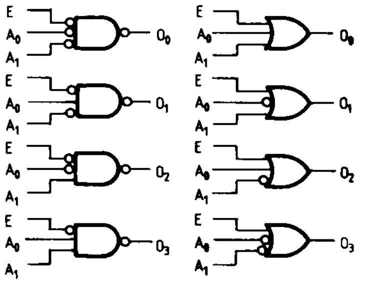
Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($\overline{E}_a \bullet \overline{E}_a$). In demultiplexing applications, Decoder "a" can accepts either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \bullet \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying $\overline{E}_a$ to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ to $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are used in some applications replacing multiple gate functions as shown in Fig. 1. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \bullet (E + \overline{A}_0 + A_1) \bullet (E + A_0 + \overline{A}_1) \bullet (E + \overline{A}_0 + \overline{A}_1)$$

$$\text{where } E = E_a + \overline{E}_a;\ E = E_b + \overline{E}_b$$

Fig. 1



TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUPTUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Treshold Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Treshold Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			− 0.65	− 1.5	$V_{CC} = MIN, I_{IN} = -18mA$		V
V_{OH}	Output HIGH Voltage LS155 Only	54	2.5	3.4		$V_{CC} = MIN, I_{OH} = -400\mu A, V_{IN} = V_{IH}$ or V_{IL} per Truth Table		V
		74	2.7	3.4				
I_{OH}	Output HIGH Current LS156 Only				100	$V_{CC} = MIN, V_{OH} = 5.5V, V_{IN} = V_{IH}$ or V_{IL} per Truth Table		μA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	$I_{OL} = 4.0mA$	$V_{CC} = MIN$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
		74		0.35	0.5	$I_{OL} = 8.0mA$		
I_{IH}	Input HIGH Current				20 0.1	$V_{CC} = MAX$, $V_{IN} = 2.7V$ $V_{CC} = MAX$, $V_{IN} = 7.0V$		μA mA
I_{IL}	Input LOW Current				− 0.4	$V_{CC} = MAX$, $V_{IN} = 0.4V$		mA
I_{OS}	Output Short Circuit Current (Note 2)		− 20		− 100	$V_{CC} = MAX$, $V_{OUT} = 0V$		mA
I_{CC}	Power Supply Current			6.0	10	$V_{CC} = MAX$		mA

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits				Test Conditions		Units
		LS155		LS156				
		Typ.	Max.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	17 19	26 30	31 34	46 51	Fig. 2	$V_{CC} = 5.0V$ $C_L = 15pF$ $R_L = 2k\Omega$ (Only LS156)	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	10 19	15 30	25 34	40 51	Fig. 3		ns
t_{PLH} t_{PHL}	Propagation Delay, E_a to Output	18 18	27 27	32 32	48 48	Fig. 2		ns

Notes:

1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$

AC WAVEFORMS

Fig. 2

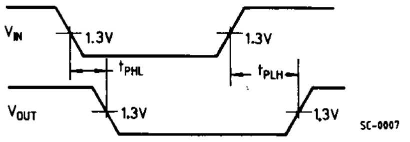
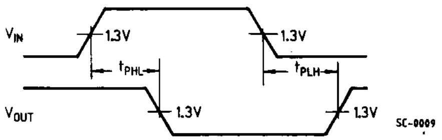
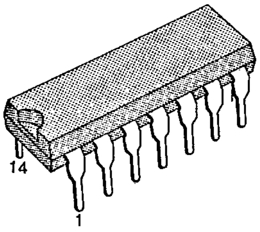
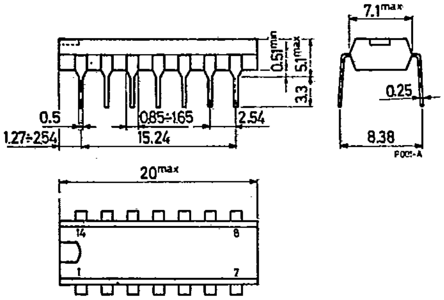


Fig. 3

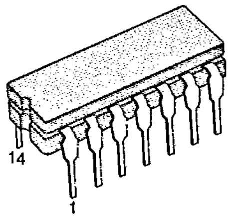


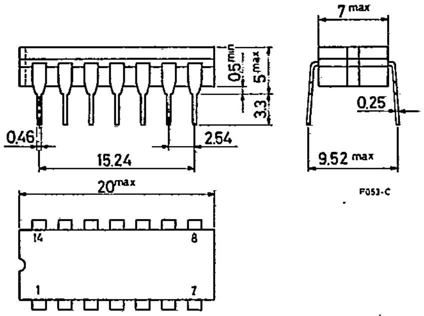
14-LEAD PLASTIC DIP



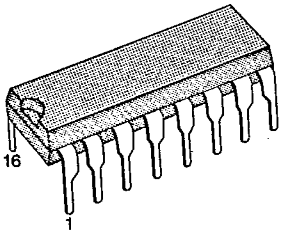


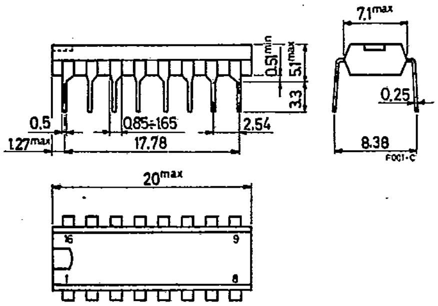
14-LEAD CERAMIC DIP





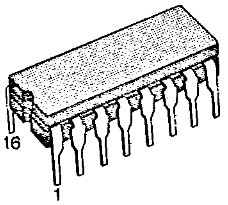
16-LEAD PLASTIC DIP

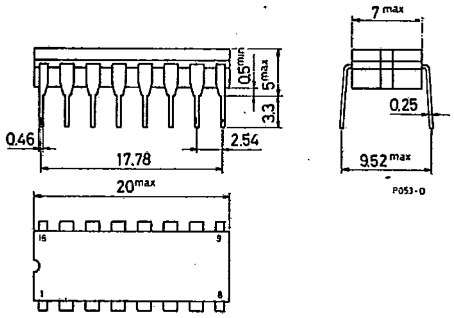




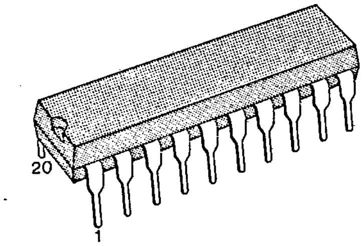
Packages

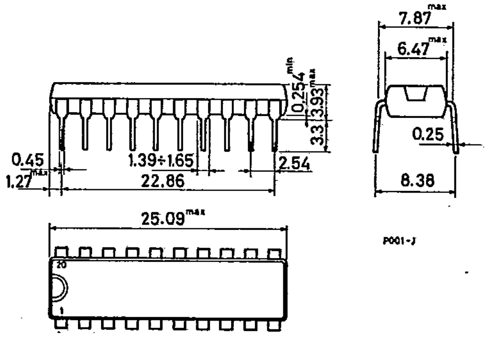
16-LEAD CERAMIC DIP





20-LEAD PLASTIC DIP





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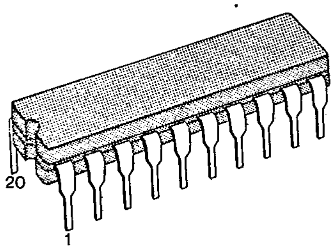
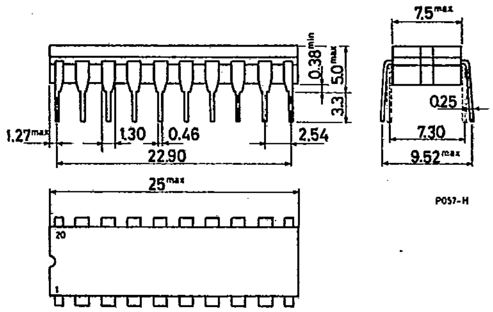
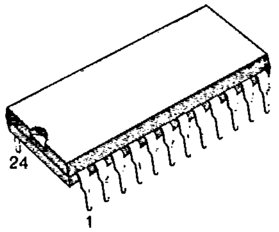
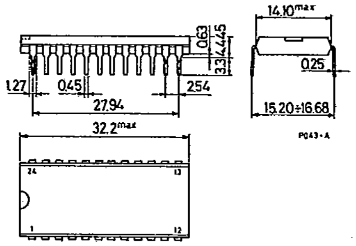




Packages

24-LEAD PLASTIC DIP





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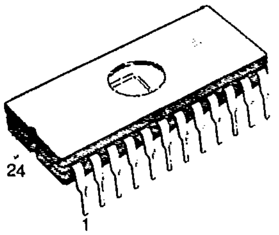
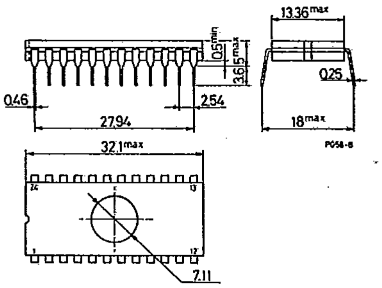
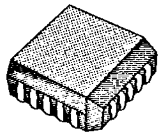
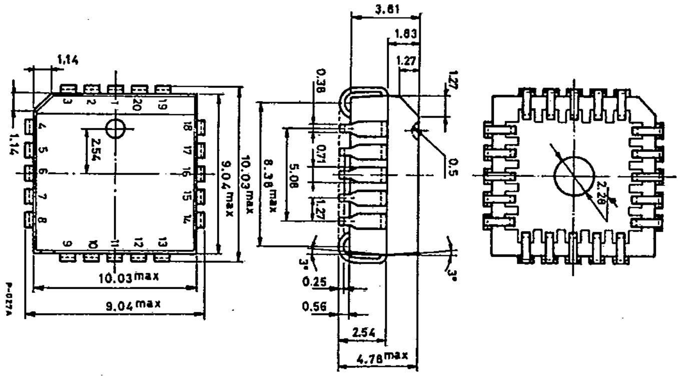




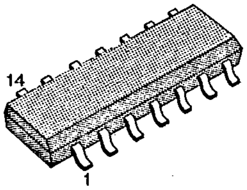
CHIP CARRIER 20 LEAD PLASTIC

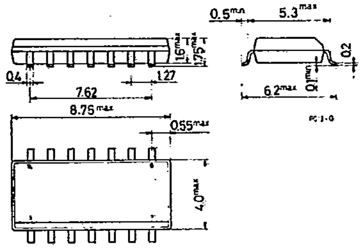




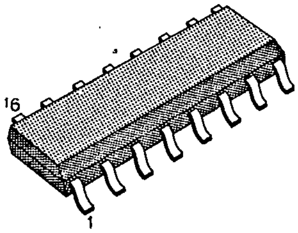
Packages

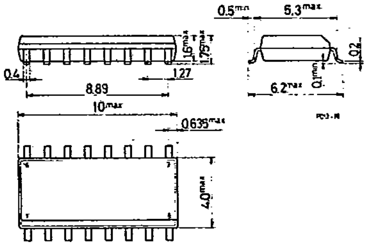
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.