2

Features

- Fast Read Access Time 45ns
- · Fast Byte Write 1ms
- Self-Timed Byte Write Cycle Internal Address and Data Latches Internal Control Timer
 Automatic Clear Before Write
- Direct Microprocessor Control
 DATA POLLING
- Low Power

80mA Active Current

500µA CMOS Standby Current (28HC16L)

High Reliability CMOS Technology

Endurance: 10⁴ cycles Data Retention: 10 years

- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDÉC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

The AT28HC16/16L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. The device is optimized for high speed applications, featuring access times to 45ns. Its 16k of memory is organized as 2,048 words by 8 bits. The AT28HC16/16L comes in a space saving 24 pin DIP.

The AT28HC16/16L is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device being written will go to a busy state and automatically clear and write the latched data using an internal control timer. Data polling of I/O7 may be used to detect the end of the write cycle. Once a write cycle has been completed, a new access for a read or a write may begin immediately.

Atmel's high-speed CMOS technology is used to achieve access times of 45ns for the AT28HC16 with under 440mW of power dissipation. The AT28HC16L offers ultra low standby power consumption of under 2.75mW at access time to 55ns.

The AT28HC16/16L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and for improved data retention characteristics. An extra 16 bytes of E²PROM are available for device identification or tracking.

Pin Configurations

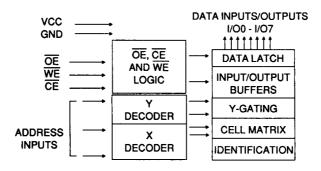
A7 G A6 G A5 G A4 G A3 G A1 G A0 G I/O1 G I/O2 G I/O2 G GND G	5 6 7 8 9 10 11	~	24 23 22 21 20 19 18 17 16 15 14	ممممممعمم	VCC A8 A9 WE 0E 1/07 1/06 1/05 1/04
GND =			13	Ĕ	1/03
GND -	12		13	P	1/03

Pin Name	Function
A0 - A10	Addresses
CE	Chip Enable
ŌĒ	Output Enable
WE	Write Enable
1/00 - 1/07	Data Inputs/Outputs
NC	No Connect

16K (2K x 8) High Speed CMOS E²PROM



Block Diagram



Operating Modes

<u> </u>				
Mode	CE	ŌĒ	WE	1/0
Read	VIL	VIL	ViH	Dout
Write ⁽²⁾	VIL	ViH	VIL	DiN
Standby/Write Inhibit	ViH	X ⁽¹⁾	х	High Z
Write Inhibit	X	X	ViH	
Write Inhibit	X	VIL	X	
Output Disable	X	ViH	Х	High Z
Chip Erase	VIL	V _H ⁽³⁾	ViL	High Z

Notes: 1. X can be VIL or VIH.

3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28HC16/16L is accessed like a Static RAM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever CE or OE is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28HC16/16L is similar to writing into a Static RAM. A low pulse on the WE or CE input with OE high and CE or WE low (respectively) initiates a byte write. The address location is latched on the last falling edge of WE (or CE); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

DATA POLLING: The AT28HC16/16L provides DATA POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) Vcc sense—if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay—once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit—holding any one of OE low, CE high or WE high inhibits byte write cycles. (d) Noise Protection—a WE or CE pulse of less than 10ns (typical) will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC16/16L may be set to the high state by the CHIP CLEAR operation. By setting \overline{CE} low and \overline{OE} to 12 volts, the chip is cleared when a 10 msec low pulse is applied to \overline{WE} .

DEVICE IDENTIFICATION: In the AT28HC16/16L there are an extra 16 bytes of E²PROM memory available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7F0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

^{2.} Refer to A.C. Programming Waveforms.

Absolute Maximum Ratings*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground0.6V to +6.25V
All Output Voltages with Respect to Ground0.6V to Vcc +0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28HC16-45	AT28HC16L-55	AT28HC16-55	AT28HC16-70 AT28HC16L-70	AT28HC16-90 AT28HC16L-90
Operating	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
Temperature	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
(Case)	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power St	pply	5V±10%	5V±10%	5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
ILI	Input Load Current	VIN=0V to VCC + 1V		,	10	μΑ
llo	Output Leakage Current	V _{I/O} =0V to V _C C			10	μА
ISB1	Vcc Standby Current CMOS	CE=Vcc-0.3V to Vcc + 1.0V	(AT28HC16L)		500	μA
ISB2 Vcc Standby Current TTL		CE=2.0V to Vcc + 1.0V	AT28HC16L		3	mA
		CE=2.0V 10 VCC + 1.0V	AT28HC16		60	mA
lcc	Vcc Active Current A.C.	f=10MHz; lout=0mA			80	mA
VIL	Input Low Voltage			,	0.8	٧
ViH	Input High Voltage			2.0		V
VoL	Output Low Voltage	I _{OL} =12mA			.4	٧
Voн	Output High Voltage	I _{OH} =-4.0mA		2.4		٧

Pin Capacitance (f=1MHz T=25°C) (5)

	Тур	Max	Units	Conditions
Cin	4	6	pF	VIN = 0V
Соит	8	12	pF	Vout = 0V

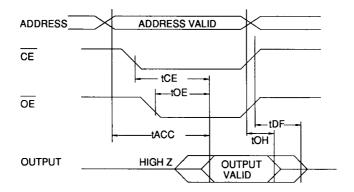




A.C. Read Characteristics (1)

			HC16 15		3HC16 55		HC16L 55		3HC16 70		HC16L 70	-	HC16L 90	
Symbol	Parameter	Min	Мах	Min	Мах	Min	Мах	Min	Max	Min	Мах	Min	Max	Units
tacc	Address to Output Delay		45		55		55		70		70		90	ns
toE (2)	CE to Output Delay		30		40		55		50		70		90	ns
toe (3)	OE to Output Delay	0	30	0	40	0	40	0	50	0	50	0	50	ns
t _{DF} (4,5)	OE to Output Float	0	30	0	40	0	40	0	50	0	50	0	50	ns
tон	Output Hold from OE or Address, whichever occurred first	0		0		0		0		0		0		ns

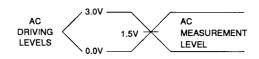
A.C. Read Waveforms



Notes:

- 1. $C_L = 30pF$.
- \overline{CE} may be delayed up to tACC tCE after the address transition without impact on tACC.
- OE may be delayed up to tCE tOE after the falling edge of CE without impact on tCE or by tACC - tOE after an address change without impact on tACC.
- 4. t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first (CL = 5pF).
- 5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



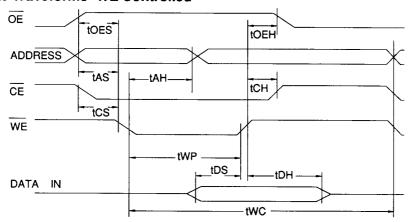
 t_R , $t_F < 5 ns$

Output Test Load

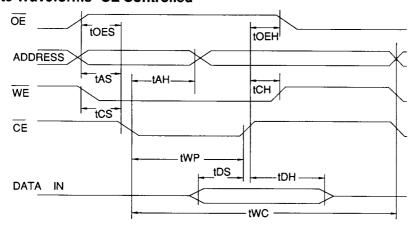
A.C. Write Characteristics

Symbol	Parameter	Min	Тур	Max	Units
tas, toes	Address, OE Set-up Time	0			ns
tah	Address Hold Time	50			ns
twp	Write Pulse Width	100		1000	ns
tos	Data Set-up Time	50			ns
tDH,tOEH	Data, OE Hold Time	0			ns
twc	Write Cycle Time		0.5	1.0	ms

A.C. Write Waveforms- WE Controlled



A.C. Write Waveforms- **CE** Controlled





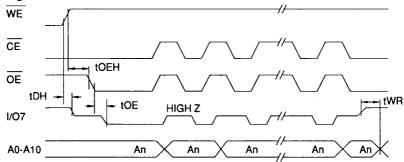


Data Polling Characteristics (1)

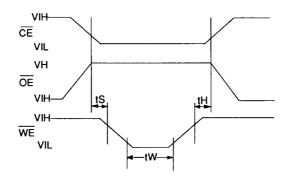
Symbol	Parameter	Min	Тур	Max	Units
ton	Data Hold Time	0			ns
t OEH	OE Hold Time	0			ns
toe	OE to Output Delay			100	ns
twn	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms



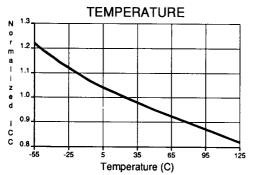
Chip Erase Waveforms



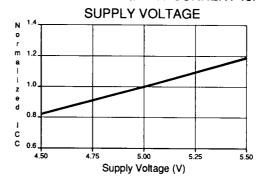
 $t_S = t_H = 1 \mu sec \text{ (min.)}$ $t_W = 10 m sec \text{ (min.)}$ $V_H = 12.0 V \pm 0.5 V$

2

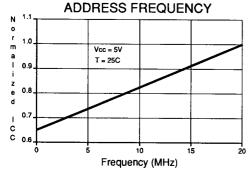
NORMALIZED SUPPLY CURRENT vs.



NORMALIZED SUPPLY CURRENT vs.



NORMALIZED SUPPLY CURRENT vs.





tacc	Icc	(mA)			
(ns)	Active	Standby	Ordering Code	Package	Operation Range
45	45 80 60	AT28HC16N-45DC AT28HC16-45DC AT28HC16N-45PC AT28HC16-45PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)	
			AT28HC16N-45DI AT28HC16-45DI AT28HC16N-45PI AT28HC16-45PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
55	80	60	AT28HC16N-55DC AT28HC16-55DC AT28HC16N-55PC AT28HC16-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-55DI AT28HC16-55DI AT28HC16N-55PI AT28HC16-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
	:		AT28HC16N-55DM AT28HC16-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-55DM/883 AT28HC16-55DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
70	80	60	AT28HC16N-70DC AT28HC16-70DC AT28HC16N-70PC AT28HC16-70PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-70DI AT28HC16-70DI AT28HC16N-70PI AT28HC16-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16N-70DM AT28HC16-70DM	24D3 24D6	Military (-55°C to 125°C)
	:		AT28HC16N-70DM/883 AT28HC16-70DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
90	80	60	AT28HC16N-90DC AT28HC16-90DC AT28HC16N-90PC AT28HC16-90PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-90DI AT28HC16-90DI AT28HC16N-90PI AT28HC16-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)

tacc			Ordorina Codo	Dashasa	Operation Pange		
(ns)	Active	Standby	Ordering Code	Package	Operation Range		
90	90 80 60		AT28HC16N-90DM AT28HC16-90DM	24D3 24D6	Military (-55°C to 125°C)		
			AT28HC16N-90DM/883 AT28HC16-90DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)		

Package Type					
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)				
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)				
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)				
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)				





tacc	Icc (mA)				
(ns)	Active	Standby	Ordering Code	Package	Operation Range
55	80	0.5	AT28HC16LN-55DC AT28HC16L-55DC AT28HC16LN-55PC AT28HC16L-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16LN-55DI AT28HC16L-55DI AT28HC16LN-55PI AT28HC16L-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-55DM AT28HC16L-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-55DM/883 AT28HC16L-55DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
70	80	0.5	AT28HC16LN-70DC AT28HC16L-70DC AT28HC16LN-70PC AT28HC16L-70PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16LN-70DI AT28HC16L-70DI AT28HC16LN-70PI AT28HC16L-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-70DM AT28HC16L-70DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-70DM/883 AT28HC16L-70DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
90	80	30 0.5	AT28HC16LN-90DC AT28HC16L-90DC AT28HC16LN-90PC AT28HC16L-90PC AT28HC16L-W	24D3 24D6 24P3 24P6 DIE	Commercial (0°C to 70°C)
			AT28HC16LN-90DI AT28HC16L-90DI AT28HC16LN-90PI AT28HC16L-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-90DM AT28HC16L-90DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-90DM/883 AT28HC16L-90DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)

Package Type				
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)			
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)			
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)			
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)			
w	Die			

