FM1208S FRAM® Memory

4,096-Bit Nonvolatile Ferroelectric RAM
Product Specification

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Features

- 4,096 Bit Bytewide Nonvolatile Ferroelectric RAM
  Organized as 512 x 8
- CMOS Technology with Integrated Ferroelectric Storage Cells
- Fully Synchronous Operation
  - 200ns Read Access
  - 400ns Read/Write Cycle Time
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
- On Chip Data Protection Circuit
- 10 Year Data Retention without Power
- Single 5 Volt ±10% Supply
- Low Power Consumption
  - Active Current: 10mA
  - Standby Current: 100µA
- CMOS/TTL Compatible I/O Pins
- 24 Pin DIP and SOP Packages
- 0-70°C Ambient Operating Temperature Range

Description

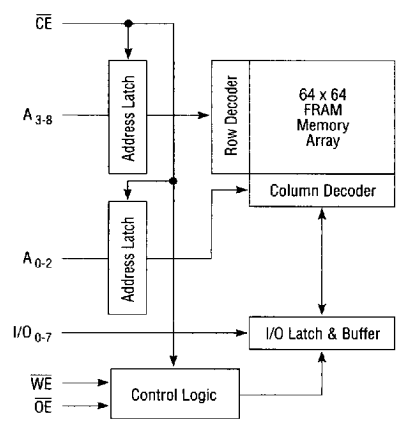
The FM1208S is a bytewide ferroelectric RAM, or FRAM® product, organized as 512 x 8. FRAM memory products from Ramtron combine the read/write characteristics of semiconductor RAM with the nonvolatile retention of magnetic storage.

This product is manufactured in a CMOS technology with the addition of integrated thin film ferroelectric storage cells developed and patented by Ramtron.

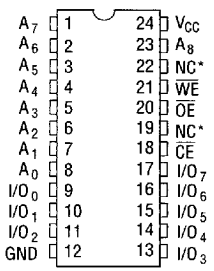
The ferroelectric cells are polarized on each read or write cycle, therefore no special store or recall sequence is required. The memory is always static and nonvolatile.

Ramtron's FRAM products operate from a single +5 volt power supply and are TTL/CMOS compatible on all inputs and outputs. The FM1208S utilizes the JEDEC standard bytewide SRAM pinout, but differ slightly in operation due to the integrated address latch.

Functional Diagram



Pin Configuration



* Must be Unconnected or Tied to GND

Device Operation

Read Operation

When $\overline{CE}$ is low and $\overline{WE}$ is high, a read operation is performed by the FRAM memory. On the falling edge of $\overline{CE}$, all address bits (A_0 - A_8) are latched into the part and the cycle is started. Data will appear on the output pins a maximum access time (t_{CA}) after the beginning of the cycle.

The designer should ensure that there are no address transitions from t_{AS} (setup time) before the falling edge of $\overline{CE}$ to t_{AH} (hold time) after it. After t_{AH}, the address pins are ignored for the remainder of the cycle. It is equally important that $\overline{CE}$ be generated such that unwanted glitches or pulses, of any duration, be prevented.

After the read has completed, $\overline{CE}$ should be brought high for the precharge interval (t_{PC}). During this period data is restored in the internal memory cells and the chip is prepared for the next read or write. FRAM memories will not operate in systems in which CE does not toggle with every access.

The $\overline{OE}$ pin may be used to avoid bus conflicts on the system bus. Only when both $\overline{CE}$ and $\overline{OE}$ are low will the FRAM memory drive its outputs. Under all other circumstances, the output drivers are held in a high impedance (High-Z) condition. Note that the internal read operation is performed regardless of the state of the $\overline{OE}$ pin.

Write Operation

When CE falls while $\overline{WE}$ is low, or $\overline{WE}$ falls while $\overline{CE}$ is low, a write operation will be performed by the FRAM memory. On the falling edge of $\overline{CE}$, as in the read cycle, the address will be latched into the part with the same setup and hold requirements. As in the read cycle, $\overline{CE}$ must be held high for a precharge interval (t_{PC}) between each access.

Data is latched into the part on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Write operations take place regardless of the state of $\overline{OE}$, however, it may need to be driven high by the system at the beginning of the cycle in order to avoid bus conflicts.

There is no long internal write delay after a write operation. Data is immediately nonvolatile and power may be removed from the part upon completion of the precharge interval following the write.

Low Voltage Protection

When V_{CC} is below 3.5V (typical), all read and write operations to the part will be ignored. For systems in which unwanted signal transitions would otherwise occur on the $\overline{CE}$ pin at or above this voltage, $\overline{CE}$ should be held high with a power supply monitor circuit.

Whenever V_{CC} rises above 3.5V, either after power up or a brownout, no read or write operation will take place until $\overline{CE}$ has been high (above V_{IH}) for at least a precharge interval (t_{PC}). When it is brought low, an access will start.

Theory of Operation

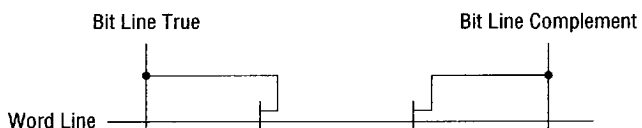
The FM1208S FRAM memory uses a patented ferroelectric technology to achieve nonvolatility. Ferroelectric material may be polarized in one direction or another with the application of an electric field, and will remain polarized when the field is removed. They are insensitive to magnetic fields.

The FM1208S is designed with a differential cell architecture, as shown in the figure below. During a read operation, the word line and plate enable lines are brought high, transferring charge from the ferroelectric storage elements to the bit lines. Nonvolatile elements polarized in the opposite direction to the field will source more charge than those polarized in the direction of the field. Sense amplifiers built into the chip compare the two charge magnitudes, producing a binary value. After the read operation, the data is then automatically re-written back into the nonvolatile elements.

During the write operation, the sense amplifiers drive the bit lines to the state of the data input pins. The word line is enabled and the place enable line is pulsed, polarizing each of the complementary nonvolatile storage elements in the appropriate direction.

The part may be read or written a total of 10 billion (10^{10}) cycles without degrading the data retention of the device. Operation of the part beyond this limit will eventually result in nonvolatile data retention failure.

FRAM Memory Cell



Absolute Maximum Ratings(1)

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	0 to +70°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Parameter	Description	Max	Test Condition
$C_{I/O}$ (2)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN} (2)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(2) This parameter is periodically sampled and not 100% tested.

DC Operating Conditions

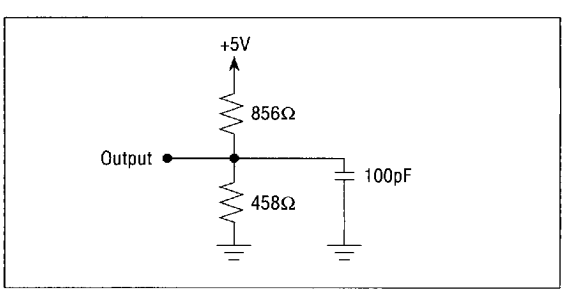
T_A = 0° to 70°C; Typical Values at 25°C

Symbol	Parameters	Min	Typ	Max	Test Condition
V_{CC}	Power Supply Voltage	4.5V	5.0	5.5V	
I_{CC1}	Power Supply Current - Active		5.0mA	10mA	V_{CC} = Max, $\overline{CE}$ Cycling at Minimum Cycle Time CMOS Input Levels and I/Os Unloaded
I_{SB1}	Power Supply Current - Standby (TTL)		200µA	1.2mA	V_{CC} = Max, $\overline{CE}$ = V_{IH}, TTL Input Levels, $I_{I/O}$ = 0mA
I_{SB2}	Power Supply Current - Standby (CMOS)		10µA	100µA	V_{CC} = Max, $\overline{CE}$ = V_{CC}, CMOS Input Levels, $I_{I/O}$ = 0mA
I_{IL}	Input Leakage Current			10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current			10µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-1V		0.8V	
V_{IH}	Input High Voltage	2.0V		V_{CC} + 1V	
V_{OL}	Output Low Voltage			0.4V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4V			I_{OH} = -2mA

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	0 to 3 V
Input Rise and Fall Time	10ns
Input and Output Timing Levels	1.5V

Equivalent AC Test Load Circuit



Pin Names

Pin Names	Function
A_0 - A_8	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input

Pin Names	Function
$\overline{OE}$	Output Enable Input
V_{CC}	+5 Volts
GND	Ground
NC	No Connect

Power Up/Power Down Timing(3)

Symbol	Parameter	Min	Units
t_{PU}	V_{CC} Stable to First Access	100	µs
t_{PD}(4)	Last Access to Power Down	0	µs

(3) Timing specifications measured to/from the time at which V_{CC} crosses 4.5V. These parameters are sampled and not 100% tested.
(4) Access, including precharge (t_{PC}) which follows, must complete before V_{CC} drops below 4.5V.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Read Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	JEDEC Symbol	Min	Max	Unit
t_{RC}	Read Cycle Time	t_{ELEL}	400		ns
t_{CA}	Chip Enable Active Time	t_{ELEH}	200	10,000	ns
t_{PC}	Precharge Time	t_{EHEL}	200		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		ns
t_{AH}	Address Hold Time	t_{ELAX}	30		ns
t_{CE}	Chip Enable Access Time	t_{ELQV}		200	ns
t_{OE}	Output Enable Access Time	t_{OLQV}		30	ns
t_{HZ}	Chip Enable to Output High-Z	t_{EHQZ}		45	ns
t_{OHZ}	Output Enable to Output High-Z	t_{OHQZ}		35	ns

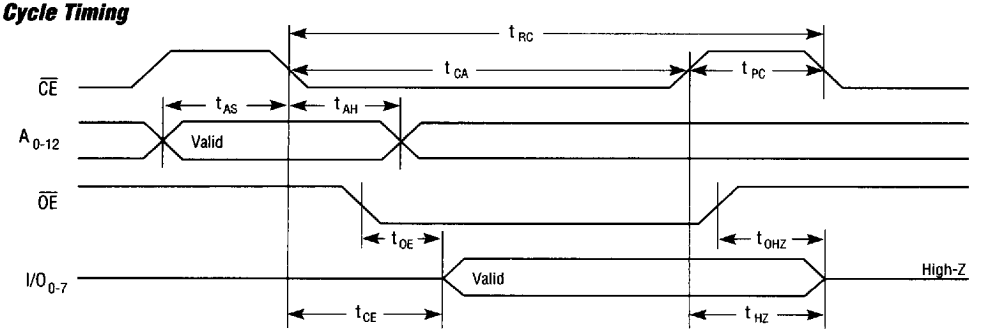
Write Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V ± 10%

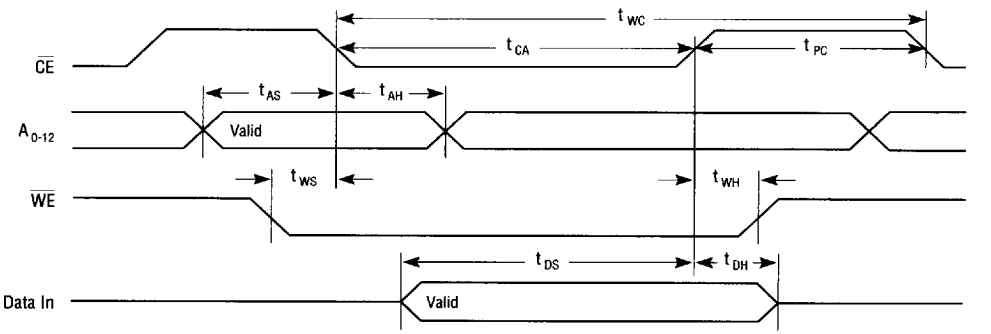
Symbol	Parameter	JEDEC Symbol	Min	Max	Unit
t_{WC}	Write Cycle Time	t_{ELEL}	400		ns
t_{CA}	Chip Enable Active Time	t_{ELEH}	200	10,000	ns
t_{CW}	Chip Enable to Write High	t_{ELWH}	200		ns
t_{PC}	Precharge Time	t_{EHEL}	200		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		ns
t_{AH}	Address Hold Time	t_{ELAX}	30		ns
t_{WP}	Write Enable Pulse Width	t_{WLWH}	80		ns
t_{DS}	Data Setup Time	t_{DVWH}	80		ns
t_{DH}	Data Hold Time	t_{WHDX}	5		ns
t_{WZ}(2)	Write Enable Low to Output High Z	t_{WLQZ}		25	ns
t_{WS}(5)	Write Setup	t_{CLWL}	0		ns
t_{WH}(5)	Write Hold	t_{WHCH}	0		ns

(2) This parameter is periodically sampled and not 100% tested.
(5) Not a device specification, merely distinguishes $\overline{CE}$ and $\overline{WE}$ controlled accesses.

Read Cycle Timing

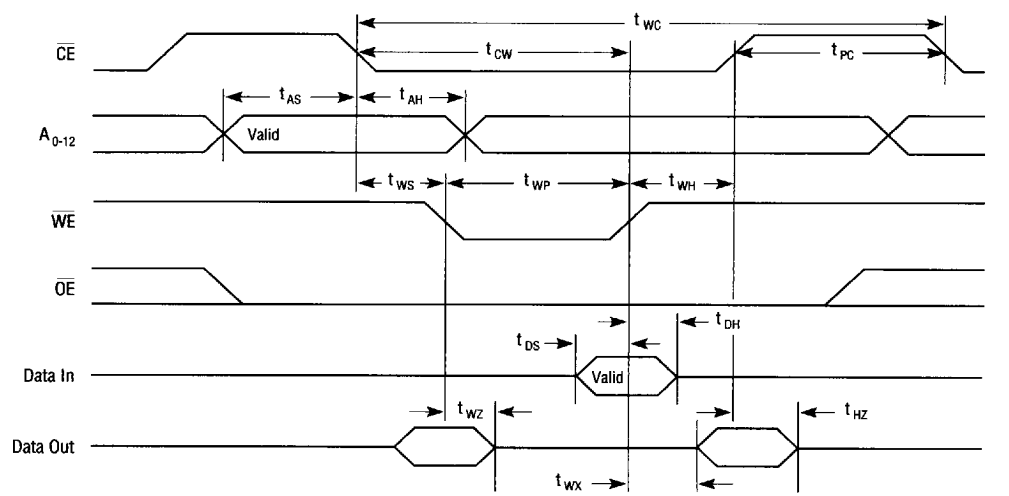


$\overline{CE}$ Controlled Write(6)



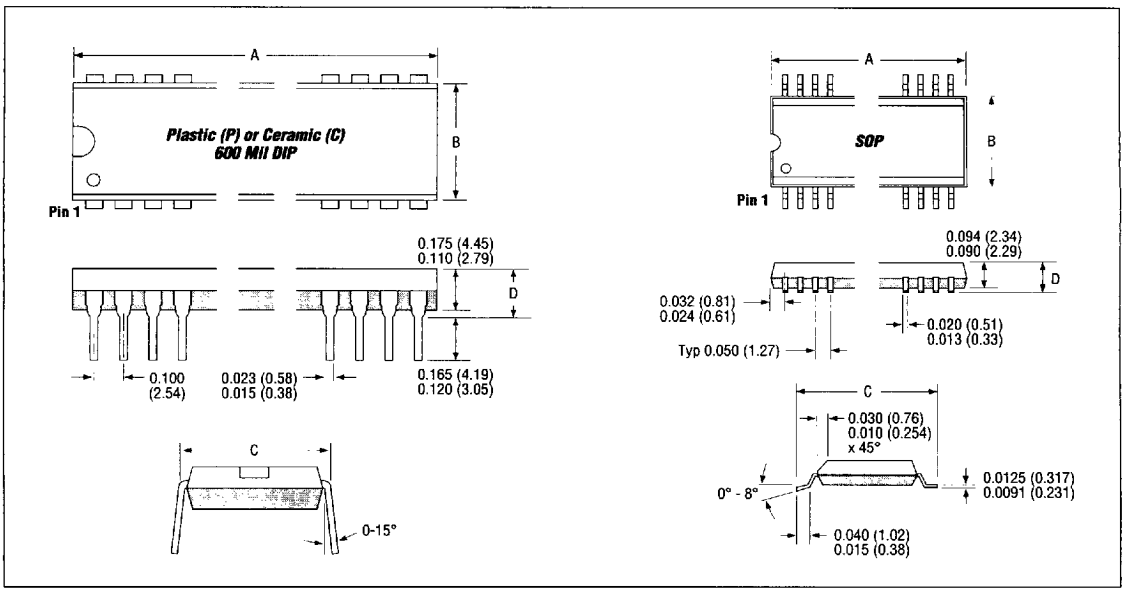
(6) State of $\overline{OE}$ does not affect operation of device for this cycle.

$\overline{WE}$ Controlled Write



Packaging Information

Package	Type	Dimensions in Inches (Millimeters)			
		FM1208S 24-Pin			
		A	B	C	D
Plastic/Ceramic 600 Mil DIP	P/PT/C	1.240 (32.64) 1.285 (31.50)	0.598 (15.19) 0.514 (13.06)	0.620 (15.75) 0.590 (14.99)	0.225 (5.72) 0.140 (3.56)
Plastic SOP	S	0.614 (15.59) 0.598 (15.19)	0.300 (7.62) 0.287 (7.29)	0.416 (10.57) 0.398 (10.11)	0.105 (2.65) 0.093 (2.35)



Ordering Information