| FUJITSU SEMICONDUCTOR |
| DATA SHEET |

FLASH MEMORY

CMOS

4M (512K × 8/256K × 16)

MBM29F400TA/MBM29F400BA

■ DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard word-wide pinouts**
  48-pin TSOP (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  44-pin SOP (Package suffix: PF)
- **Minimum 100,000 write/erase cycles**
- **High performance**
  70 ns maximum access time
- **Sector erase architecture**
  One 16 Kbyte, two 8 Kbytes, one 32 Kbyte and seven 64 Kbytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  20 mA typical active read current for Byte Mode
  28 mA typical active read current for Word Mode
  30 mA typical write/erase current
  25 µA typical standby current
- **Low Vcc write inhibit ≤ 3.2 V**
- **Sector protection**
  Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Boot Code Sector Architecture**
  T=Top sector
  B=Bottom sector

Embedded Erase™, Embedded Program™ and ExpressFlash™ are trademarks of Advanced Micro Devices, Inc.

■ GENERAL DESCRIPTION

The MBM29F400TA/BA is a 4M-bit, 5.0 V-only Flash memory organized as 512K bytes of 8 bits each or 256K words of 16 bits each. The MBM29F400TA/BA is offered in a 48-pin TSOP and 44-pin SOP packages. This device is designed to be programmed in-system with the standard system 5.0 V Vcc supply. A 12.0 V VPP is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers. The MBM29F400TA/BA is erased when shipped from the factory.

The standard MBM29F400TA/BA offers access times between 70 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The MBM29F400TA/BA is pin and command set compatible with JEDEC standard 4M-bit E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F400TA/BA is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed.)

This device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low Vcc detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of DQ7, by the Toggle Bit feature on DQ6, or the RY/$\overline{BY}$ pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The MBM29F400TA/BA memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

■ PRODUCT SELECTOR GUIDE

Part No:		MBM29F400TA/MBM29F400BA		
Ordering Part No:	Vcc = 5.0V±5%	− 70	−	−
	Vcc = 5.0V±10%	−	− 90	− 12
Max Access Time (ns)		70	90	120
$\overline{CE}$ ($\overline{E}$) Access (ns)		70	90	120
$\overline{OE}$ ($\overline{G}$) Access (ns)		30	35	50

■ BLOCK DIAGRAM
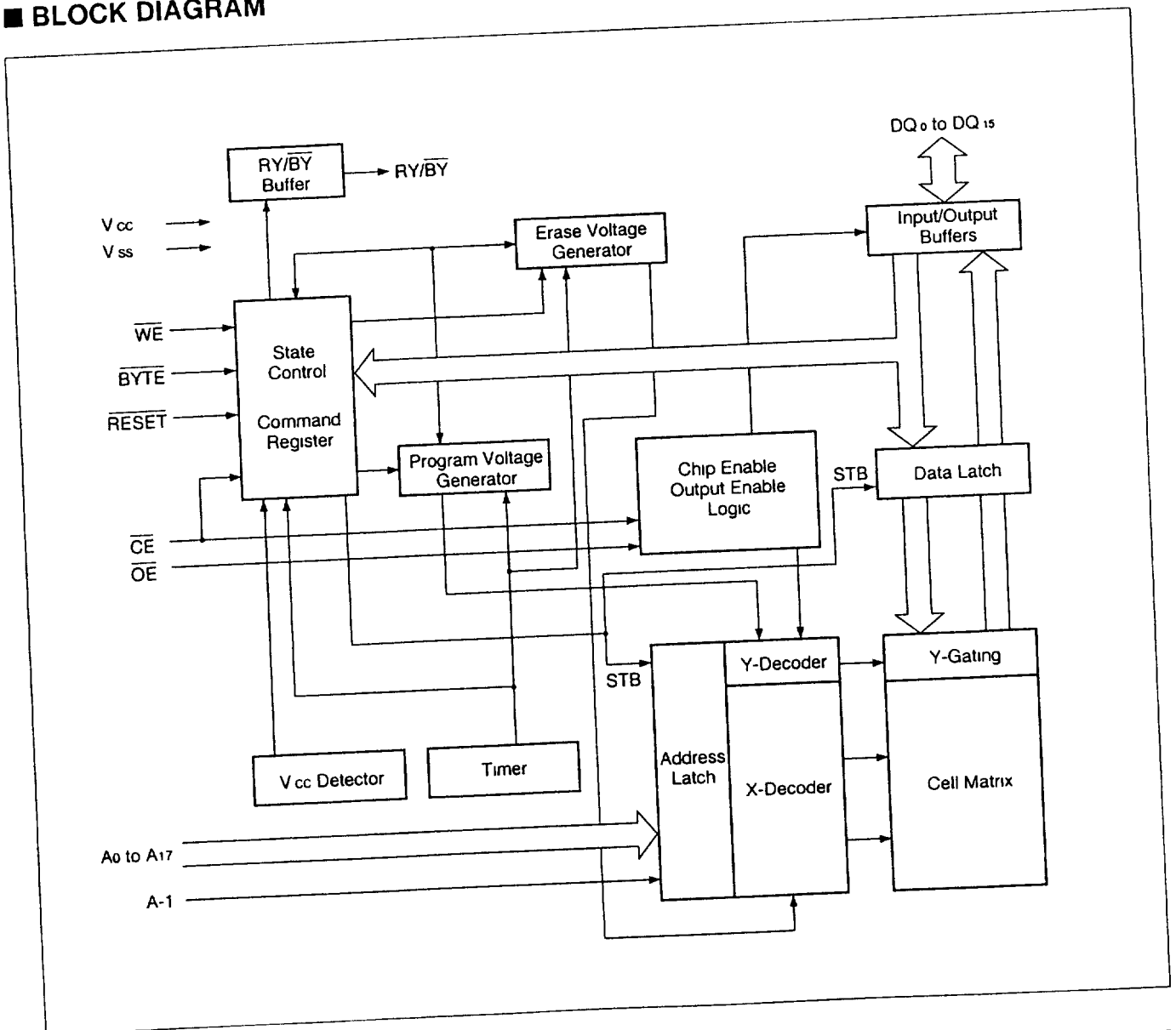
■ PACKAGE
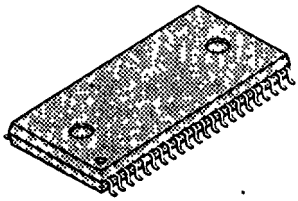
(FPT-44P-M16)
44-pin SOP

(FPT-48P-M19)

48-pin TSOP

(FPT-48P-M20)

MBM29F400TA/400BA

■ CONNECTION DIAGRAMS

SOP

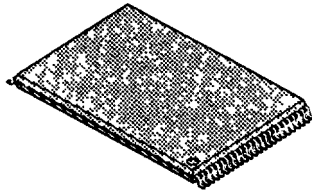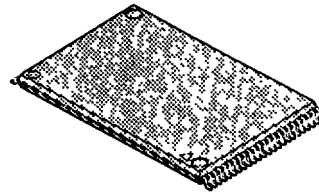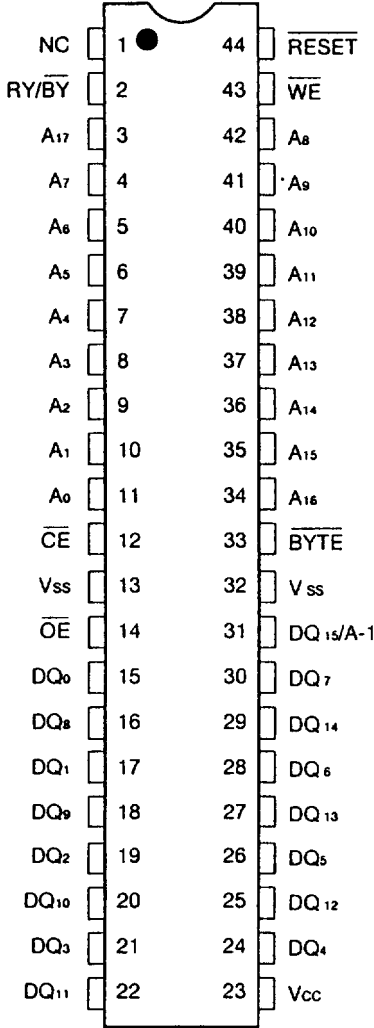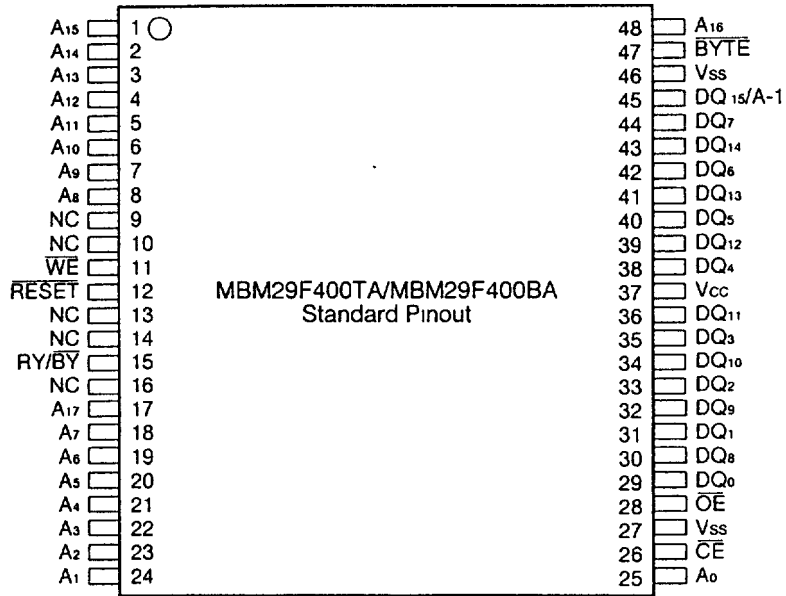|			
NC	1	44	$\overline{RESET}$
RY/$\overline{BY}$	2	43	$\overline{WE}$
A_{17}	3	42	A_8
A_7	4	41	A_9
A_6	5	40	A_{10}
A_5	6	39	A_{11}
A_4	7	38	A_{12}
A_3	8	37	A_{13}
A_2	9	36	A_{14}
A_1	10	35	A_{15}
A_0	11	34	A_{16}
$\overline{CE}$	12	33	$\overline{BYTE}$
Vss	13	32	Vss
$\overline{OE}$	14	31	DQ_{15}/A-1
DQ_0	15	30	DQ_7
DQ_8	16	29	DQ_{14}
DQ_1	17	28	DQ_6
DQ_9	18	27	DQ_{13}
DQ_2	19	26	DQ_5
DQ_{10}	20	25	DQ_{12}
DQ_3	21	24	DQ_4
DQ_{11}	22	23	Vcc

TSOP

MBM29F400TA/MBM29F400BA Standard Pinout

A_{15}	1	48	A_{16}
A_{14}	2	47	$\overline{BYTE}$
A_{13}	3	46	Vss
A_{12}	4	45	DQ_{15}/A-1
A_{11}	5	44	DQ_7
A_{10}	6	43	DQ_{14}
A_9	7	42	DQ_6
A_8	8	41	DQ_{13}
NC	9	40	DQ_5
NC	10	39	DQ_{12}
$\overline{WE}$	11	38	DQ_4
$\overline{RESET}$	12	37	Vcc
NC	13	36	DQ_{11}
NC	14	35	DQ_3
RY/$\overline{BY}$	15	34	DQ_{10}
NC	16	33	DQ_2
A_{17}	17	32	DQ_9
A_7	18	31	DQ_1
A_6	19	30	DQ_8
A_5	20	29	DQ_0
A_4	21	28	$\overline{OE}$
A_3	22	27	Vss
A_2	23	26	$\overline{CE}$
A_1	24	25	A_0

MBM29F400TA/MBM29F400BA Reverse Pinout

A_{16}	1	48	A_{15}
$\overline{BYTE}$	2	47	A_{14}
Vss	3	46	A_{13}
DQ_{15}/A-1	4	45	A_{12}
DQ_7	5	44	A_{11}
DQ_{14}	6	43	A_{10}
DQ_6	7	42	A_9
DQ_{13}	8	41	A_8
DQ_5	9	40	NC
DQ_{12}	10	39	NC
DQ_4	11	38	$\overline{WE}$
Vcc	12	37	$\overline{RESET}$
DQ_{11}	13	36	NC
DQ_3	14	35	NC
DQ_{10}	15	34	RY/$\overline{BY}$
DQ_2	16	33	NC
DQ_9	17	32	A_{17}
DQ_1	18	31	A_7
DQ_8	19	30	A_6
DQ_0	20	29	A_5
$\overline{OE}$	21	28	A_4
Vss	22	27	A_3
$\overline{CE}$	23	26	A_2
A_0	24	25	A_1

■ LOGIC SYMBOL

Table 1 MBM29F400TA/BA Pin Configuration

Pin	Function
A-1, A0 to A17	Address Inputs
DQ0 to DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
NC	No Internal Connection
Vss	Device Ground
Vcc	Device Power Supply (5.0V±10% or ±5%)

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

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MBM29F400    TA    -70    PFTN
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PACKAGE TYPE
PFTN = 48-Pin Thin Small Outline Package
(TSOP) Standard Pinout
PFTR = 48-Pin Thin Small Outline Package
(TSOP) Reverse Pinout
PF = 44-Pin Small Outline Package

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
TA = Top sector
BA = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29F400
4Mega-bit (512K × 8-Bit or 256K × 16-Bit) CMOS Flash Memory
5.0 V-only Read, Write and Erase

Valid Combinations	
MBM29F400TA/BA-70	
MBM29F400TA/BA-90	PFTN, PFTR, PF
MBM29F400TA/BA-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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Table 2   MBM29F400TA/BA User Bus Operations ($\overline{\text{BYTE}}$ = V$_{\text{IH}}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A$_0$	A$_1$	A$_6$	A$_9$	DQ$_0$ to DQ$_{15}$	$\overline{\text{RESET}}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V$_{\text{ID}}$	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V$_{\text{ID}}$	Code	H
Read (3)	L	L	H	A$_0$	A$_1$	A$_6$	A$_9$	D$_{\text{OUT}}$	H
Standby	H	X	X	X	X	X	X	HIGH-Z	H
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H
Write	L	H	L	A$_0$	A$_1$	A$_6$	A$_9$	D$_{\text{IN}}$	H
Enable Sector Protect (2)	L	V$_{\text{ID}}$	L	X	X	X	V$_{\text{ID}}$	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V$_{\text{ID}}$	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V$_{\text{ID}}$
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L

Table 3   MBM29F400TA/BA User Bus Operations ($\overline{\text{BYTE}}$ = V$_{\text{IL}}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A$_0$	A$_1$	A$_6$	A$_9$	DQ$_0$ to DQ$_7$	$\overline{\text{RESET}}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V$_{\text{ID}}$	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V$_{\text{ID}}$	Code	H
Read (3)	L	L	H	A$_0$	A$_1$	A$_6$	A$_9$	D$_{\text{OUT}}$	H
Standby	H	X	X	X	X	X	X	HIGH-Z	H
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H
Write	L	H	L	A$_0$	A$_1$	A$_6$	A$_9$	D$_{\text{IN}}$	H
Enable Sector Protect (2)	L	V$_{\text{ID}}$	L	X	X	X	V$_{\text{ID}}$	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V$_{\text{ID}}$	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V$_{\text{ID}}$
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L

Legend:
L = V$_{\text{IL}}$, H = V$_{\text{IH}}$, X = Don't Care. See DC Characteristics for voltage levels.

Notes:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 7.
2. Refer to the section on Sector Protection.
3. $\overline{\text{WE}}$ can be V$_{\text{IL}}$ if $\overline{\text{OE}}$ is V$_{\text{IL}}$, $\overline{\text{OE}}$ at V$_{\text{IH}}$ initiates the write operations.

Read Mode

The MBM29F400TA/BA has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (tACC) is equal to the delay from stable addresses to valid output data. The chip enable access time (tCE) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least tACC-tOE time).

Standby Mode

The MBM29F400TA/BA has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc ± 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at VIH) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (VIH), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0, A1 and A6.

The manufacturer and device codes may also be read via the command register, for instances when the MBM29F400TA/BA is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 7 (refer to Autoselect Command section).

Byte 0 (A0 = VIL) represents the manufacturer's code (Fujitsu = 04H) and byte 1 (A0 = VIH) the device identifier code (MBM29F400TA = 23H and MBM29F400BA = ABH for x8 mode; MBM29F400TA = 2223H and MBM29F400BA = 22ABH for x16 mode). These two bytes/words are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be VIL (see Tables 4.1 and 4.2).

Table 4.1   MBM29F400TA/BA Sector Protection Verify Autoselect Codes

Type			A_{12} to A_{17}	A_6	A_1	A_0	Code (HEX)
Manufacturer's Code			X	VIL	VIL	VIL	04H
MBM29F400A Device Code	MBM29F400TA	Byte	X	VIL	VIL	VIH	23H
		Word					2223H
	MBM29F400BA	Byte	X	VIL	VIL	VIH	ABH
		Word					22ABH
Sector Protection			Sector Addresses	VIL	VIH	VIL	01H*

*Outputs 01H at protected sector addresses

Table 4.2   Expanded Autoselect Code Table

Type		Code	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer's Code		04H	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MBM29F400A Device Code	MBM29F400TA (B)	23H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	0	0	1	1
	(W)	2223H	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1
	MBM29F400BA (B)	ABH	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	0	1	0	1	0	1	1
	(W)	22ABH	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1
Sector Protection		01H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode
(W): Word mode

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to VIL, while $\overline{CE}$ is at VIL and $\overline{OE}$ is at VIH. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The MBM29F400TA/BA features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 10). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, Fujitsu may program and protect sectors in the factory prior to shipping the device (AMD's Express Flash™ service).

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest $V_{ID} = 11.5$ V) and $\overline{CE} = V_{IL}$. The sector addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the eleven (11) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 14 and 20 for sector protection algorithm and waveforms.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) while (A_6, A_1, A_0) $= (0, 1, 0)$ will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce 00H for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1 and A_6 are don't care. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) are the sector address will produce a logical "1" at DQ_0 for a protected sector. See Table 4.1 for Autoselect codes.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors of the MBM29F400TA/BA device in order to change data. The Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to high voltage (12V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12V is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again.

Sector Unprotect

The MBM29F400TA/BA also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To active this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A_9. The $\overline{CE}$ and A_0 pins must be set at V_{IL}. Pins A_6 and A_1 must be set to V_{IH}. Refer to Figure 21 for the sector unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A_6 is set at V_{IL}. Performing a read operation at address location XXX2H, where the higher order addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) define a particular sector address, will produce 00H at data outputs (DQ_0 to DQ_7) for an unprotected sector.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable). Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Table 5   Sector Address Tables (MBM29F400TA)

Sector Address	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range
SA0	0	0	0	X	X	X	00000h–0FFFFh
SA1	0	0	1	X	X	X	10000h–1FFFFh
SA2	0	1	0	X	X	X	20000h–2FFFFh
SA3	0	1	1	X	X	X	30000h–3FFFFh
SA4	1	0	0	X	X	X	40000h–4FFFFh
SA5	1	0	1	X	X	X	50000h–5FFFFh
SA6	1	1	0	X	X	X	60000h–6FFFFh
SA7	1	1	1	0	X	X	70000h–77FFFh
SA8	1	1	1	1	0	0	78000h–79FFFh
SA9	1	1	1	1	0	1	7A000h–7BFFFh
SA10	1	1	1	1	1	X	7C000h–7FFFFh

Table 6   Sector Address Tables (MBM29F400BA)

Sector Address	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range
SA0	0	0	0	0	0	X	00000h–03FFFh
SA1	0	0	0	0	1	0	04000h–05FFFh
SA2	0	0	0	0	1	1	06000h–07FFFh
SA3	0	0	0	1	X	X	08000h–0FFFFh
SA4	0	0	1	X	X	X	10000h–1FFFFh
SA5	0	1	0	X	X	X	20000h–2FFFFh
SA6	0	1	1	X	X	X	30000h–3FFFFh
SA7	1	0	0	X	X	X	40000h–4FFFFh
SA8	1	0	1	X	X	X	50000h–5FFFFh
SA9	1	1	0	X	X	X	60000h–6FFFFh
SA10	1	1	1	X	X	X	70000h–7FFFFh

Table 7   MBM29F400TA/BA Command Definitions

Command Sequence Read/Reset		Bus Write Cycles Req'd	First Bus Write Cycle Addr	Data	Second Bus Write Cycle Addr	Data	Third Bus Write Cycle Addr	Data	Fourth Bus Read/Write Cycle Addr	Data	Fifth Bus Write Cycle Addr	Data	Sixth Bus Write Cycle Addr	Data
Read/Reset	Word	1	XXXXH	F0H										
	Byte													
Read/Reset	Word	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
	Byte		AAAAH		5555H		AAAAH							
Autoselect	Word	4	5555H	AAH	2AAAH	55H	5555H	90H						
	Byte		AAAAH		5555H		AAAAH							
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
	Byte		AAAAH		5555H		AAAAH							
Chip Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Sector Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care). Data (B0H)												
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care). Data (30H)												

Notes:
1. Address bit A15 = X = Don't Care for all address commands except or Program Address (PA) and Sector Address (SA). Write Sequences may be initiated with A15 in either state.
2. Address bit A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. Bus operations are defined in Table 2 and 3.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14, A13 and A12 will uniquely select any sector.
5. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
6. The system should generate the following address patterns:
   Word Mode: 5555H or 2AAAH to addresses A0 to A14
   Byte Mode: AAAAH or 5555H to addresses A-1 to A14

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 04H. A read cycle from address XX01H returns the device code (MBM29F400TA = 23H and MBM29F400BA = ABH for x8 mode; MBM29F400TA = 2223H and MBM29F400BA = 22ABH for x16 mode). (See Tables 4.1 and 4.2.)

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Scanning the sector addresses (A17, A16, A15, A14, A13 and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program™ Algorithm command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 16 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 17 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data=30H) is latched on the rising edge of $\overline{WE}$. A time-out of 50 μs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased sequentially by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 μs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 μs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 50 μs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 10).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50 μs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to the read mode. Data polling must be performed at an address within any of the sectors being erased.

Figure 17 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then perform data reads (not program) from a non-busy sector during a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B0H) which is allowed only during the Sector Erase Operation includes the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 μs to 15 μs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit (DQ6) to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command, the user must wait until the toggle bit stops toggling before data reads from the device can be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 8   Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2 to DQ0
In Progress	Auto-Programming	$\overline{DQ_7}$	Toggle	0	0	$(\overline{D})$ (Note 1)
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ_7}$	Toggle	1	1	$(\overline{D})$ (Note 1)
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Notes:
1. DQ0, DQ1 and DQ2 are reserve pins for future use.
2. DQ8 to DQ15 = Don't Care for x16 mode.
3. DQ4 is for Fujitsu internal use only.

DQ7

Data Polling

The MBM29F400TA/BA device features Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for Data Polling (DQ7) is shown in Figure 18.

For chip erase, the Data Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the MBM29F400TA/BA data pins (DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0 to DQ6 may be still invalid. The valid data on DQ0 to DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out (see Table 8).

See Figure 8 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6

Toggle Bit

The MBM29F400TA/BA also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 μs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 μs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle.

See Figure 9 for the Toggle Bit timing specifications and diagrams.

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2 and 3.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

It this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 8: Hardware Sequence Flags.

RY/$\overline{BY}$

Ready/Busy

The MBM29F400TA/BA provides a RY/$\overline{BY}$ output pin as a way to indicate to the host system that the Embedded™ Algorithms are either in progress or completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/$\overline{BY}$ pin is low, the device will not accept any additional program or erase commands. If the MBM29F400TA/BA is placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high. Also, since this is an open drain output, many RY/$\overline{BY}$ pins can be tied together in parallel with a pull up resistor to Vcc.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth $\overline{WE}$ pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth $\overline{WE}$ pulse. The RY/$\overline{BY}$ pin should be ignored while $\overline{RESET}$ is at VIL. Refer to Figure 13 for a detailed timing diagram.

$\overline{RESET}$

Hardware Reset

The MBM29F400TA/BA device may be reset by driving the $\overline{RESET}$ pin to VIL. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (VIL) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset 20 μs after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the device requires an additional 50 ns before it will allow read access. When the $\overline{RESET}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. Refer to Figure 11 for the timing diagram. Refer to Temporary Sector Unprotect for additional functionality.

Byte/Word Configuration

The $\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29F400TA/BA device. When this pin is driven high, the device operates in the word (16-bit) mode. The data is read and programmed at DQ0 to DQ15. When this pin is driven low, the device operates in byte (8-bit) mode. Under this mode, the DQ15/A-1 pin becomes the lowest address bit and DQ8 to DQ14 bits are tristated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ0 to DQ7 and the DQ8 to DQ15 bits are ignored. Refer to Figures 12 and 13 for the timing diagram.

Data Protection

The MBM29F400TA/BA is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form Vcc power-up and power-down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2 V (typically 3.7 V). If Vcc < VLKO, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the Vcc level is greater than VLKO. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ =VIL and $\overline{OE}$ = VIH will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature Plastic Packages ....–65°C to +125°C
Ambient Temperature with Power Applied ....–55°C to +125°C
Voltage with Respect to Ground All pins except A9 (Note 1) ....–2.0 V to +7.0 V
Vcc (Note 1) ....–2.0 V to +7.0 V
A9 (Note 2) ....–2.0 V to +14.0 V
Output Short Circuit Current (Note 3) ....200 mA

Notes:
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may negative overshoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is Vcc +0.5 V. During voltage transitions, outputs may overshoot to Vcc +2.0 V for periods of up to 20 ns.
2. Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may negative overshoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods of up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

■ OPERATING RANGES

Commercial Devices
  Ambient Temperature (TA) ....0°C to +70°C

Vcc Supply Voltages
  Vcc for MBM29F400TA-70/BA-70...+4.75 V to +5.25 V
  Vcc for MBM29F400TA-90, 12 /BA-90, 12.................................+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MBM29F400TA/400BA

■ MAXIMUM OVERSHOOT
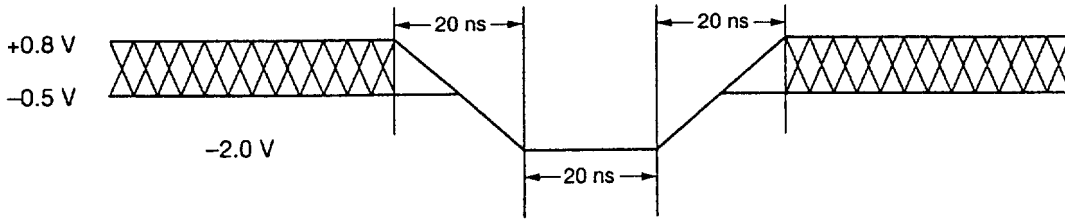
Figure 1 Maximum Negative Overshoot Waveform
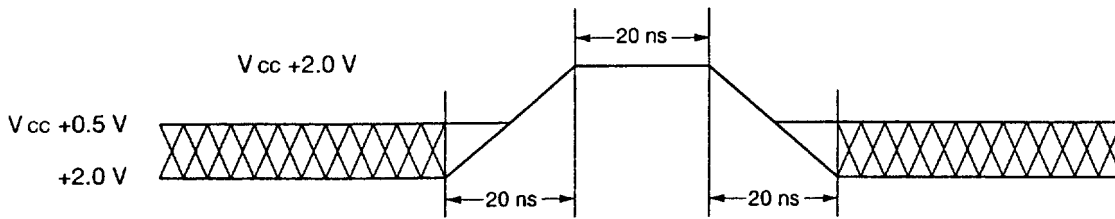
Figure 2 Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

• **TTL/NMOS Compatible**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = Vss to Vcc, Vcc = Vcc Max		—	±1.0	μA
I_{LIT}	A9 Input Leakage Current	Vcc = Vcc Max, A9 = 12.5V		—	50	μA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to Vcc, Vcc = Vcc Max		—	±1.0	μA
I_{CC1}	Vcc Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte	—	40	mA
			Word		50	
I_{CC2}	Vcc Active Current (Note 2, 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	60	mA
I_{CC3}	Vcc Standby Current	Vcc = Vcc Max, $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}		—	1.0	mA
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	Vcc+0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	Vcc = 5.0V		11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA, Vcc = Vcc Min		—	0.45	V
V_{OH}	Output High Level	I_{OH} = −2.5mA, Vcc = Vcc Min		2.4	—	V
V_{LKO}	Low Vcc Lock-Out Voltage			3.2	4.2	V

Notes:
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. Not 100% tested.

• **CMOS Compatible**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = Vss to Vcc, Vcc = Vcc Max		—	±1.0	μA
I_{LIT}	A9 Input Leakage Current	Vcc = Vcc Max, A9 = 12.5V		—	50	μA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to Vcc, Vcc = Vcc Max		—	±1.0	μA
I_{CC1}	Vcc Active Current (Note 1)	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH	Byte	—	40	mA
			Word		50	
I_{CC2}	Vcc Active Current (Note 2, 3)	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH		—	60	mA
I_{CC3}	Vcc Standby Current	Vcc = Vcc Max, $\overline{CE}$ = Vcc±0.5V, $\overline{OE}$ = VIH		—	100	μA
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			0.7×Vcc	Vcc+0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	Vcc = 5.0V		11.5	12.5	V
V_{OL}	Output Low Voltage	IOL = 5.8 mA, Vcc = Vcc Min		—	0.45	V
V_{OH1}	Output High Voltage	IOH = −2.5 mA, Vcc = Vcc Min		0.85Vcc	—	V
V_{OH2}		IOH = −100 μA, Vcc = Vcc Min		Vcc−0.4	—	V
V_{LKO}	Low Vcc Lock-out Voltage			3.2	4.2	V

Notes:
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at VIH.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. Not 100% tested.

■ AC CHARACTERISTICS

• Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		-70 (Note 1)	-90 (Note 2)	-12 (Note 2)	Unit
JEDEC	Standard							
tAVAV	tRC	Read Cycle Time (Note 4)		Min.	70	90	120	ns
tAVQV	tACC	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	90	120	ns
tELQV	tCE	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	90	120	ns
tGLQV	tOE	Output Enable to Output Delay		Max.	30	35	50	ns
tEHQZ	tDF	Chip Enable to Output High-Z (Notes 3, 4)		Max.	20	20	30	ns
tGHQZ	tDF	Output Enable to Output High-Z (Notes 3, 4)		Max.	20	20	30	ns
tAXQX	tOH	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	0	0	ns
	tREADY	$\overline{RESET}$ pin low to read mode		Max.	20	20	20	μs
	tELFL tELFH	$\overline{CE}$ or $\overline{BYTE}$ switching low or high		Max.	5	5	5	ns

Notes:

1. Test Conditions:
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0V to 3.0V
   Timing measurement reference level
     Input: 1.5V
     Output: 1.5V

2. Test Conditions:
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45V to 2.4V
   Timing measurement reference level
     Input: 0.8 and 2.0V
     Output: 0.8 and 2.0V

3. Output driver disable time.
4. Not 100% tested.
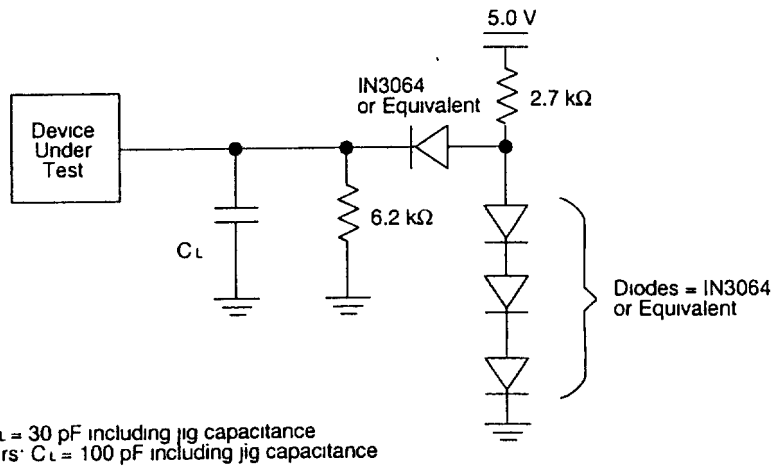
Figure 3 Test Conditions

• Write/Erase/Program Operations
  Alternate $\overline{\text{WE}}$ Controlledn Writes

Parameter Symbols		Description		-70	-90	-12	Unit
JEDEC	Standard						
tAVAV	tWC	Write Cycle Time (Note 3)	Min.	70	90	120	ns
tAVWL	tAS	Address Setup Time	Min.	0	0	0	ns
tWLAX	tAH	Address Hold Time	Min.	45	45	50	ns
tDVWH	tDS	Data Setup Time	Min.	30	45	50	ns
tWHDX	tDH	Data Hold Time	Min.	0	0	0	ns
	tOES	Output Enable Setup Time (Note 3)	Min.	0	0	0	ns
	tOEH	Output Enable Hold Time	Read (Note 3)	Min.	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling (Note 3)	Min.	10	10	10	ns

Notes: (Continued)
  1. This does not include the preprogramming time.
  2. These timings are for Sector Protect operation.
  3. Not 100% tested.
  4. Output Driver Disable Time.
  5. These timings are for Sector Unprotect operation.

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(Continued)

Parameter Symbols		Description		-70	-90	-12	Unit
JEDEC	Standard						
tGHWL	tGHWL	Read Recover Time Before Write	Min.	0	0	0	ns
tELWL	tCS	$\overline{CE}$ Setup Time	Min.	0	0	0	ns
tWHEH	tCH	$\overline{CE}$ Hold Time	Min.	0	0	0	ns
tWLWH	tWP	Write Pulse Width	Min.	35	45	50	ns
tWHWL	tWPH	Write Pulse Width High	Min.	20	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation	Typ.	16	16	16	µs
tWHWH2	tWHWH2	Erase Operation (Note 1)	Typ.	1.5	1.5	1.5	sec
			Max.	30	30	30	sec
	tVCS	Vcc Set Up Time (Note 3)	Min.	50	50	50	µs
	tVLHT	Voltage Transition Time (Notes 2, 3, 5)	Min.	4	4	4	µs
	tWPP	Write Pulse Width (Note 2)	Min.	100	100	100	µs
	tWPP2	Write Pulse Width (Note 5)	Min.	10	10	10	ms
	tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Notes 2, 3, 5)	Min.	4	4	4	µs
	tCSP	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 3)	Min.	4	4	4	µs
	tRP	$\overline{RESET}$ Pulse Width	Min.	500	500	500	ns
	tFLQZ	$\overline{BYTE}$ Switching Low to Output High-Z (Notes 3, 4)	Max.	20	30	30	ns
	tBUSY	Program/Erase Valid to RD/$\overline{BY}$ Delay (Note 3)	Min.	30	35	50	ns

Notes:
1. This does not include the preprogramming time.
2. These timings are for Sector Protect operation.
3. Not 100% tested.
4. Output Driver Disable Time.
5. These timings are for Sector Unprotect operation.

- **Write/Erase/Program Operations**
  Alternate CE Controlled Writes

Parameter Symbols		Description			–70	–90	–12	Unit
JEDEC	Standard							
tAVAV	tWC	Write Cycle Time (Note 4)		Min.	70	90	120	ns
tAVEL	tAS	Address Setup Time		Min.	0	0	0	ns
tELAX	tAH	Address Hold Time		Min.	45	45	50	ns
tDVEH	tDS	Data Setup Time		Min.	30	45	50	ns
tEHDX	tDH	Data Hold Time		Min.	0	0	0	ns
	tOES	Output Enable Setup Time		Min.	0	0	0	ns
	tOEH	Output Enable Hold Time (Note 4)	Read (Note 4)	Min.	0	0	0	ns
			Toggle and Data Polling	Min.	10	10	10	ns
tGHEL	tGHEL	Read Recover Time Before Write		Min.	0	0	0	ns
tWLEL	tWS	WE Setup Time		Min.	0	0	0	ns
tEHWH	tWH	WE Hold Time		Min.	0	0	0	ns
tELEH	tCP	CE Pulse Width		Min.	35	45	50	ns
tEHEL	tCPH	CE Pulse Width High		Min.	20	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation		Typ.	16	16	16	μs
tWHWH2	tWHWH2	Erase Operation (Note 1)		Typ.	1.5	1.5	1.5	sec
				Max.	30	30	30	sec
	tVCS	Vcc Set Up Time (Note 4)		Typ.	50	50	50	μs
	tRP	RESET Pulse Width		Min.	500	500	500	ns
	tFLQZ	BYTE Switching Low to Output High-Z (Notes 3, 4)		Max.	20	30	30	ns
	tBUSY	Program/Erase Valid to RD/BY Delay (Note 4)		Min.	30	35	50	ns

Notes:
1. This does not include the preprogramming time.
2. These timings are for Sector Protect/Unprotect operations.
3. This timing is only for Sector Unprotect.
4. Not 100% tested.

■ SWITCHING WAVEFORMS

• Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care: Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State
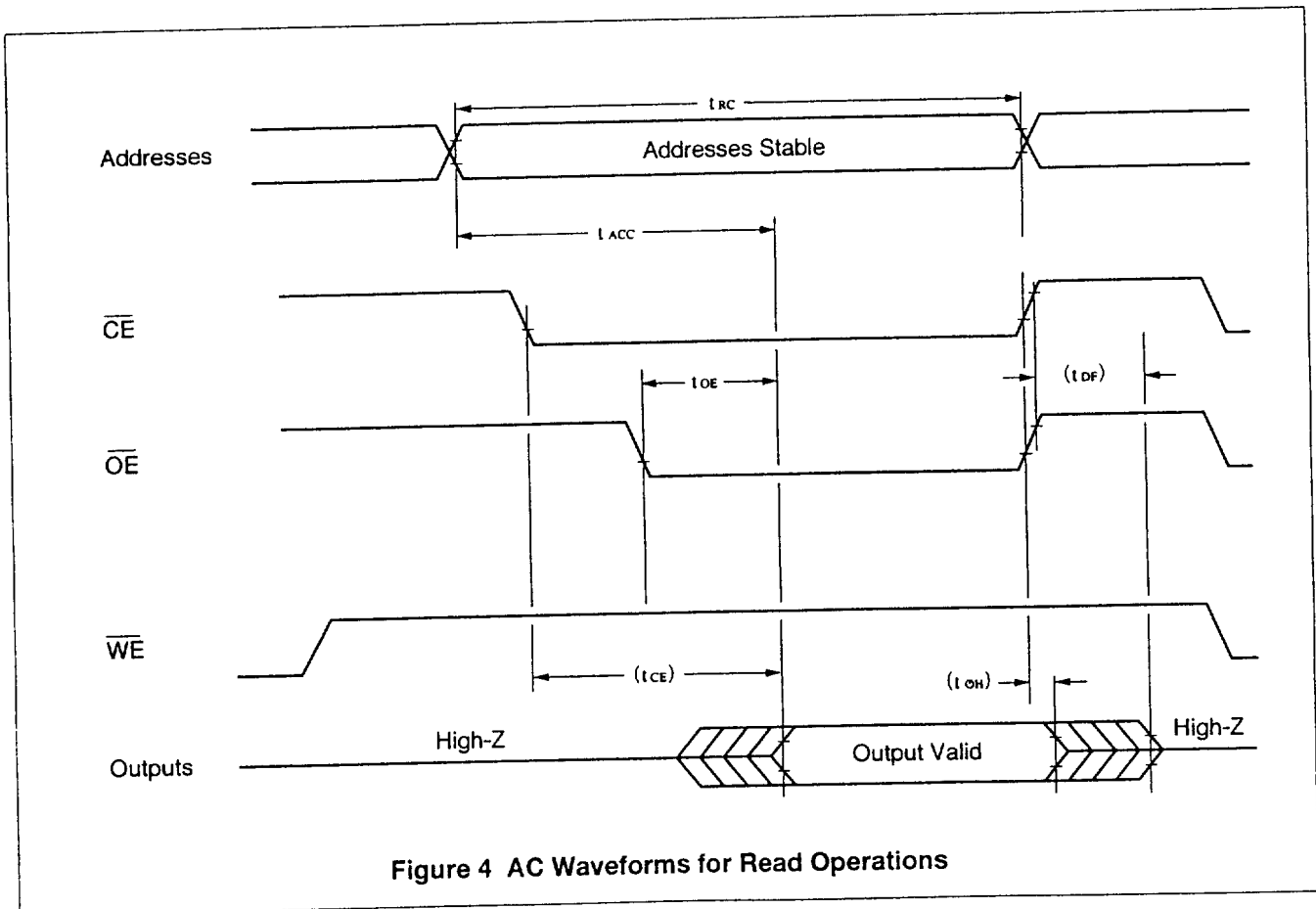
Figure 4 AC Waveforms for Read Operations
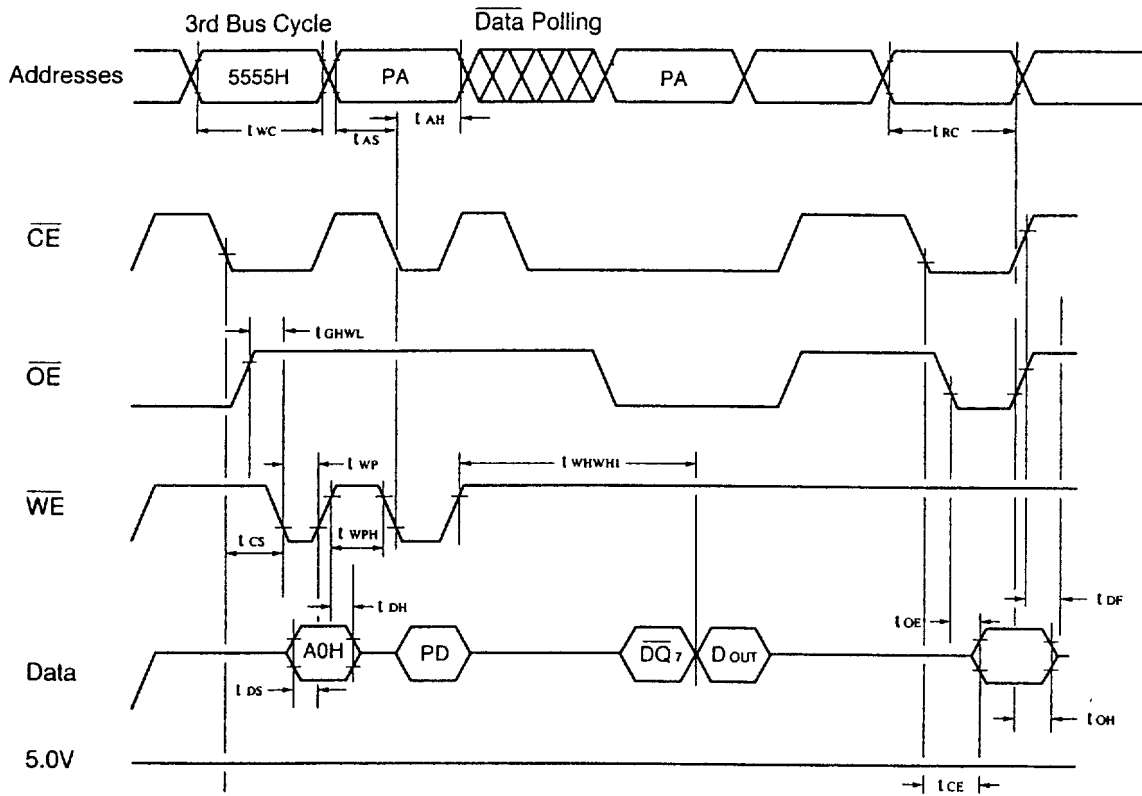
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D$_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

Figure 5 Program Operation Timings
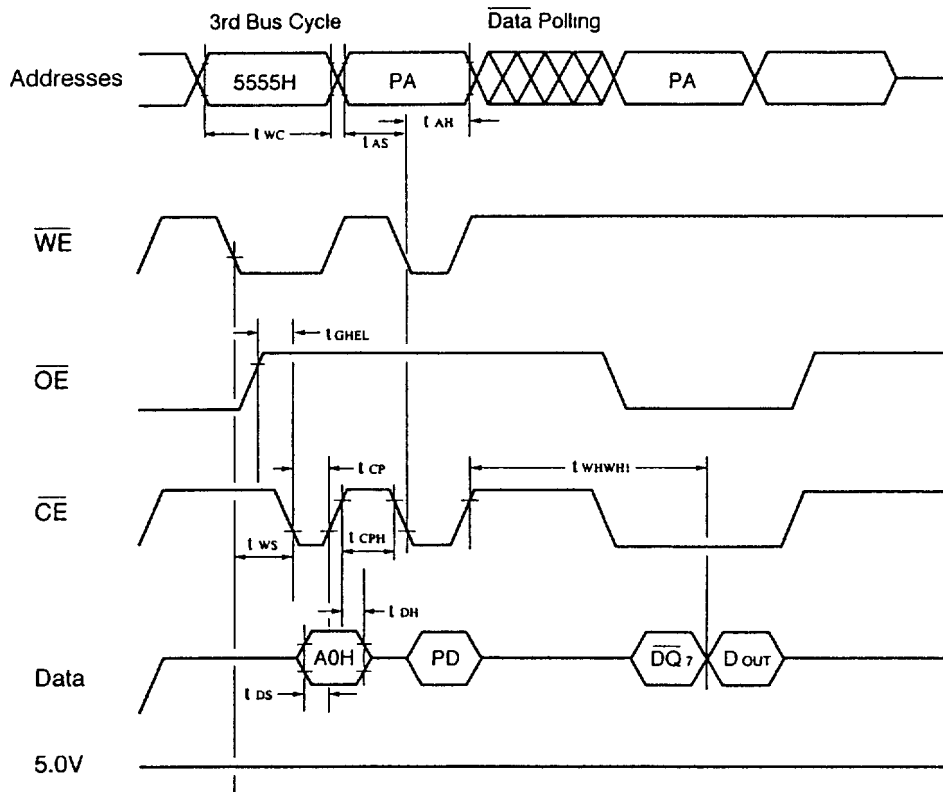
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ7}$ is the output of the complement of the data written to the device.
4. D$_{OUT}$ is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

Figure 6 Alternate $\overline{CE}$ Controlled Program Operation Timings
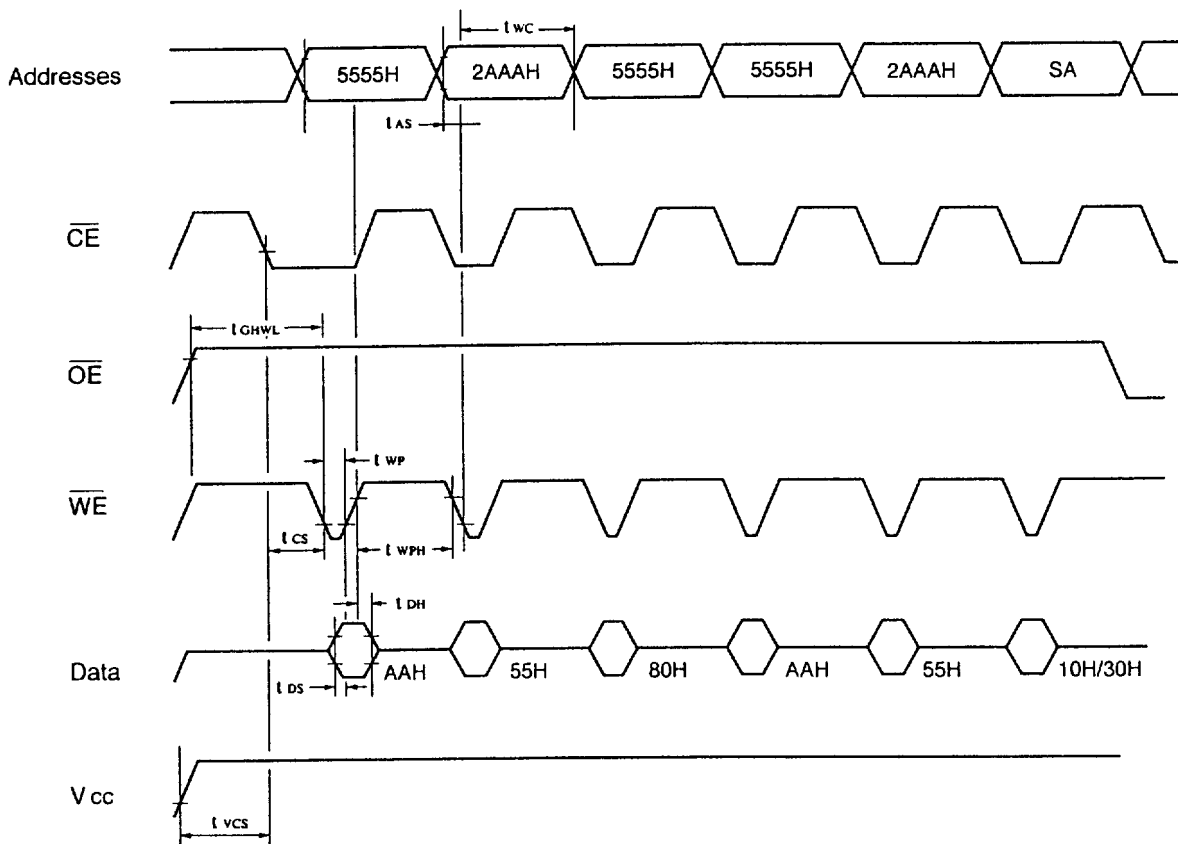
Notes:
1. SA is the sector address for Sector Erase. Addresses = 5555H for Word, AAAAH for Byte.
2. These waveforms are for the x16 mode.

Figure 7 AC Waveforms Chip/Sector Erase Operations
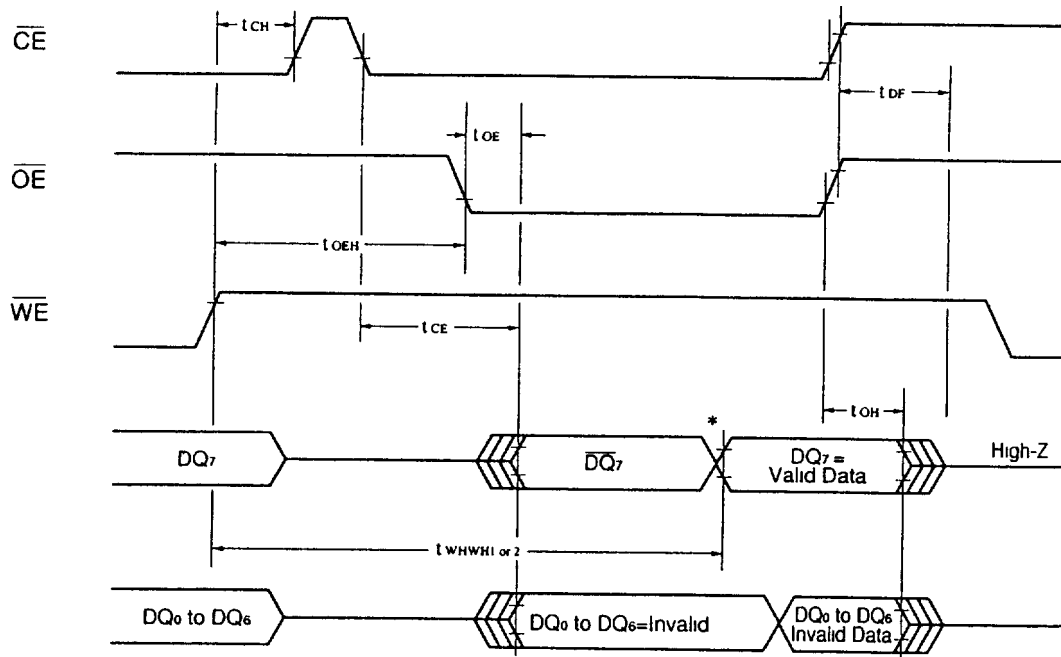
*DQ7 = Valid Data (The device has completed the Embedded operation).

Figure 8 AC Waveforms for Data Polling during Embedded Algorithm Operations
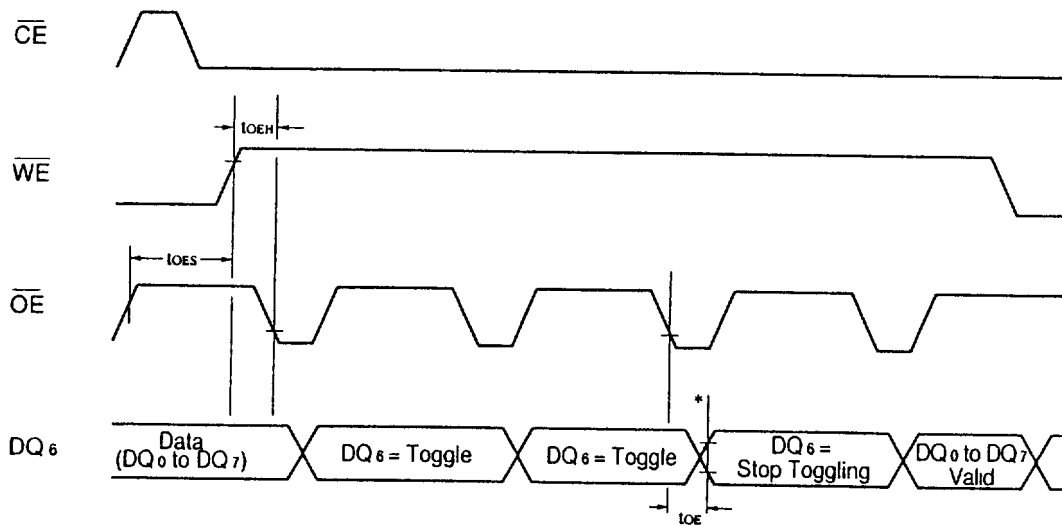
*DQ6 stops toggling (The device has completed the Embedded operation).

Figure 9 AC Waveforms for Toggle Bit during Embedded Algorithm Operations
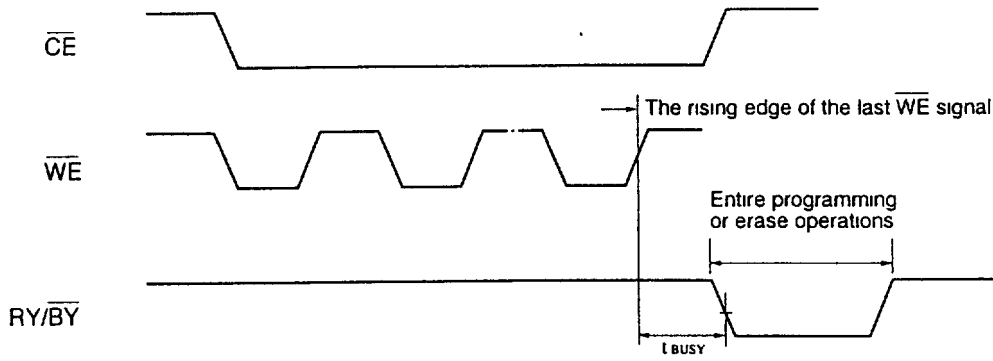
Figure 10 RY/$\overline{BY}$ Timing Diagram during Program/Erase Operations
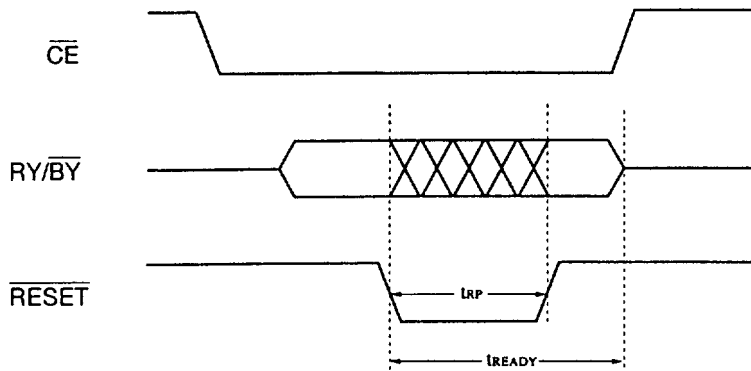
Figure 11 $\overline{RESET}$/RY/$\overline{BY}$ Timing Diagram
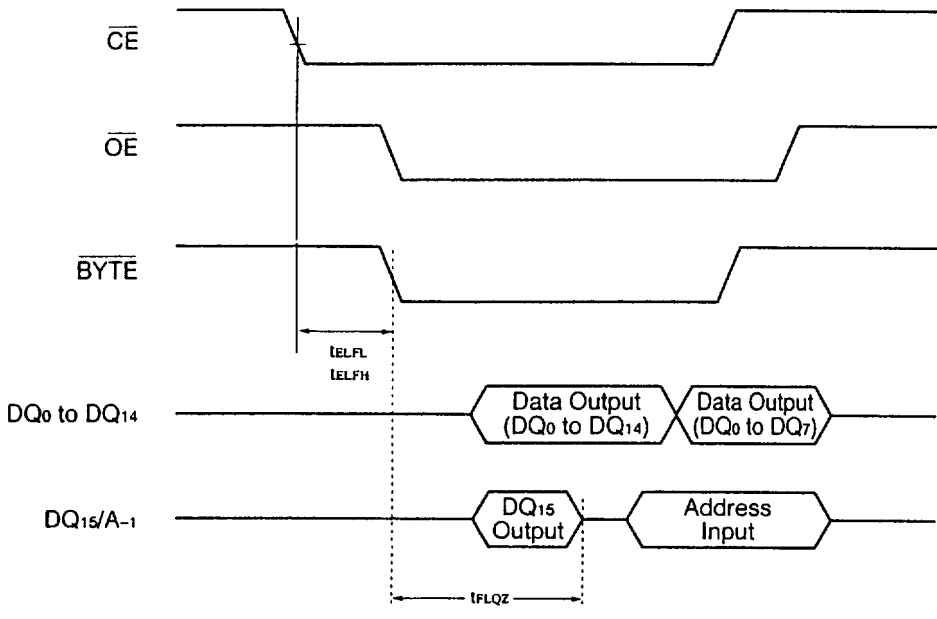
Figure 12 BYTE Timing Diagram for Read Operations

CE

OE

BYTE

tELFL
tELFH

DQ0 to DQ14

Data Output
(DQ0 to DQ14)

Data Output
(DQ0 to DQ7)

DQ15/A-1

DQ15
Output

Address
Input

tFLQZ
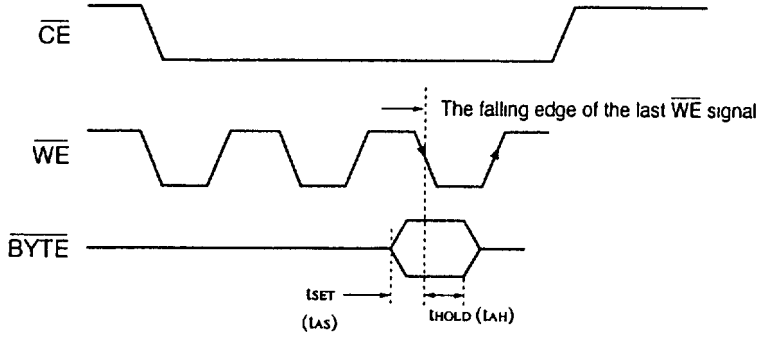
Figure 13 BYTE Timing Diagram for Write Operations

CE

WE

The falling edge of the last WE signal

BYTE

tSET
(tAS)

tHOLD (tAH)
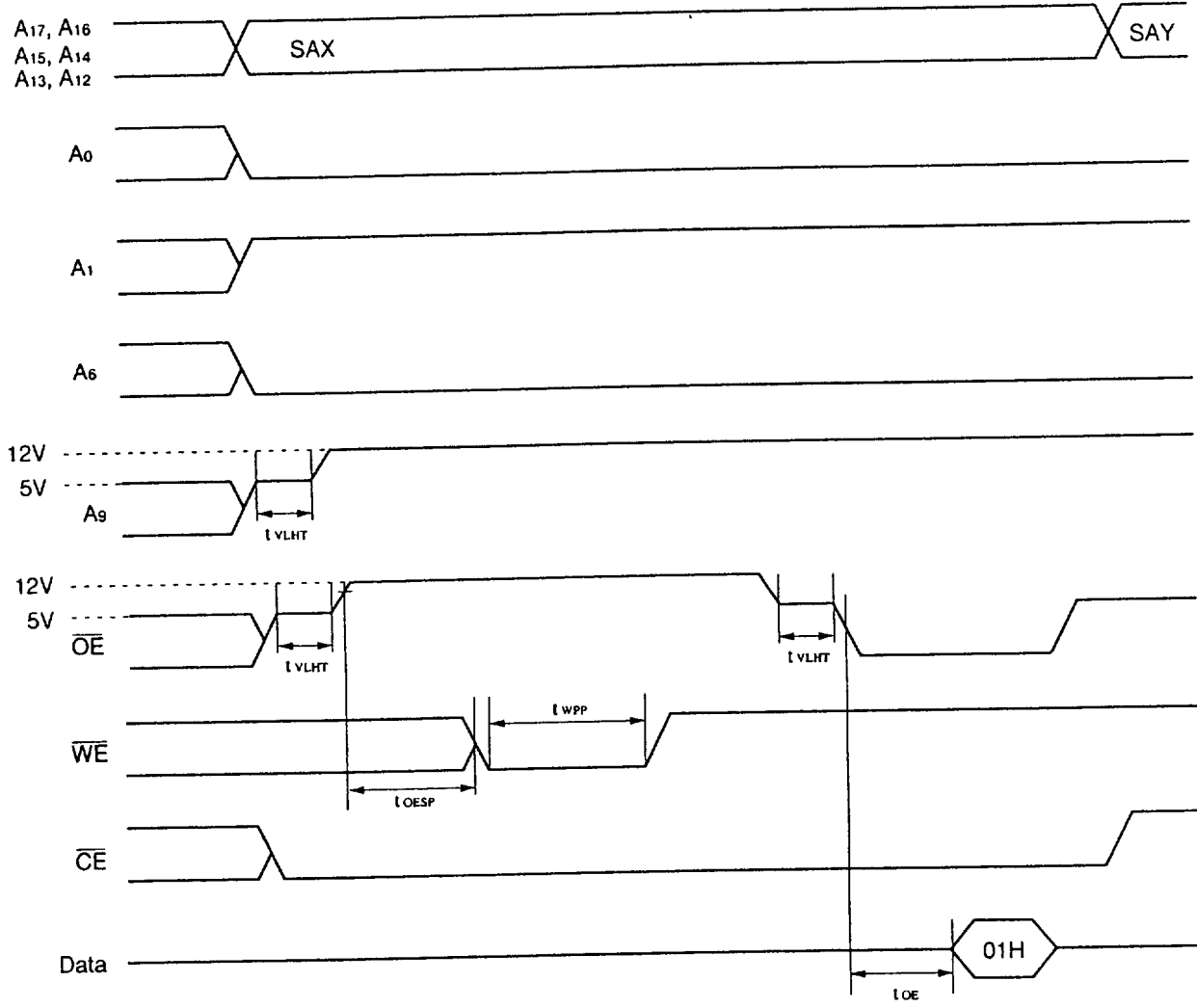
SAX = Sector Address for initial sector
SAY = Sector Address for next sector

Figure 14 AC Waveforms for Sector Protection
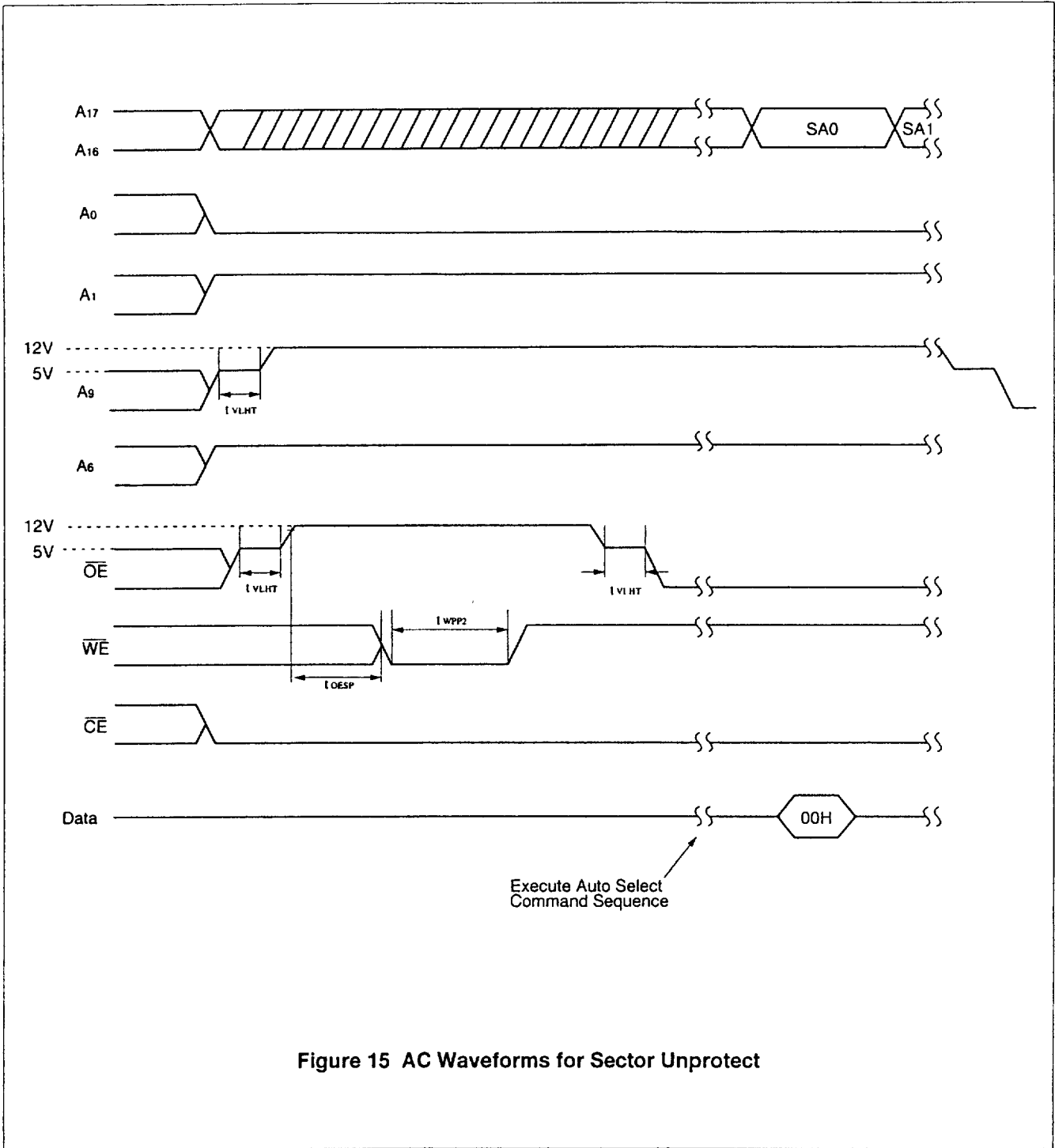
Figure 15 AC Waveforms for Sector Unprotect

EMBEDDED ALGORITHMS

```
                          ┌──────────┐
                          │  Start   │
                          └────┬─────┘
                               │
           ┌─────────────►┌────┴─────────────┐
           │              │Write Program Command│
           │              │   Sequence       │
           │              │  (See below)     │
           │              └────┬─────────────┘
           │                   │
           │              ┌────┴─────────────┐
           │              │Data Polling Device│
           │              └────┬─────────────┘
           │                   │
  ┌────────┴────────┐   No  ┌──┴──────┐
  │Increment Address│◄──────┤Last Address│
  └─────────────────┘       │    ?     │
                            └────┬─────┘
                               Yes│
                          ┌───────┴───────┐
                          │Programming Completed│
                          └───────────────┘
```

Program Command Sequence (Address/Command):

```
                    ┌──────────────┐
                    │  5555H/AAH   │
                    └──────┬───────┘
                           │
                    ┌──────┴───────┐
                    │  2AAAH/55H   │
                    └──────┬───────┘
                           │
                    ┌──────┴───────┐
                    │  5555H/A0H   │
                    └──────┬───────┘
                           │
              ┌────────────┴────────────┐
              │Program Address/Program Data│
              └─────────────────────────┘
```
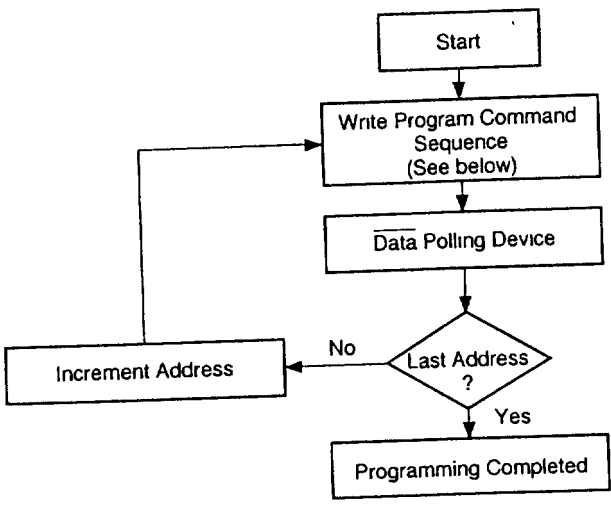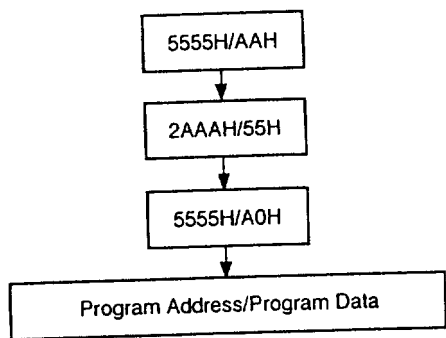
Figure 16 Embedded Programming Algorithm

Table 9 Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby*		
Write	Program	Valid Address/Data Sequence
Read		Data Polling to Verify Programming
Standby*		Compare Data Output to Data Expected

*Device is either powered-down, erase inhibit or program inhibit.

EMBEDDED ALGORITHMS

```
                    ┌──────────────┐
                    │    Start     │
                    └──────┬───────┘
                           ▼
              ┌────────────────────────┐
              │  Write Erase Command   │
              │       Sequece          │
              │     (See below)        │
              └────────────┬───────────┘
                           ▼
              ┌────────────────────────┐
              │  Data Polling or Toggle Bit │
              │  Successfully Completed │
              └────────────┬───────────┘
                           ▼
              ┌────────────────────────┐
              │   Erasure Completed    │
              └────────────────────────┘
```

Chip Erase Command Sequence
(Address/Command):

Individual Sector/Multiple Sector
Erase Command Sequence
(Address/Command):

```
   ┌──────────────┐          ┌──────────────┐
   │  5555H/AAH   │          │  5555H/AAH   │
   └──────┬───────┘          └──────┬───────┘
          ▼                         ▼
   ┌──────────────┐          ┌──────────────┐
   │  2AAAH/55H   │          │  2AAAH/55H   │
   └──────┬───────┘          └──────┬───────┘
          ▼                         ▼
   ┌──────────────┐          ┌──────────────┐
   │  5555H/80H   │          │  5555H/80H   │
   └──────┬───────┘          └──────┬───────┘
          ▼                         ▼
   ┌──────────────┐          ┌──────────────┐
   │  5555H/AAH   │          │  5555H/AAH   │
   └──────┬───────┘          └──────┬───────┘
          ▼                         ▼
   ┌──────────────┐          ┌──────────────┐
   │  2AAAH/55H   │          │  2AAAH/55H   │
   └──────┬───────┘          └──────┬───────┘
          ▼                         ▼
   ┌──────────────┐          ┌───────────────────┐
   │  5555H/10H   │          │ Sector Address/30H │
   └──────────────┘          └─────────┬─────────┘
                                        ▼
                             ┌───────────────────┐
                             │ Sector Address/30H │ ┐ Additional sector
                             └───────────────────┘ ├ erase commands
                                     ┊             │ are optional
                             ┌───────────────────┐ │
                             │ Sector Address/30H │ ┘
                             └───────────────────┘
```

Figure 17 Embedded Erase Algorithm

Table 10 Embedded Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby*		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby*		Compare Output to FFH

*Device is either powered-down, erase inhibit or program inhibit.

VA = Byte address for programming
= Any of the sector addresses
within the sector being erased
during sector erase operation
= XXXXH during chip erase
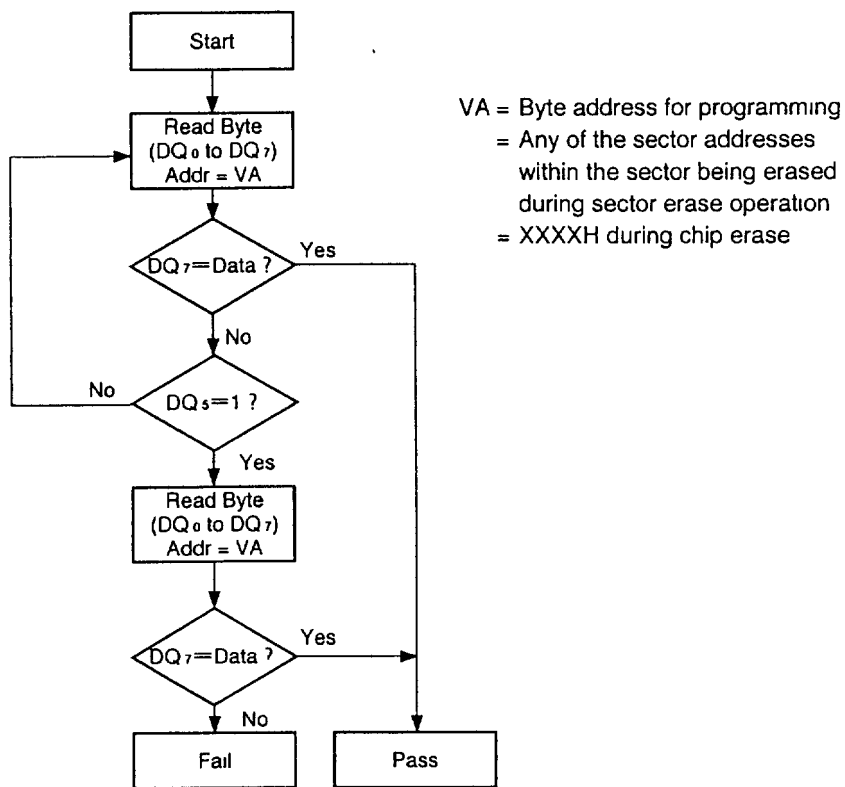
Note: DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 18 Data Polling Algorithm
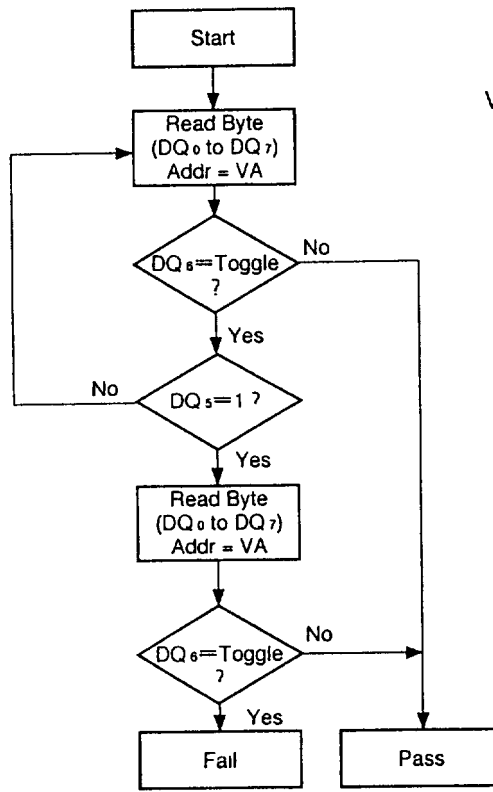
VA = Byte address for programming
  = Any of the sector addresses within the sector being erased during sector erase operation
  = XXXXH during chip erase
  = Any address not within the sector in the process of an Erase Suspend operation.

Note: DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 19 Toggle Bit Algorithm

```
                                    ┌─────────────────────┐
                                    │        Start        │
                                    └─────────────────────┘
                                              │
                                              ▼
                                    ┌─────────────────────┐
                                    │  Set Up Sector Addr │◄──────────┐
                                    │ (A17, A16, A15, A14,│           │
                                    │      A13, A12)      │           │
                                    └─────────────────────┘           │
                                              │                       │
                                              ▼                       │
                                    ┌─────────────────────┐           │
                                    │      PLSCNT = 1     │           │
                                    └─────────────────────┘           │
                                              │                       │
                                              ▼                       │
                                    ┌─────────────────────┐           │
                                    │ OE = V ID, A9 = V ID,│          │
                                    │   CE = V IL,        │           │
                                    │   RESET = V IH      │           │
                                    └─────────────────────┘           │
                                              │                       │
                                              ▼                       │
                                    ┌─────────────────────┐           │
                                    │   Activate WE Pulse │           │
                                    └─────────────────────┘           │
                                              │                       │
                                              ▼                       │
                                    ┌─────────────────────┐           │
                                    │   Time out 100 μs   │           │
                ┌─────────────────┐ └─────────────────────┘           │
                │ Increment PLSCNT│           │                       │
                └─────────────────┘           ▼                       │
                         ▲          ┌─────────────────────┐           │
                         │          │   Power Down OE     │           │
                         │          │ WE = V IH, CE = OE  │           │
                         │          │     = V IL          │           │
                         │          │ A9 should remain V ID│          │
                         │          └─────────────────────┘           │
                         │                    │                       │
                         │                    ▼                       │
                         │          ┌─────────────────────┐           │
                         │          │   Read from Sector  │           │
                         │          │ Addr = SA, A1A0 = 10,│          │
                         │          │       A6 = 0        │           │
                         │          └─────────────────────┘           │
                    No   │                    │                       │
                         │                    ▼                       │
              ◄─────────◇           No  ◇─────────────◇               │
              │ PLSCNT = 25 ?│◄─────────│  Data = 01H ?│              │
              ◇─────────────◇           ◇─────────────◇               │
                    │ Yes                      │ Yes                  │
                    ▼                          ▼              Yes     │
          ┌─────────────────┐        ◇─────────────────────◇─────────┘
          │  Device Failed  │        │ Protect Another Sector?│
          └─────────────────┘        ◇─────────────────────◇
                                              │ No
                                              ▼
                                    ┌─────────────────────┐
                                    │ Remove V ID from A9 │
                                    │ Write Reset Command │
                                    └─────────────────────┘
                                              │
                                              ▼
                                    ┌─────────────────────┐
                                    │  Sector Protection  │
                                    │     Completed       │
                                    └─────────────────────┘
```

Figure 20 Sector Protection Algorithm

Notes:
SA0 = Sector Address for initial sector
SA10 = Sector Address for last sector
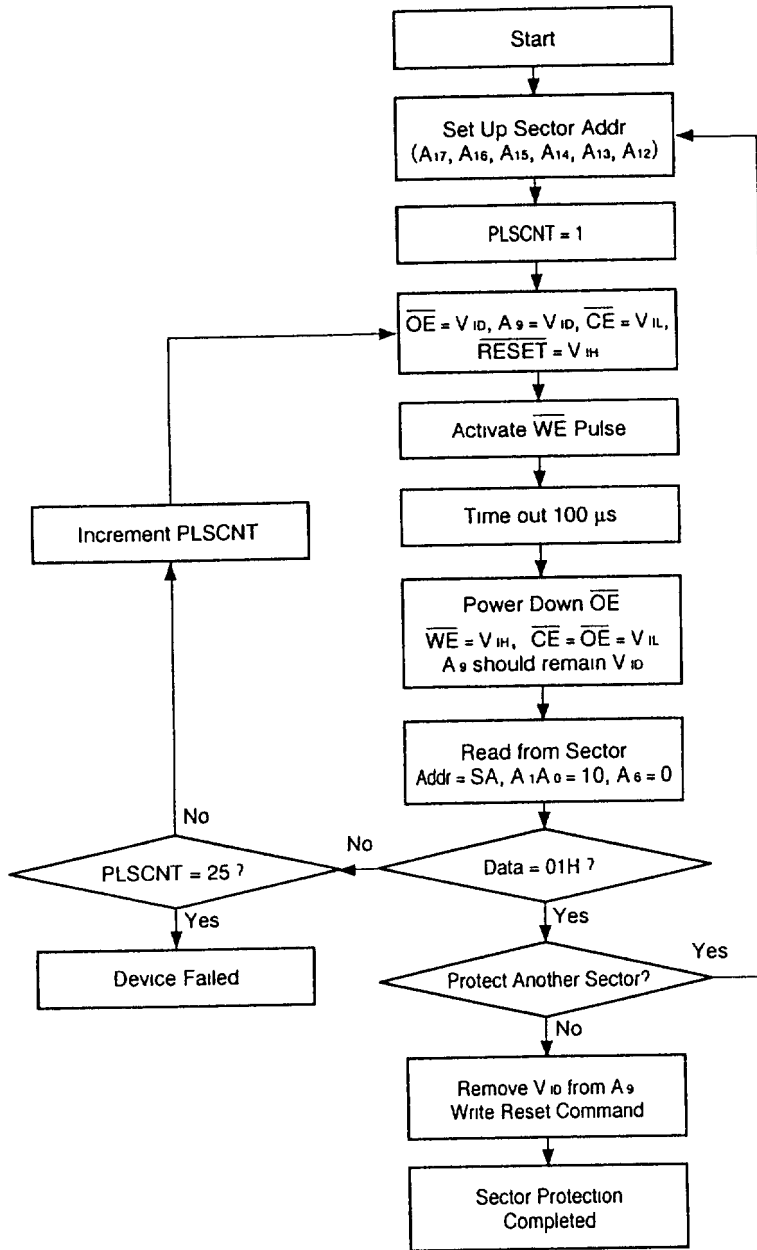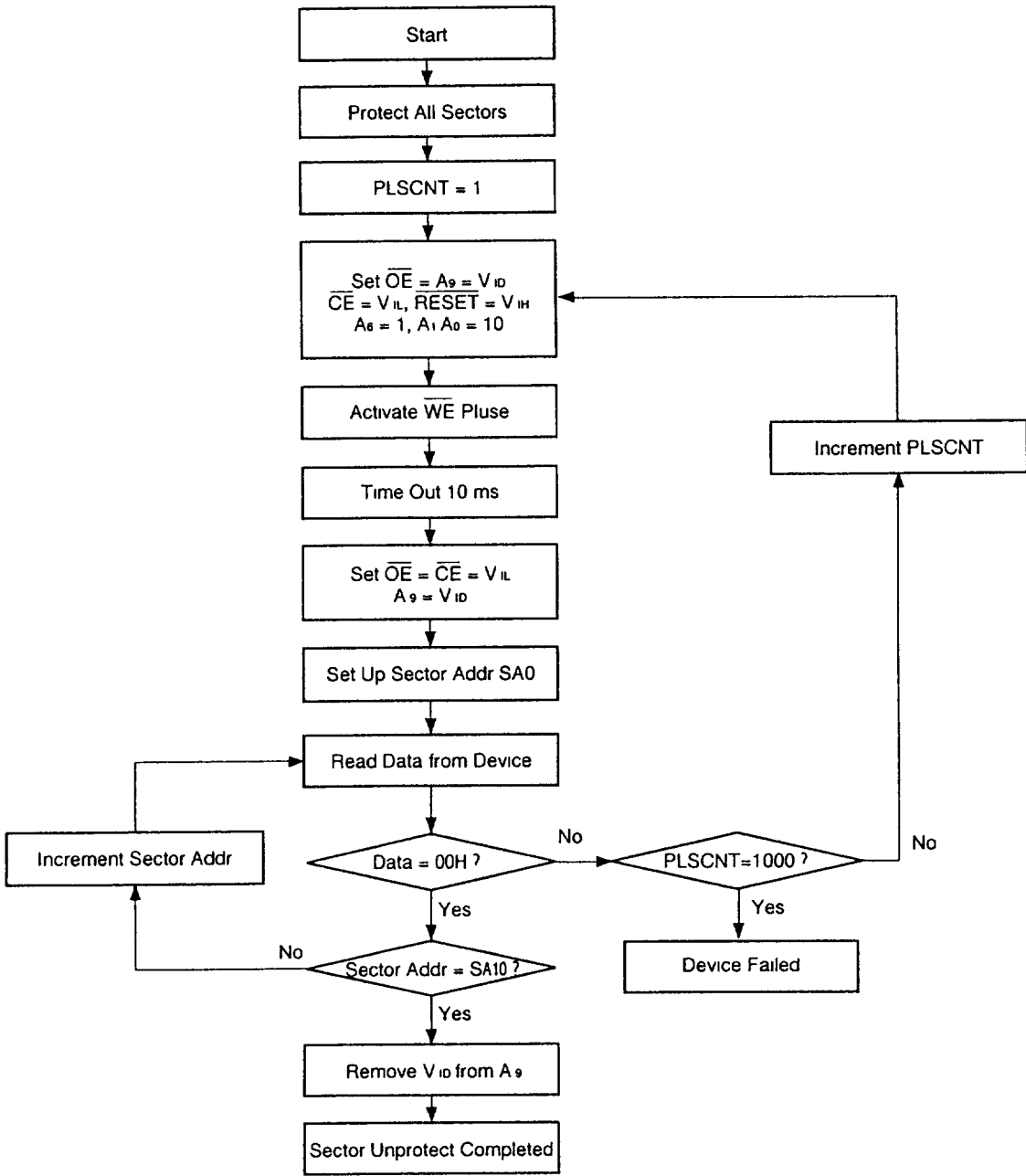Please refer to Table 4 for details.

Figure 21 Sector Unprotect Algorithm

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip and Sector Erase Time	—	1.5 (Note 1)	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time	—	16	1000 (Note 2)	µs	Excludes system-level overhead
Chip Programming Time	—	8.5 (Note 1)	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	1,000,000	—	Cycles	

Notes:
1. 25°C, 5V Vcc, 100,000 cycles
2. The Embedded Algorithms allow for 48 ms byte program time.

■ LATCHUP CHARACTERISTICS

Description	Min.	Max.
Input Voltage with respect to Vss on all I/O pins	– 1.0V	Vcc + 1.0V
Vcc Current	– 100 mA	+ 100 mA

Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.

■ TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0	6	7.5	pF
COUT	Output Capacitance	VOUT = 0	8.5	12	pF
CIN2	Control Pin Capacitance	VIN = 0	8	10	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz

■ SOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	10	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, $f = 1.0$ MHz

■ DATA RETENTION

Parameter	Test Conditions	Min.	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

MBM29F400TA/400BA

■ PACKAGE DIMENSIONS

(Suffix: PFN)
(FPT-44P-M16)

*[1] Resin Protrusin.(Each Side 0 15(006)MAX)
*[2] Resin Protrusin:(Each Side 0 38(015)MAX)

*[1] 28 20±0 20(1 110± 008)

23

44

2 80(110)MAX
(MOUNTING HEIGHT)

0 80±0 20
(031± 008)

*[2]13 30±0.20   16 00±0 30
(524± 008)   (630± 012)

INDEX

0 15 -0 05 -0 05
(006± 002)

LEAD No ①

22

1 27(050)NOM

△ 0 10(004)   0 40 -0 10 -0 05 (016 -004 -002)   ⊕ ∅0.10(004) ⓜ   0 225±0 125 (.009± 005) (STAND OFF)

© 1994 FUJITSU LIMITED F44022S-1C-1   inches : mm (inches)

(Suffix: PFTN)
(FPT-48P-M19)

* Resin Protrusin (Each Side 0 15(006)MAX)

1 20(047)   (MOUNTING HEIGHT)
MAX
1 00±0 05
(039± 002)

LEAD No ①

48

INDEX

0 22±0 05
(009± 002)   ⊕ 0 08(003) ⓜ

* 12.00±0.10
(472±.004)

0 50(020)
TYP

24

25

0 10±0 05
(004± 002)   (STAND OFF)

20 00±0 20(787± 008)

* 18 40±0 10(724± 004)

0 155±0 055
(006± 002)

△ 0 10(004)   0 60±0.10
(024± 004)

© 1994 FUJITSU LIMITED F48031S-1C-1   inches : mm (inches)

(Suffix: PFTR)
(FPT-48P-M20)

* Resin Protrusin (Each Side 0.15(006)MAX)

1 20(047) (MOUNTING HEIGHT)
MAX

1 00±0 05
(.039± 002)

LEAD No ① 48

INDEX

* 12 00±0 10
(472± 004)

0 22±0 05
(.009± 002) ⊕ 0 08(003) Ⓜ

0 50(020)
TYP

24 25

0 10±0 05 (STAND OFF)
(004± 002)

20 00±0 20(787± 008)

* 18 40±0 10(724±.004)

0 155±0 055
(006± 002)

△ 0 10(004)

0 60±0 10
(.024± 004)
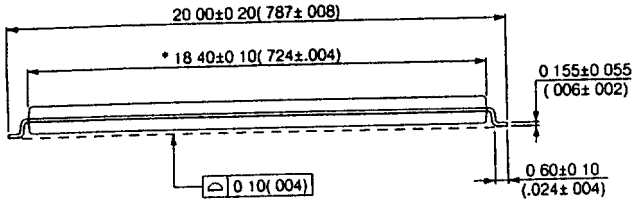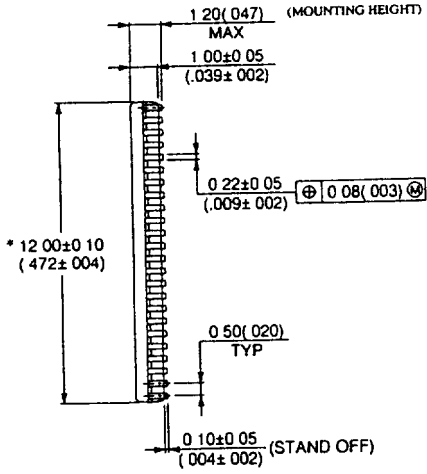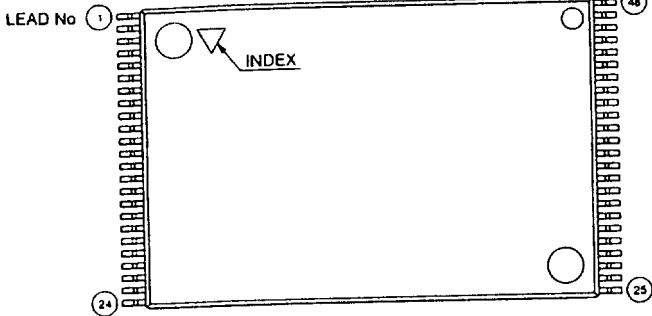
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inches : mm (inches)

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