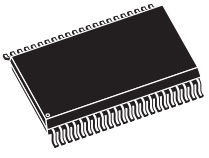
M59PW1282

128Mbit (two 64Mb, x16, Uniform Block, LightFlash™) 3V Supply, Multiple Memory Product

FEATURES SUMMARY

- MASK-ROM PIN-OUT COMPATIBLE
- TWO 64 Mbit LightFlash™ MEMORIES STACKED IN A SINGLE PACKAGE
- SUPPLY VOLTAGE
  - V_{CC} = 2.7 to 3.6V for Read
  - V_{PP} = 11.4 to 12.6V for Program and Erase
- ACCESS TIME
  - 90ns at V_{CC} = 3.0 to 3.6V
  - 100, 120ns at V_{CC} = 2.7 to 3.6V
- PROGRAMMING TIME
  - 9µs per Word typical
  - Multiple Word Programming Option (16s typical Chip Program)
- ERASE TIME
  - 85s typical Chip Erase
- UNIFORM BLOCKS
  - 64 blocks of 2 Mbits
- PROGRAM/ERASE CONTROLLER
  - Embedded Word Program algorithms
- 10,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code : 88A8h

Figure 1. Package



SO44 (M)

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SUMMARY DESCRIPTION

The M59PW1282 is a 128Mbit (8Mb x16), Mask-ROM pinout compatible, non-volatile LightFlash™ memory, that can be read, erased and reprogrammed. Read operations can be performed using a single low voltage (2.7 to 3.6V) supply. Program and Erase operations require an additional V_{PP} (11.4 to 12.6V) power supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The Mask-ROM compatibility is obtained using a dual function Address/Voltage Supply pin (A22/V_{PP}). In Read mode the A22/V_{PP} pin works as an address pin; in Program or Erase mode it also works as a voltage supply pin. At the beginning of any program or erase operation, a specific procedure (see Figure 4) must be performed to internally memorize the A22 value that will be used during the program or erase operation.

The device is composed of two 64Mbit memories stacked in a single package. Recommended operating conditions do not allow both memories to be active at the same time. Address A22 selects the memory to be enabled. The other memory is in Standby mode.

The memory is divided into 64 uniform blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller (P/E.C.) simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The M59PW1282 features an innovative command, Multiple Word Program, that is used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written to the memory at any one time. Using this command the entire memory can be programmed in 16s, compared to 72s using the standard Word Program.

The end of a Program or Erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards. Chip Enable and Output Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in SO44 package and is supplied with all the bits set to '1').

Figure 2. Logic Diagram

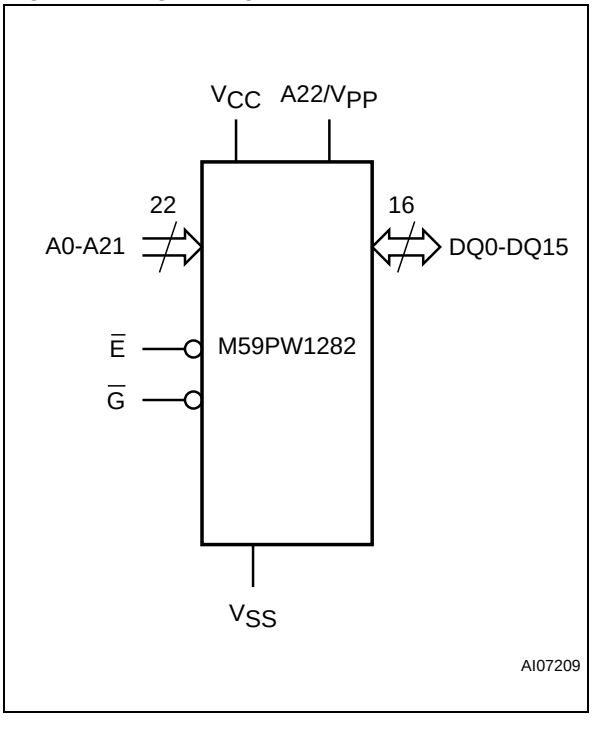


Table 1. Signal Names

A0-A21	Address Inputs
A22/V_{PP}	Address Input/Supply Voltage for Program/Erase
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage read
V_{SS}	Ground

Figure 3. SO Connections

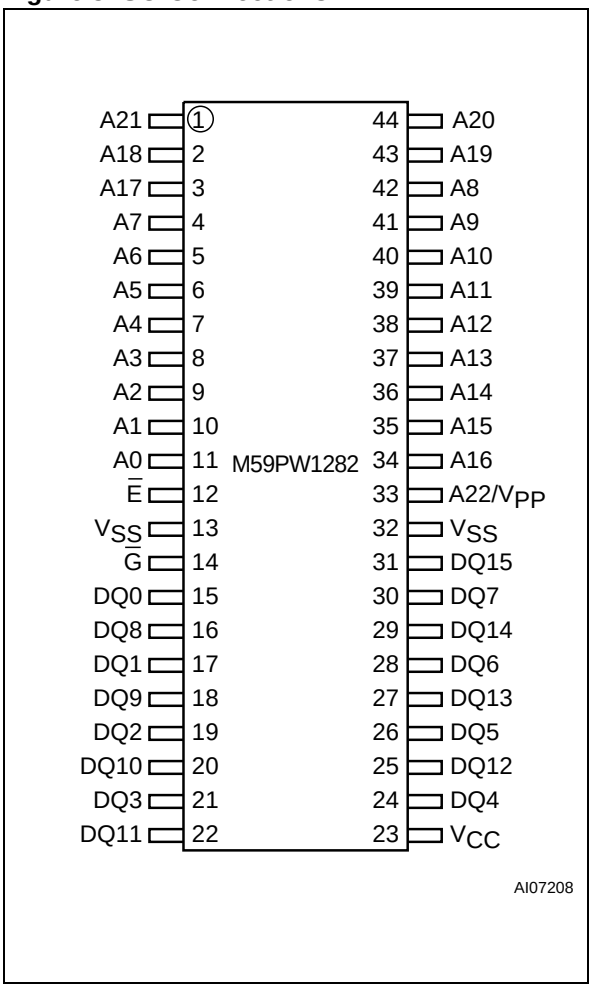


Table 2. Block Addresses

Block Number	Address Range
64	7E0000h-7FFFFFh
63	7C0000h-7DFFFFh
62	7A0000h-7BFFFFh
61	780000h-79FFFFh
60	760000h-77FFFFh
59	740000h-75FFFFh
58	720000h-73FFFFh
57	700000h-71FFFFh
56	6E0000h-6FFFFFh
55	6C0000h-6DFFFFh
54	6A0000h-6BFFFFh
53	680000h-69FFFFh
52	660000h-67FFFFh
51	640000h-65FFFFh
50	620000h-63FFFFh
49	600000h-61FFFFh
48	5E0000h-5FFFFFh
47	5C0000h-5DFFFFh
46	5A0000h-5BFFFFh
45	580000h-59FFFFh
44	560000h-57FFFFh
43	540000h-55FFFFh
42	520000h-53FFFFh
41	500000h-51FFFFh
40	4E0000h-4FFFFFh
39	4C0000h-4DFFFFh
38	4A0000h-4BFFFFh
37	480000h-49FFFFh
36	460000h-47FFFFh
35	440000h-45FFFFh
34	420000h-43FFFFh
33	400000h-41FFFFh
32	3E0000h-3FFFFFh
31	3C0000h-3DFFFFh
30	3A0000h-3BFFFFh
29	380000h-39FFFFh
28	360000h-37FFFFh
27	340000h-35FFFFh
26	320000h-33FFFFh
25	300000h-31FFFFh
24	2E0000h-2FFFFFh
23	2C0000h-2DFFFFh
22	2A0000h-2BFFFFh
21	280000h-29FFFFh
20	260000h-27FFFFh
19	240000h-25FFFFh
18	220000h-23FFFFh
17	200000h-21FFFFh
16	1E0000h-1FFFFFh
15	1C0000h-1DFFFFh
14	1A0000h-1BFFFFh
13	180000h-19FFFFh
12	160000h-17FFFFh
11	140000h-15FFFFh
10	120000h-13FFFFh
9	100000h-11FFFFh
8	0E0000h-0FFFFFh
7	0C0000h-0DFFFFh
6	0A0000h-0BFFFFh
5	080000h-09FFFFh
4	060000h-07FFFFh
3	040000h-05FFFFh
2	020000h-03FFFFh
1	000000h-01FFFFh

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A21). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

Address/Voltage Supply (A22/V_{PP}). The A22/V_{PP} signal has two functions.

During read operations the A22/V_{PP} signal works as an address input, which is used to select the Top (A22 = V_{IH}) or Bottom (A22 = V_{IL}) die.

During program or erase operations it also works as a V_{PP} voltage supply pin. At the beginning of any program or erase operation, a specific procedure (see Figure 4) must be performed to internally memorize the A22 value that will be used during the program or erase operation.

When the V_{PP} is in the V_{HH} range (see Table 12, DC Characteristic, for the relevant values) program and erase operations are enabled. During such operations V_{PP} must be stable in the V_{HH} range. Program and erase operation are not allowed when V_{PP} is below the V_{HH} range.

Data Inputs/Outputs (DQ0-DQ7). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the command sent to the Command Interface of the Program/Erase Controller. When reading the Status Register they report the status of the ongoing algorithm.

Data Inputs/Outputs (DQ8-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations the Command Interface does not use these bits. When reading the Status Register these bits should be ignored.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read operations to be performed. It also controls the Bus Write operations, when V_{PP} is in the V_{HH} range.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operations of the memory. It also allows Bus Write operations, when V_{PP} is in the V_{HH} range.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for Read operations.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program operations, I_{CC3}.

Vss Ground. The V_{SS} Ground is the reference for all voltage measurements.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Electronic Signature. See Tables 3, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs and applying a Low signal, V_{IL}, to Chip Enable and Output Enable. The Data Inputs/Outputs will output the value, see Figure 12, Read AC Waveforms, and Table 12, Read AC Characteristics, for details of when the output becomes valid.

During read array operations A22 selects Top (A22 = V_{IH}) or Bottom (A22 = V_{IL}) die.

Bus Write. Bus Write operations write to the Command Interface. Bus Write is enabled only when V_{PP} is set to V_{HH}. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figure 12, Write AC Waveforms, and Table 14, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 12, DC Characteristics.

During program operation the memory will continue to use the Program Supply Current, I_{CC3}, for Program operation until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Tables 3, Bus Operations, once the Auto Select Command is executed. To exit Electronic Signature mode, the Read/Reset command must be issued.

Table 3. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	A22/V_{PP}(2)	Address Inputs A0-A21	Data Inputs/Outputs DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IL}/V_{IH}(3)	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{HH}(4)	Command Address	Data Input
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{HH}	A0 = V_{IL}, A1 = V_{IL}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{HH}	A0 = V_{IH}, A1 = V_{IL}, Others V_{IL} or V_{IH}	88AAh

Note: 1. X = V_{IL} or V_{IH}.
2. When reading the Status Register during a program operation A22/V_{PP} must be kept at V_{HH}.
3. V_{IL} enables the Bottom die, V_{IH} enables the Top die during read array operation.
4. V_{HH} after latching A22 at V_{IL} or V_{IH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

Refer to Tables 4 and 5, for a summary of the commands.

As the device contains two internal memories care must be taken to issue the commands to the correct address. To select the Top die (A22 = V_{IH}) or the Bottom die (A22 = V_{IL}) the A22 latch procedure (see Figure 4) must be followed.

It is not necessary to repeat the A22 latch procedure if all the commands are issued to the same die, unless the power supply V_{CC} is switched off.

Read/Reset Command.

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

V_{PP} must be set to V_{HH} during the Read/Reset command. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored. The command can be issued, between Bus Write cycles before the start of a program operation, to return the device to read mode. Once the program operation has started the Read/Reset command is no longer accepted.

Auto Select Command.

The Auto Select command is used to read the Manufacturer Code and the Device Code. V_{PP} must be set to V_{HH} during the Auto Select command. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued, all other commands are ignored.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

Word Program Command.

The Word Program command can be used to program a Word to the memory array. V_{PP} must be set to V_{HH} during Word Program. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the P/E.C.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'.

Multiple Word Program Command

The Multiple Word Program command can be used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written in the memory at once. V_{PP} must be set to V_{HH} during Multiple Word Program. If V_{PP} is set either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read mode.

It has four phases: the Setup Phase to initiate the command, the Program Phase to program the data to the memory, the Verify Phase to check that the data has been correctly programmed and reprogram if necessary and the Exit Phase.

Setup Phase. The Multiple Word Program command requires three Bus Write operations to initiate the command (refer to Table 4, Multiple Word Program Command and Figure 8, Multiple Word Program Flowchart).

The Status Register must be read in order to check that the P/E.C. has started (see Table 8 and Figure 8).

Program Phase. The Program Phase requires n+1 Bus Write operations, where n is the number of Words, to execute the programming phase (refer to Table 5, Multiple Word Program and Figure 7, Multiple Word Program Flowchart).

Before any Bus Write operation of the Program Phase, the Status Register must be read in order to check that the P/E.C. is ready to accept the operation (see Table 8 and Figure 8).

The Program Phase is executed in three different sub-phases:

1. The first Bus Write operation of the Program Phase (the 4th of the command) latches the

Start Address and the first Word to be programmed.

2. Each subsequent Bus Write operation latches the next Word to be programmed and automatically increments the internal Address Bus. It is not necessary to provide the address of the location to be programmed but only a Continue Address, CA (A17 to A21 equal to the Start Address), that indicates to the PC that the Program Phase has to continue. A0 to A16 are 'don't care'.
3. Finally, after all Words have been programmed, a Bus Write operation (the $(n+1)^{th}$) with a Final Address, FA (A17 or a higher address pin different from the Start Address), ends the Program Phase.

The memory is now set to enter the Verify Phase.

Verify Phase. The Verify Phase is similar to the Program Phase in that all Words must be resent to the memory for them to be checked against the programmed data.

Before any Bus Write Operation of the Verify Phase, the Status Register must be read in order to check that the P/E.C. is ready for the next operation or if the reprogram of the location has failed (see Table 8 and Figure 8).

Three successive steps are required to execute the Verify Phase of the command:

1. The first Bus Write operation of the Verify Phase latches the Start Address and the Word to be verified.
2. Each subsequent Bus Write operation latches the next Word to be verified and automatically increments the internal Address Bus. As in the Program Phase, it is not necessary to provide the address of the location to be programmed but only a Continue Address, CA (A17 to A21 equal to the Start Address).
3. Finally, after all Words have been verified, a Bus Write cycle with a Final Address, FA (A17 or a higher address pin different from the Start Address) ends the Verify Phase.

Exit Phase. After the Verify Phase ends, the Status Register must be read to check if the command has successfully completed or not (see Table 8 and Figure 8).

If the Verify Phase accomplishes successfully, the memory returns to the Read mode and DQ6 stops toggling.

On the contrary, if the P/E.C. fails to reprogram a given location, the Verify Phase terminates, DQ6 continues toggling and error bit DQ5 is set in the Status Register. If the error is due to a V_{PP} failure DQ4 is also set.

When the operation fails a Read/Reset command must be issued to return the device to Read mode.

During the Multiple Word Program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

Note that the Multiple Word Program command cannot change a bit set at '0' back to '1'.

Block Erase Command.

The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost.

V_{PP} must be set to V_{HH} during Block Erase. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode.

Six Bus Write operations are required to select the block . The Block Erase operation starts the P/E.C. after the last Bus Write operation. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the P/E.C. has started the Block Erase operation.

During the Block Erase operation the memory will ignore all commands. Typical block erase times are given in Table 6. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Chip Erase Command.

The Chip Erase command can be used to erase the entire memory. It sets all of the bits in the memory to '1'. All previous data in the memory is lost.

V_{PP} must be set to V_{HH} during Chip Erase. If V_{PP} is set to either V_{IL} or V_{IH} the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode. Six Bus Write operations are required to issue the Chip Erase Command and start the P/E.C.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 6. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

Table 4. Standard Commands

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Word Program	4	555	AA	2AA	55	555	A0	PA	PD				
Block Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A0-A10 and DQ0-DQ7 to verify the commands; A11-A21, DQ8-DQ15 are Don't Care.

Table 5. Multiple Word Program Command

Phase	Length	Bus Write Operations													
		1st		2nd		3rd		4th		5th		nth		Final	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Set-Up	3	555	AA	2AA	55	555	20								
Program	n+1	SA	PD1	CA	PD2	CA	PD3	CA	PD4	CA	PD5	CA	PAn	FA	X
Verify	n+1	SA	PD1	CA	PD2	CA	PD3	CA	PD4	CA	PD5	CA	PAn	FA	X

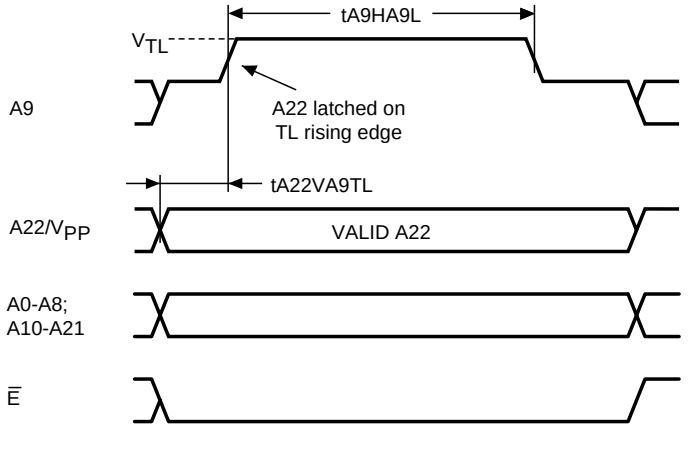
Note: A Bus Read must be done between each Write cycle where the data is programmed or verified, to Read the Status Register and check that the memory is ready to accept the next data. SA is the Start Address. CA is the Continue Address. FA is the Final Address. X Don't Care, n = number of Words to be programmed.

Table 6. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1)	Typical after 10k W/E Cycles (1)	Max	Unit
Chip Erase		80	85	120	s
Block Erase (128 KWords)		1.5		6	s
Program (Word)		9		200	µs
Chip Program (Multiple Word)		16		280	s
Chip Program (Word by Word)		72		280	s
Program/Erase Cycles (per Block)	10,000				cycles

Note: 1. T_A = 25°C, V_{PP} = 12V.

Figure 4. A22 Latch Procedure Waveforms



Note: $\overline{G} = V_{IH}$; DQ0–DQ15 are Don't care; $V_{TL} = 10.5 \pm 0.25V$; $V_{CC} = 2.7$ to $3.6V$.

Table 7. A22 Latch Procedure AC Characteristics

Symbol	Parameter	Min	Unit
$t_{A22VA9TL}$	A22 valid to A9 at Third Level	1	µs
t_{A9HA9L}	A9 High to A9 Low	1	µs

Figure 5. Programming Flowchart

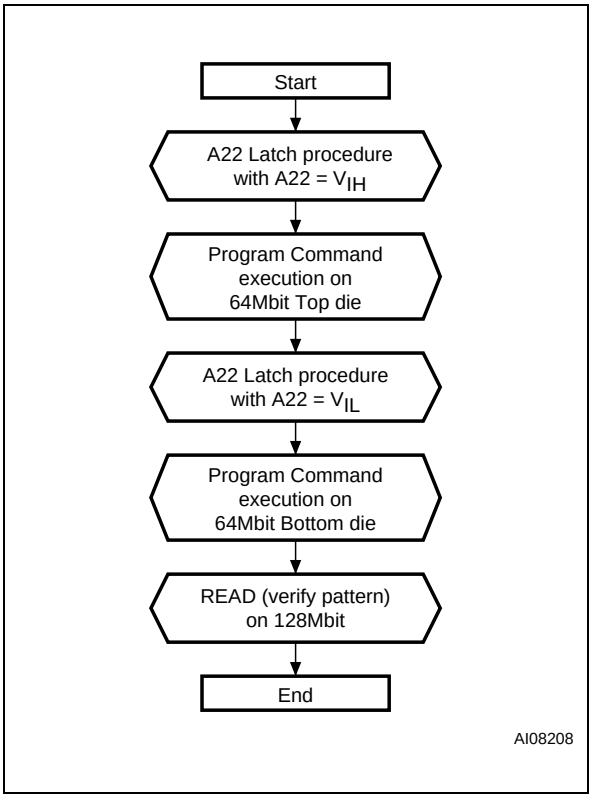


Figure 6. Chip Erase Flowchart

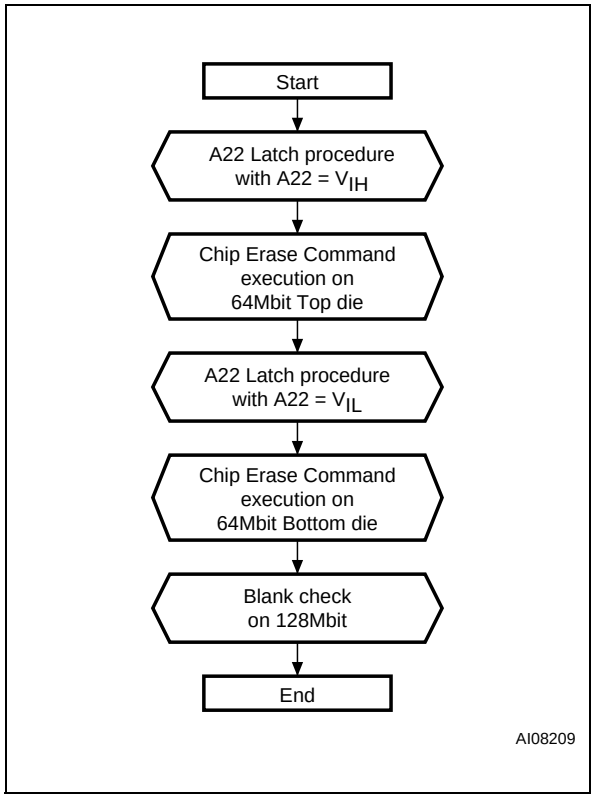
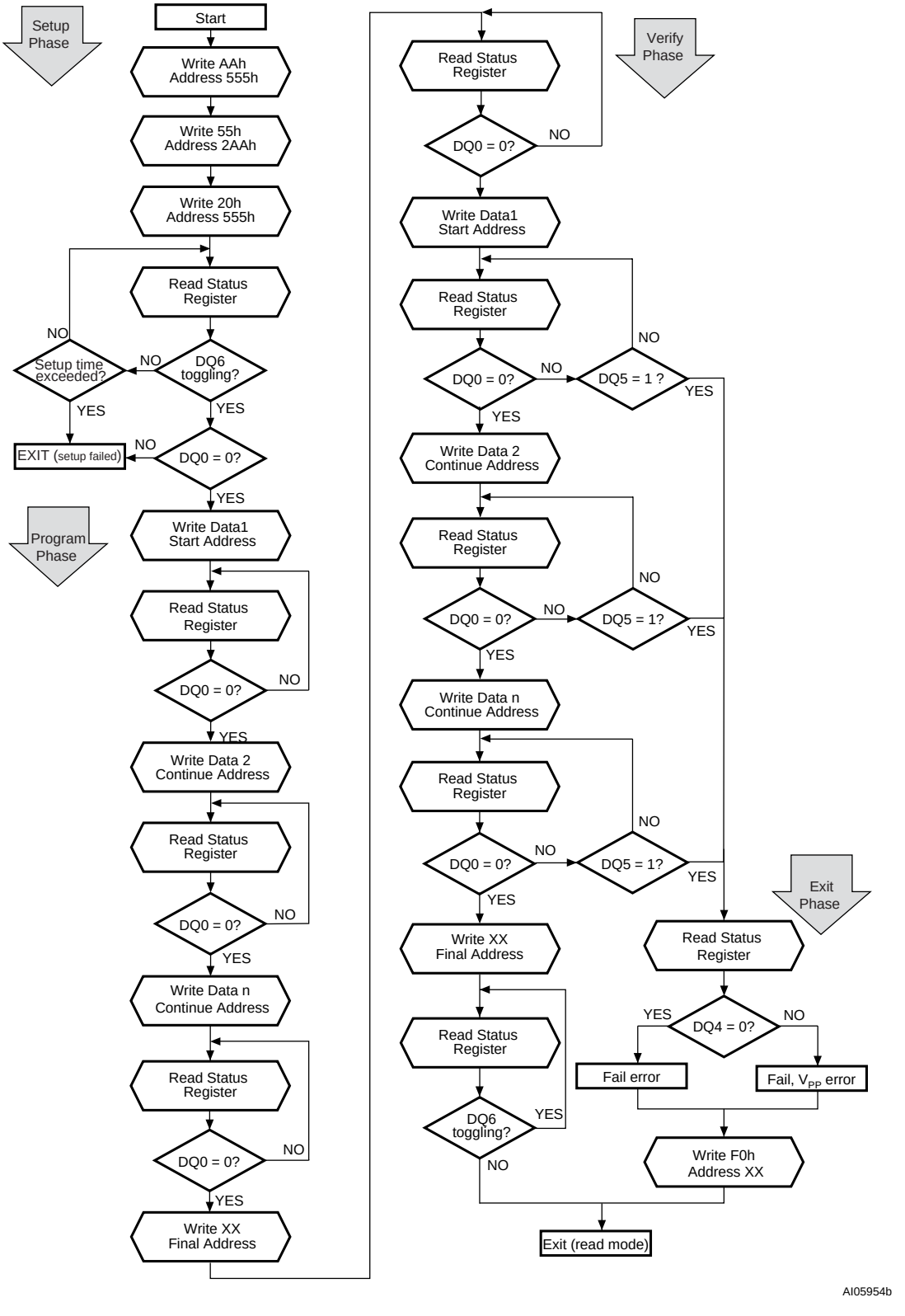


Figure 7. Multiple Word Program Flowchart for 64Mbit Top and Bottom Die



STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations. The bits in the Status Register are summarized in Table 8, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the P/E.C. has successfully completed its operation. The Data Polling Bit is output on DQ7 when the Status Register is read.

During a Word Program operation the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Word Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

Figure 8, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the P/E.C. has successfully completed its operation. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

Figure 9, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the P/E.C. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

V_{PP} Status Bit (DQ4). The V_{PP} Status Bit can be used to identify if any Program or Erase operation has failed due to a V_{PP} error. If V_{PP} falls below V_{HH} during any Program or Erase operation, the operation aborts and DQ4 is set to '1'. If V_{PP} remains at V_{HH} throughout the Program or Erase operation, the operation completes and DQ4 is set to '0'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of P/E.C. operation during a Block Erase command. Once the P/E.C. starts erasing the Erase Timer Bit is set to '1'. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the P/E.C. during Block Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the block being erased. Once the operation completes the memory returns to Read mode.

After an Erase operation that causes the Error Bit to be set, the Alternative Toggle Bit can be used to identify where the error occurred. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within a block that has not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Multiple Word Program Bit (DQ0). The Multiple Word Program Bit can be used to indicate whether the P/E.C. is active or inactive during Multiple Word Program. When the P/E.C. has written one Word and is ready to accept the next Word, the bit is set to '0'.

Status Register Bit DQ1 is reserved.

Table 8. Status Register Bits

Command (1)	P/E.C. Status	Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ0
Multiple Word Program	Programming	–	–	Toggle	0	–	0	–	1
	Waiting for data	–	–	Toggle	0	–	0	–	0
	Program fail	–	–	Toggle	1	(2)	0	–	1
Word Program	Programming	–	$\overline{DQ7}$	Toggle	0	–	0	–	–
	Program error	–	$\overline{DQ7}$	Toggle	1	(2)	0	–	–
Chip Erase/ Block Erase	Erasing	In erasing block	0	Toggle	0	–	1	Toggle	–
		Not in erasing block	0	Toggle	0	–	1	No Toggle	–
	Erase fail	In failed block	0	Toggle	1	(2)	1	Toggle	–
		Not in failed block	0	Toggle	1	(2)	1	No Toggle	–

Note: 1. Unspecified data bits should be ignored.
2. DQ4 = 0 if $V_{PP} \geq V_{HH}$ during Program/Erase algorithm execution; DQ4 = 1 if $V_{PP} < V_{HH}$ during Program/Erase algorithm execution.

Figure 8. Data Polling Flowchart

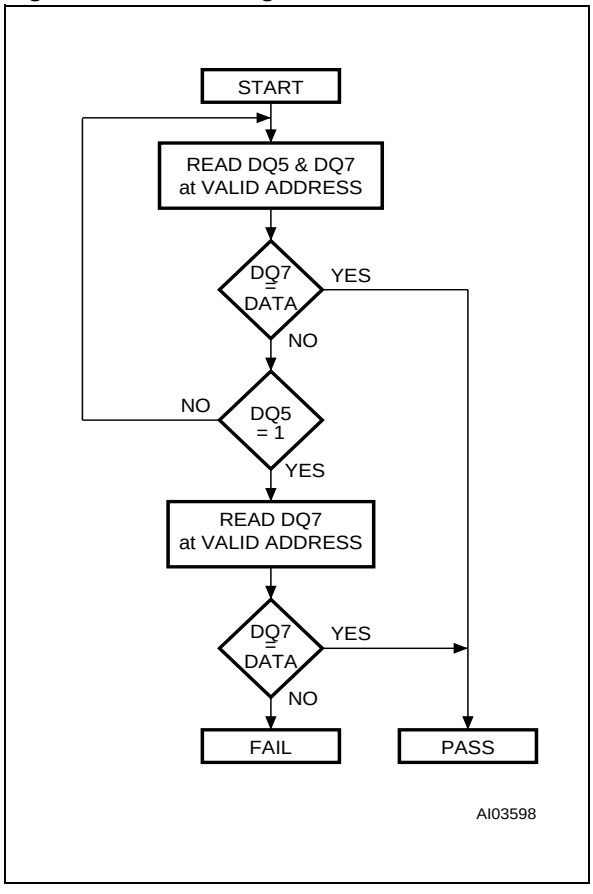
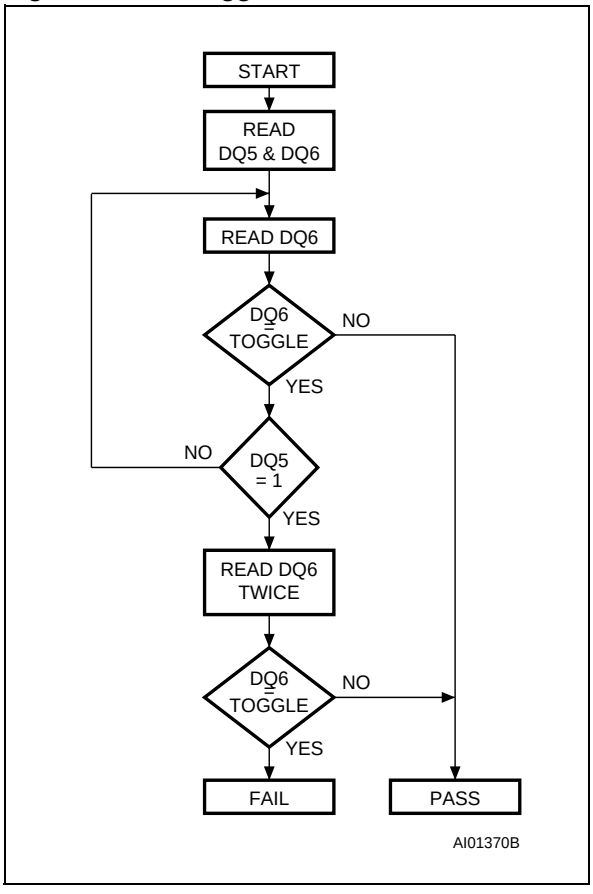


Figure 9. Data Toggle Flowchart



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage (1,2)	–0.6	V_{CC} +0.6	V
V_{CC}	Read Supply Voltage	–0.6	4	V
V_{PP}	Program/Erase Supply Voltage (3)	–0.6	13.5	V

Note: 1. Minimum voltage may undershoot to –2V for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V for less than 20ns during transitions.
3. Maximum voltage may overshoot to 14.0V for less than 20ns during transitions. V_{PP} must not remain at V_{HH} for more than a total of 80hrs.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 10, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 10. Operating and AC Measurement Conditions

Parameter	M59PW1282		Unit
	100, 120		
	Min	Max	
V_{CC} Read Supply Voltage	2.7	3.6	V
V_{PP} Program/Erase Supply Voltage	11.4	12.6	V
Ambient Operating Temperature (T_A)	0	70	°C
Load Capacitance (C_L)	30		pF
Input Rise and Fall Times		10	ns
Input Pulse Voltages	0 to 3		V
Input and Output Timing Ref. Voltages	1.5		V

Figure 10. AC Measurement I/O Waveform

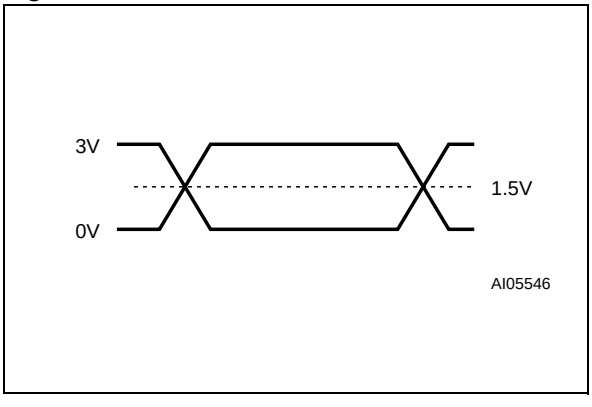


Figure 11. AC Measurement Load Circuit

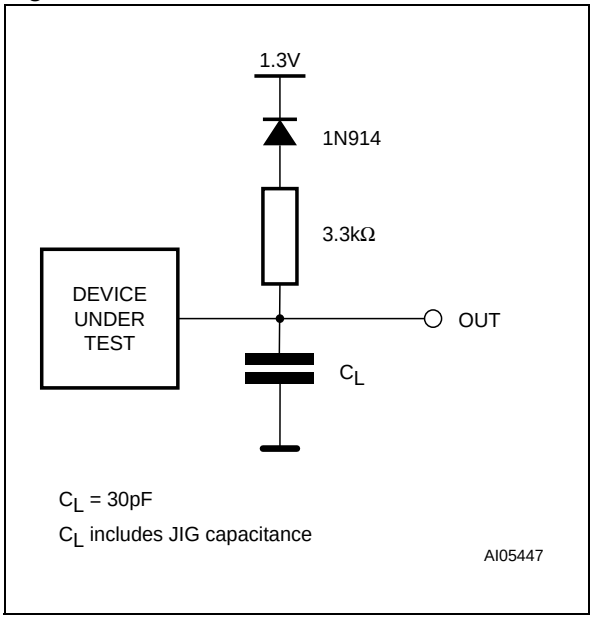


Table 11. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		24	pF
$C_{A22/Vpp}$	A22/V_{PP} Capacitance	$V_{A22/Vpp}$ = 0V		50	pF

Note: Sampled only, not 100% tested.

Table 12. DC Characteristics

Symbol	Parameter (1)	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2} (2)	Supply Current (Standby)	$\overline{E} = V_{CC}$ ±0.2V		150	µA
I_{CC3}	Supply Current (Program)	P/E.C. active		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
V_{HH}	V_{PP} Program Voltage		11.4	12.6	V
I_{HH}	V_{PP} Current (Program)	P/E.C. Active		10	mA

Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Average Value.

Figure 12. Read AC Waveforms

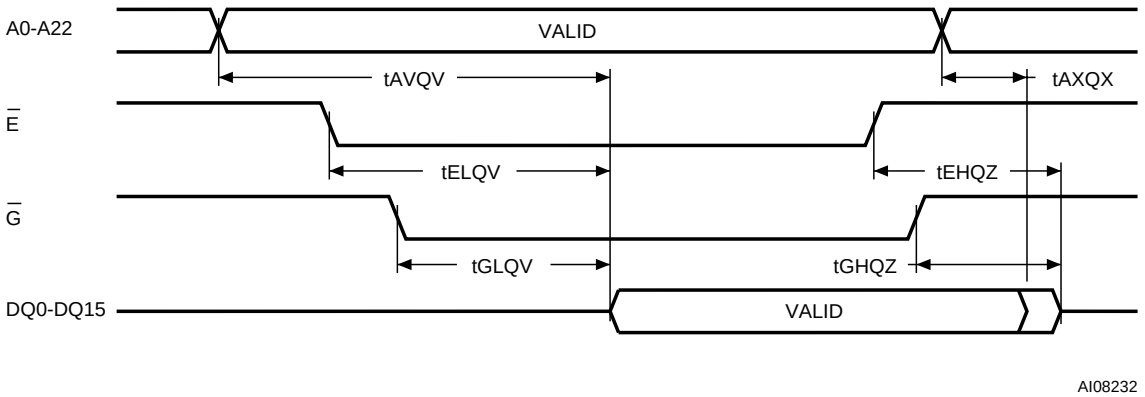


Table 13. Read AC Characteristics

Symbol	Alt	Parameter (1)	Test Condition		M59PW1282			Unit
					100		120	
					V_{CC} = 3.0 to 3.6V	V_{CC} = 2.7 to 3.6V	V_{CC} = 2.7 to 3.6V	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	90	100	120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	90	100	120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	35	35	35	ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	30	30	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	30	30	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition		Min	0	0	0	ns

Note: 1. V_{PP} must be applied after V_{CC} and with the Chip Enable ($\overline{E}$) at V_{IH}.
2. Sampled only, not 100% tested.

Figure 13. Write AC Waveforms, Chip Enable Controlled

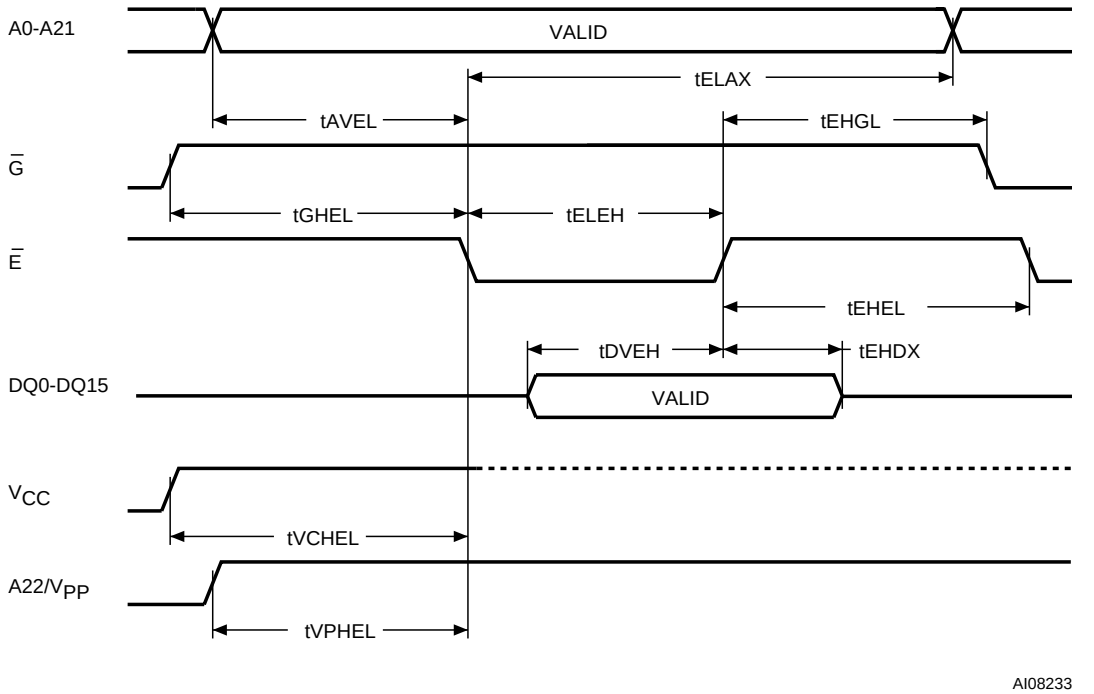


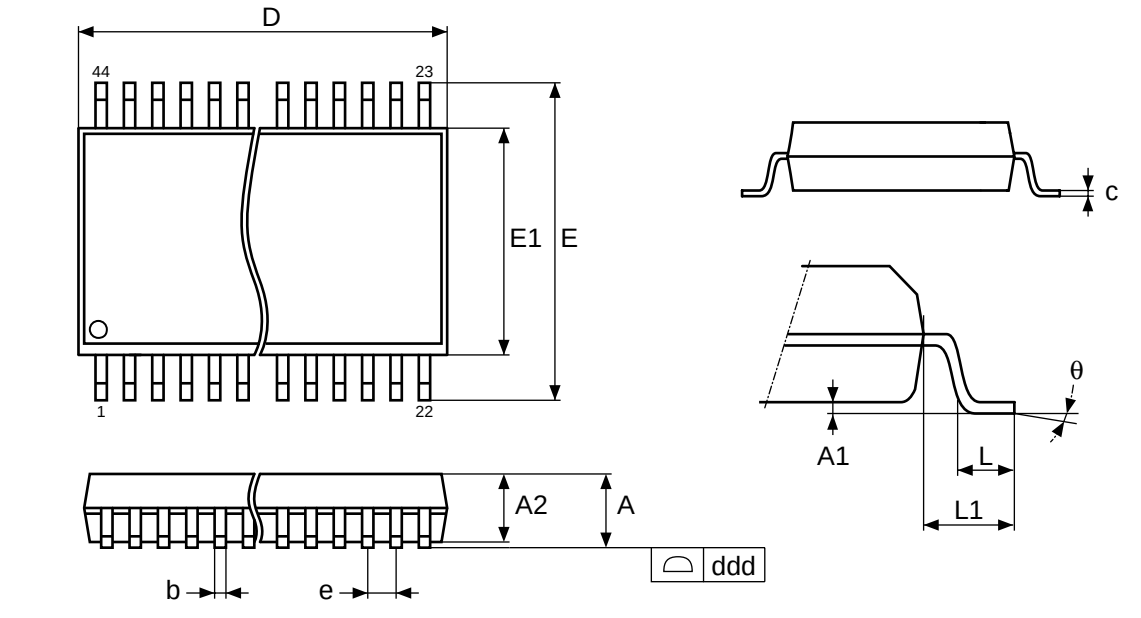
Table 14. Chip Enable Controlled, Write AC Characteristics

Symbol	Alt	Parameter (1)		M59PW1282	Unit
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	50	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	50	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	50	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	100	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	10	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	10	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	µs
t_{VPHEL} (2)	t_{VCS}	V_{PP} High to Chip Enable Low	Min	500	ns

Note: 1. T_A = 25°C; A22/V_{PP} = 11.4 to 12.6V; V_{CC} = 2.7 to 3.6V.
V_{PP} must be applied after V_{CC} and with the Chip Enable ($\overline{E}$) at V_{IH}.
Sampled only, not 100% tested.
2. Not required in Auto Select or Read/Reset command sequences.

PACKAGE MECHANICAL

Figure 14. SO44 - 44 lead Plastic Small Outline, 500 mils body width, Package Outline



Note: Drawing is not to scale.

Table 15. SO44 - 44 lead Plastic Small Outline, 500 mils body width, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.00			0.118
A1	0.10			0.004		
A2	2.69	2.56	2.79	0.106	0.101	0.110
b		0.35	0.50		0.014	0.020
c		0.18	0.28		0.007	0.011
D	28.50	28.37	28.63	1.122	1.117	1.127
ddd			0.10			0.004
E	16.03	15.77	16.28	0.631	0.621	0.641
E1	12.60	12.47	12.73	0.496	0.491	0.501
e	1.27	–	–	0.050	–	–
L	0.79			0.031		
L1	1.73			0.068		
θ			8°			8°
N	44			44		

PART NUMBERING

Table 16. Ordering Information Scheme

Example: M59PW1282 100 M 1 T

Device Type
M59P = LightFlash™ Memory

Operating Voltage
W = V_{CC} = 2.7 to 3.6V

Device Function
128 = 128 Mbit (x16)

Device Function
2 = 2 dice stacked

Speed
100 = 100 ns (1)
120 = 120 ns

Package
M = SO44, 500mils body width

Temperature Range
1 = 0 to 70 °C

Option
T = Tape & Reel Packing

Note: 1. This speed also guarantees 90ns access time at V_{CC} = 3.0 to 3.6V.

Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 17. Document Revision History

Date	Version	Revision Details
20-Jan-2003	1.0	First Issue
06-Feb-2003	2.0	Part Number changed
07-Mar-2003	3.0	Document Status changed to Preliminary Data Document extended to full size
29-Apr-2003	3.1	100ns speed class guarantees 90ns at V_{CC} = 3.0 to 3.6V
20-Nov-2003	3.2	Datasheet status updated to “Full Datasheet”.