

**8M-BIT [1M x 8/512K x 16] CMOS  
SINGLE VOLTAGE FLASH MEMORY**

**FEATURES**

- 5V  $\pm$  10% write and erase
- JEDEC-standard EEPROM commands
- Endurance : 10,000 cycles
- Fast access time: 120/150ns
- Sector erase architecture
  - 8 equal sectors of 128k bytes each
  - Sector erase time: 50ms typical
- Auto Erase and Auto Program Algorithms
  - Automatically erases any one of the sectors or the whole chip with Erase Suspend capability
  - Automatically programs and verifies data at specified addresses
- Status Register feature for detection of program or erase cycle completion
- Low VCC write inhibit  $\leq$  3.2V
- Software and hardware data protection
- Page program operation
  - Internal address and data latches for 128 bytes/64 words per page
  - Page programming time: 3ms typical
  - Byte programming time: 24us in average
- Low power dissipation
  - 50mA active current
  - 100uA standby current
- CMOS and TTL compatible inputs and outputs
- Two independently Protected sectors
- Deep Power-Down Current
  - 1uA ICC typical
- Industry standard surface mount packaging
  - 48 lead TSOP, TYPE I
  - 44 lead SOP

**GENERAL DESCRIPTION**

The MX29F8100 is a 8-mega bit Flash memory organized as either 512K wordx16 or 1M bytex8. The MX29F8100 includes 8-128KB(131,072) blocks or 8-64KW(65,536) blocks. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F8100 is packaged in 48-pin TSOP or 44-pin SOP. For 48-pin TSOP, CE2 and RY/BY are extra pins compared with 44-pin SOP package. This is to optimize the products (such as solid-state disk drives or flash memory cards) control pin budget. PWD is available in 48 -pin TSOP for low power environment. All the above three pins(CE2,RY/BY and PWD) plus one extra VCC pin are not provided in 44-pin SOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F8100 offers access times as fast as 100ns, allowing operation of high-speed microprocessors without wait. To eliminate bus contention, the MX29F8100 has separate chip enables(CE1 and CE2), output enable (OE), and write enable (WE) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F8100 uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

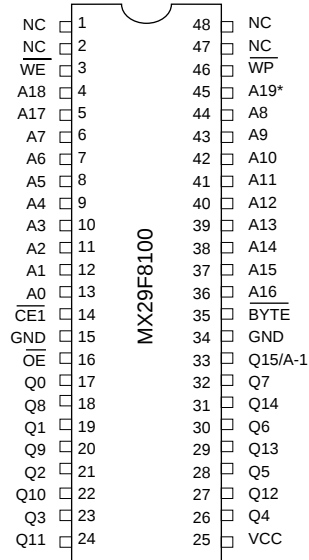
To allow for simple in-system reprogrammability, the MX29F8100 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM.

MXIC Flash technology reliably stores memory contents even after 10,000 cycles. The MXIC's cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F8100 uses a 5V  $\pm$  10% VCC supply to perform the Auto Erase and Auto Program algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC +1V.

## PIN CONFIGURATIONS

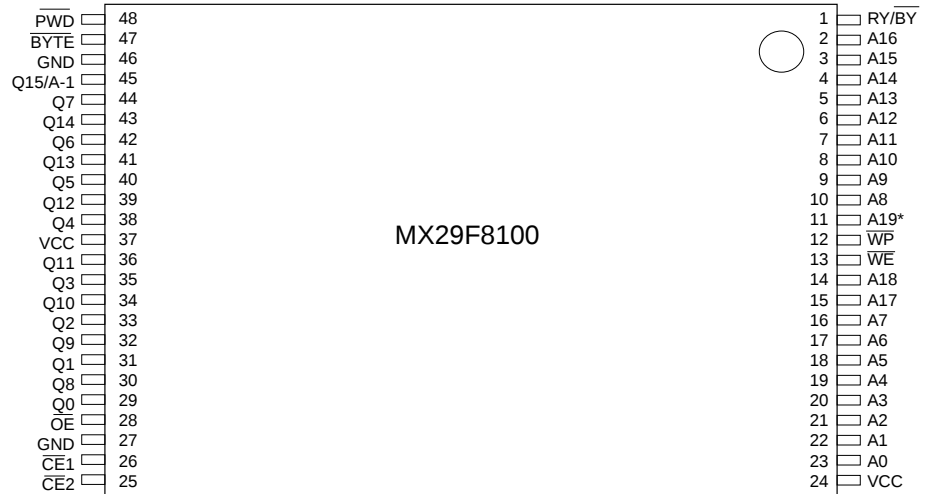
### 44 SOP(500mil)



### 48 TSOP(TYPE I) (12mm x 20mm)



(NORMAL TYPE)



(REVERSE TYPE)

## PIN DESCRIPTION

| SYMBOL    | PIN NAME                            |
|-----------|-------------------------------------|
| A0 - A18  | Address Input                       |
| Q0 - Q14  | Data Input/Output                   |
| Q15/A - 1 | Q15(Word mode)/LSB addr.(Byte mode) |
| CE1/CE2   | Chip Enable Input                   |
| PWD       | Deep Power- Down Input              |
| OE        | Output Enable Input                 |

| SYMBOL | PIN NAME                   |
|--------|----------------------------|
| WE     | Write Enable Input         |
| RY/BY  | Ready/Busy Output          |
| WP     | Sector Write Protect Input |
| BYTE   | Word/Byte Selection Input  |
| VCC    | Power Supply               |
| GND    | Ground Pin                 |

\*A19 : is suggested hard-wired to GND or VCC to minimize TTL current.

The block diagram illustrates the internal architecture of the MX29F8100 Flash Array. The central component is the **MX29F8100 FLASH ARRAY**, which is divided into four quadrants: **X-DECODER**, **Y-DECODER**, **Y-PASS GATE**, and **ARRAY SOURCE HV**. The **CONTROL INPUT LOGIC** block receives external control signals ( $\overline{WE}$ ,  $\overline{CE1}/\overline{CE2}$ ,  $\overline{OE}$ ,  $\overline{WP}$ ,  $\overline{PWD}$ , and  $\overline{BYTE}$ ) and provides signals to the **ADDRESS LATCH AND BUFFER** and the **WRITE STATE MACHINE (WSM)**. The **ADDRESS LATCH AND BUFFER** receives data from **Q15/A-1** and **A0-A18** and provides address signals to the **X-DECODER** and **Y-DECODER**. The **PROGRAM/ERASE HIGH VOLTAGE** block provides high voltage to the **ARRAY SOURCE HV** and the **Y-PASS GATE**. The **WRITE STATE MACHINE (WSM)** is connected to the **COMMAND INTERFACE REGISTER (CIR)**, **COMMAND DATA DECODER**, **COMMAND DATA LATCH**, and **I/O BUFFER**. It also receives **RY/BY** signals. The **COMMAND DATA DECODER** and **COMMAND DATA LATCH** are connected to the **I/O BUFFER**. The **COMMAND DATA LATCH** also receives data from **Q0-Q15/A-1**. The **I/O BUFFER** provides data to the **COMMAND DATA LATCH** and the **WRITE STATE MACHINE (WSM)**. The **Y-PASS GATE** provides data to the **SENSE AMPLIFIER**, which is connected to the **I/O BUFFER**. The **SENSE AMPLIFIER** also provides data to the **PGM DATA HV** block, which is connected to the **PAGE PROGRAM DATA LATCH** and the **I/O BUFFER**. The **PAGE PROGRAM DATA LATCH** provides data to the **PGM DATA HV** block, which in turn provides data to the **ARRAY SOURCE HV**.

**Table1.PIN DESCRIPTIONS**

| SYMBOL                                        | TYPE                 | NAME AND FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0 - A18                                      | INPUT                | ADDRESS INPUTS: for memory addresses. Addresses are internally latched during a write cycle, A19 don't care.(hard wired to VCC or GND is suggested)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Q0 - Q7                                       | INPUT/OUTPUT         | LOW-BYTE DATA BUS: Input data and commands during Command Interface Register(CIR) write cycles. Outputs array,status and identifier data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Q8 - Q14                                      | INPUT/OUTPUT         | HIGH-BYTE DATA BUS: Inputs data during x16 Data-Write operations. Outputs array, identifier data in the appropriate read mode; not used for status register reads. Floated when the chip is de-selected or the outputs are disabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| .Q15/A -1                                     | INPUT/OUTPUT         | Selects between high-byte data INPUT/OUTPUT( $\overline{\text{BYTE}} = \text{HIGH}$ ) and LSB ADDRESS( $\overline{\text{BYTE}} = \text{LOW}$ )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| $\overline{\text{CE1}}/\overline{\text{CE2}}$ | INPUT                | CHIP ENABLE INPUTS: Activate the device's control logic, Input buffers, decoders and sense amplifiers. With either $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ high, the device is de-selected and power consumption reduces to Standby level upon completion of any current program or erase operations. Both $\overline{\text{CE1}},\overline{\text{CE2}}$ must be low to select the device. $\overline{\text{CE2}}$ is not provided in 44-pin SOP package.<br>All timing specifications are the same for both signals. Device selection occurs with the latter falling edge of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ . The first rising edge of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ disables the device. |
| $\overline{\text{PWD}}$                       | INPUT                | POWER-DOWN: Puts the device in deep power-down mode. $\overline{\text{PWD}}$ is active low; $\overline{\text{PWD}}$ high gates normal operation. $\overline{\text{PWD}}$ also locks out erase or program operation when active low providing data protection during power transitions.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| $\overline{\text{OE}}$                        | INPUT                | OUTPUT ENABLES: Gates the device's data through the output buffers during a read cycle $\overline{\text{OE}}$ is active low.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{\text{WE}}$                        | INPUT                | WRITE ENABLE: Controls writes to the Command Interface Register(CIR). $\overline{\text{WE}}$ is active low.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| RY/ $\overline{\text{BY}}$                    | OPEN DRAIN<br>OUTPUT | READY/BUSY: Indicates the status of the internal Write State Machine(WSM). When low it indicates that the WSM is performing a erase or program operation. RY/ $\overline{\text{BY}}$ high indicate that the WSM is ready for new commands, sector erase is suspended or the device is in deep power-down mode. RY/ $\overline{\text{BY}}$ is always active and does not float to tristate off when the chip is deselected or data output are disabled.                                                                                                                                                                                                                                                                                         |
| $\overline{\text{WP}}$                        | INPUT                | WRITE PROTECT: Top or Bottom sector can be protected by writing a non-volatile protect-bit for each sector. When $\overline{\text{WP}}$ is high, all sectors can be programmed or erased regardless of the state of the protect-bits. The $\overline{\text{WP}}$ input buffer is disabled when $\overline{\text{PWD}}$ transitions low(deep power-down mode).                                                                                                                                                                                                                                                                                                                                                                                  |
| $\overline{\text{BYTE}}$                      | INPUT                | BYTE ENABLE: $\overline{\text{BYTE}}$ Low places device in x8 mode. All data is then input or output on Q0-7 and Q8-14 float. Address Q15/A-1 selects between the high and low byte. $\overline{\text{BYTE}}$ high places the device in x16 mode, and turns off the Q15/A-1 input buffer. Address A0, then becomes the lowest order address.                                                                                                                                                                                                                                                                                                                                                                                                   |
| VCC                                           |                      | DEVICE POWER SUPPLY(5V±10%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GND                                           |                      | GROUND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

## BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU . All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

**Table 2.1 Bus Operations for Word-Wide Mode ( $\overline{\text{BYTE}} = \text{VIH}$ )**

| Mode           | Notes | PWD | $\overline{\text{CE1}}$ | $\overline{\text{CE2}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0  | A1  | A9  | Q0-Q7 | Q8-Q14 | Q15/A-1 | RY/ $\overline{\text{BY}}$ |
|----------------|-------|-----|-------------------------|-------------------------|------------------------|------------------------|-----|-----|-----|-------|--------|---------|----------------------------|
| Read           | 1,2,7 | VIH | VIL                     | VIL                     | VIL                    | VIH                    | X   | X   | X   | DOUT  | DOUT   | DOUT    | X                          |
| OutputDisable  | 1,6,7 | VIH | VIL                     | VIL                     | VIH                    | VIH                    | X   | X   | X   | HighZ | HighZ  | HighZ   | X                          |
| Standby        | 1,6,7 | VIH | VIL<br>VIH<br>VIH       | VIH<br>VIL<br>VIH       | X                      | X                      | X   | X   | X   | HighZ | HighZ  | HighZ   | X                          |
| DeepPower-Down | 1,3   | VIL | X                       | X                       | X                      | X                      | X   | X   | X   | HighZ | HighZ  | HighZ   | VOH                        |
| ManufacturerID | 4,8   | VIH | VIL                     | VIL                     | VIL                    | VIH                    | VIL | VIL | VID | C2H   | 00H    | 0B      | VOH                        |
| DeviceID       | 4,8   | VIH | VIL                     | VIL                     | VIL                    | VIH                    | VIH | VIL | VID | 88H   | 00H    | 0B      | VOH                        |
| Write          | 1,5,6 | VIH | VIL                     | VIL                     | VIH                    | VIL                    | X   | X   | X   | DIN   | DIN    | DIN     | X                          |

**Table2.2 Bus Operations for Byte-Wide Mode ( $\overline{\text{BYTE}} = \text{VIL}$ )**

| Mode           | Notes   | PWD | $\overline{\text{CE1}}$ | $\overline{\text{CE2}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0  | A1  | A9  | Q0-Q7 | Q8-Q14 | Q15/A-1 | RY/ $\overline{\text{BY}}$ |
|----------------|---------|-----|-------------------------|-------------------------|------------------------|------------------------|-----|-----|-----|-------|--------|---------|----------------------------|
| Read           | 1,2,7,9 | VIH | VIL                     | VIL                     | VIL                    | VIH                    | X   | X   | X   | DOUT  | HighZ  | VIL/VIH | X                          |
| OutputDisable  | 1,6,7   | VIH | VIL                     | VIL                     | VIH                    | VIH                    | X   | X   | X   | HighZ | HighZ  | X       | X                          |
| Standby        | 1,6,7   | VIH | VIL<br>VIH<br>VIH       | VIH<br>VIL<br>VIH       | X                      | X                      | X   | X   | X   | HighZ | HighZ  | X       | X                          |
| DeepPower-Down | 1,3     | VIL | X                       | X                       | X                      | X                      | X   | X   | X   | HighZ | HighZ  | X       | VOH                        |
| ManufacturerID | 4,8     | VIH | VIL                     | VIL                     | VIL                    | VIH                    | VIL | VIL | VID | C2H   | HighZ  | VIL     | VOH                        |
| DeviceID       | 4,8     | VIH | VIL                     | VIL                     | VIL                    | VIH                    | VIH | VIL | VID | 88H   | HighZ  | VIL     | VOH                        |
| Write          | 1,5,6   | VIH | VIL                     | VIL                     | VIH                    | VIL                    | X   | X   | X   | DIN   | HighZ  | VIL/VIH | X                          |

### NOTES :

- 1.X can be VIH or VIL for address or control pins except for RY/ $\overline{\text{BY}}$  which is either VOL orVOH.
- 2.RY/ $\overline{\text{BY}}$  output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/ $\overline{\text{BY}}$  will be at VOH if it is tied to VCC through a 1K ~ 100K resistor. When the RY/ $\overline{\text{BY}}$  at VOH is independent of  $\overline{\text{OE}}$  while a WSM operation is in progress.
- 3.PWD at GND  $\pm$  0.2V ensures the lowest deep power-down current.
4. A0 and A1 at VIL provide manufacturer ID codes. A0 at VIH and A1 at VIL provide device ID codes. A0 at VIL, A1 at VIH and with appropriate sector addresses provide Sector Protect Code.(Refer to Table 4)
5. Commands for different Erase operations, Data program operations or Sector Protect operations can only be successfully completed through proper command sequence.
- 6.While the WSM is running. RY/ $\overline{\text{BY}}$  in Level-Mode stays at VOL until all operations are complete. RY/ $\overline{\text{BY}}$  goes to VOH when the WSM is not busy or in erase suspend mode.
7. RY/ $\overline{\text{BY}}$  may be at VOL while the WSM is busy performing various operations. For example, a status register read during a write operation.
8. VID = 11.5V- 12.5V.
9. Q15/A-1 = VIL, Q0 - Q7 =D0-D7 out . Q15/A-1 = VIH, Q0 - Q7 = D8 -D15 out.

## WRITE OPERATIONS

Commands are written to the COMMAND INTERFACE REGISTER (CIR) using standard microprocessor write timings. The CIR serves as the interface between the microprocessor and the internal chip operation. The CIR can decipher Read Array, Read Silicon ID, Erase and Program command. In the event of a read command, the CIR simply points the read path at either the array or the silicon ID, depending on the specific read command given. For a program or erase cycle, the CIR informs the write state machine that a program or erase has been requested. During a program cycle, the write state machine will control the program sequences and the CIR

will only respond to status reads. During a sector/chip erase cycle, the CIR will respond to status reads and erase suspend. After the write state machine has completed its task, it will allow the CIR to respond to its full command set. The CIR stays at read status register mode until the microprocessor issues another valid command sequence.

Device operations are selected by writing commands into the CIR. Table 3 below defines 8 Mbit flash family command.

**TABLE 3. COMMAND DEFINITIONS**

| Command Sequence            |      | Read/Reset | Silicon ID Read | Page/Byte Program | Chip Erase | Sector Erase | Erase Suspend | Erase Resume | Read Status Reg. | Clear Status Reg. |
|-----------------------------|------|------------|-----------------|-------------------|------------|--------------|---------------|--------------|------------------|-------------------|
| Bus Write Cycles Req'd      |      | 4          | 4               | 4                 | 6          | 6            | 3             | 3            | 4                | 3                 |
| First Bus Write Cycle       | Addr | 5555H      | 5555H           | 5555H             | 5555H      | 5555H        | 5555H         | 5555H        | 5555H            | 5555H             |
|                             | Data | AAH        | AAH             | AAH               | AAH        | AAH          | AAH           | AAH          | AAH              | AAH               |
| Second Bus Write Cycle      | Addr | 2AAAH      | 2AAAH           | 2AAAH             | 2AAAH      | 2AAAH        | 2AAAH         | 2AAAH        | 2AAAH            | 2AAAH             |
|                             | Data | 55H        | 55H             | 55H               | 55H        | 55H          | 55H           | 55H          | 55H              | 55H               |
| Third Bus Write Cycle       | Addr | 5555H      | 5555H           | 5555H             | 5555H      | 5555H        | 5555H         | 5555H        | 5555H            | 5555H             |
|                             | Data | F0H        | 90H             | A0H               | 80H        | 80H          | B0H           | D0H          | 70H              | 50H               |
| Fourth Bus Read/Write Cycle | Addr | RA         | 00H/01H         | PA                | 5555H      | 5555H        |               |              | X                |                   |
|                             | Data | RD         | C2H/88H         | PD                | AAH        | AAH          |               |              | SRD              |                   |
| Fifth Bus Write Cycle       | Addr |            |                 |                   | 2AAAH      | 2AAAH        |               |              |                  |                   |
|                             | Data |            |                 |                   | 55H        | 55H          |               |              |                  |                   |
| Sixth Bus Write Cycle       | Addr |            |                 |                   | 5555H      | SA           |               |              |                  |                   |
|                             | Data |            |                 |                   | 10H        | 30H          |               |              |                  |                   |

**COMMAND DEFINITIONS(continue Table 3.)**

| Command Sequence            |      | Sector Protection | Sector Unprotect | Verify Sector Protect | Sleep | Abort |
|-----------------------------|------|-------------------|------------------|-----------------------|-------|-------|
| Bus Write Cycles Req'd      |      | 6                 | 6                | 4                     | 3     | 3     |
| First Bus Write Cycle       | Addr | 5555H             | 5555H            | 5555H                 | 5555H | 5555H |
|                             | Data | AAH               | AAH              | AAH                   | AAH   | AAH   |
| Second Bus Write Cycle      | Addr | 2AAAH             | 2AAAH            | 2AAAH                 | 2AAAH | 2AAAH |
|                             | Data | 55H               | 55H              | 55H                   | 55H   | 55H   |
| Third Bus Write Cycle       | Addr | 5555H             | 5555H            | 5555H                 | 5555H | 5555H |
|                             | Data | 60H               | 60H              | 90H                   | C0H   | E0H   |
| Fourth Bus Read/Write Cycle | Addr | 5555H             | 5555H            | *                     |       |       |
|                             | Data | AAH               | AAH              | C2H*                  |       |       |
| Fifth Bus Write Cycle       | Addr | 2AAAH             | 2AAAH            |                       |       |       |
|                             | Data | 55H               | 55H              |                       |       |       |
| Sixth Bus Write Cycle       | Addr | SA**              | SA**             |                       |       |       |
|                             | Data | 20H               | 40H              |                       |       |       |

**Notes:**

- Address bit A15 -- A18 = X = Don't care for all address commands except for Program Address(PA) and Sector Address(SA).  
5555H and 2AAAH address command codes stand for Hex number starting from A0 to A14.
- Bus operations are defined in Table 2.
- RA = Address of the memory location to be read.  
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the  $\overline{WE}$  pulse.  
SA = Address of the sector to be erased. The combination of A16 -- A18 will uniquely select any sector.
- RD = Data read from location RA during read operation.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of  $\overline{WE}$ .  
SRD = Data read from status register.
- Only Q0-Q7 command data is taken, Q8-Q15 = Don't care.  
\* Refer to Table 4, Figure 12.  
\*\* Only the top and the bottom sectors have protect- bit feature. SA = (A18,A17,A16) = 000B or 111B is valid.

## DEVICE OPERATION

### SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (11.5V~12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the

MX29F8100 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 3.

Byte 0 (A0=VIL) represents the manufacturer's code (MXIC=C2H) and byte 1 (A0=VIH) the device identifier code (MX29F8100=88H).

To terminate the operation, it is necessary to write the read/reset command sequence into the CIR.

**Table 4. MX29F8100 Silion ID Codes and Verify Sector Protect Code**

| Type                  | A <sub>18</sub>   | A <sub>17</sub> | A <sub>16</sub> | A <sub>1</sub> | A <sub>0</sub> | Code(HEX) | DQ <sub>7</sub> | DQ <sub>6</sub> | DQ <sub>5</sub> | DQ <sub>4</sub> | DQ <sub>3</sub> | DQ <sub>2</sub> | DQ <sub>1</sub> | DQ <sub>0</sub> |
|-----------------------|-------------------|-----------------|-----------------|----------------|----------------|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Manufacturer Code     | X                 | X               | X               | VIL            | VIL            | C2H*      | 1               | 1               | 0               | 0               | 0               | 0               | 1               | 0               |
| MX29F8100 Device Code | X                 | X               | X               | VIL            | VIH            | 88H*      | 1               | 0               | 0               | 0               | 1               | 0               | 0               | 0               |
| Verify Sector Protect | Sector Address*** |                 |                 | VIH            | VIL            | C2H**     | 1               | 1               | 0               | 0               | 0               | 0               | 1               | 0               |

\* MX29F8100 Manufacturer Code = C2H, Device Code = 88H when  $\overline{\text{BYTE}} = \text{VIL}$   
 MX29F8100 Manufacturer Code = 00C2H, Device Code = 0088H when  $\overline{\text{BYTE}} = \text{VIH}$

\*\* Outputs C2H at protected sector address, 00H at unprotected scetor address.

\*\*\*Only the top and the bottom sectors have protect-bit feature. Sector address = ( A18,A17,A16) =000B or 111B

## READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the CIR contents are altered by a valid command sequence.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

The MX29F8100 is accessed like an EPROM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers flexibility in preventing bus contention.

$\overline{CE}$  stands for the combination of  $\overline{CE1}$  and  $\overline{CE2}$  in 48-pin TSOP package.  $\overline{CE}$  stands for  $\overline{CE1}$  in 44-pin SOP package.

Note that the read/reset command is not valid when program or erase is in progress.

## PAGE PROGRAM

To initiate Page program mode, a three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the page program command-A0H.

Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine (WSM), no data will be written to the device.

After three-cycle command sequence is given, a byte(word) load is performed by applying a low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . Maximum of 128 bytes of data may be loaded into each page by the same procedure as outlined in the page program section below.

## BYTE-WIDE LOAD/WORD-WIDE LOAD

Byte(word) loads are used to enter the 128 bytes(64 words) of a page to be programmed or the software codes for data protection. A byte load(word load) is performed by applying a low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ .

Either byte-wide load or word-wide load is determined (Byte = VIL or VIH is latched) on the falling edge of the  $\overline{WE}$ (or  $\overline{CE}$ ) during the 3rd command write cycle.

## PROGRAM

Any page to be programmed should have the page in the erased state first, i.e. performing sector erase is suggested before page programming can be performed.

The device is programmed on a page basis. If a byte(word) of data within a page is to be changed, data for the entire page can be loaded into the device. Any byte(word) that is not loaded during the programming of its page will be still in the erased state (i.e. FFH). Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte(word) has been loaded into the device, successive bytes(words) are entered in the same manner. Each new byte(word) to be programmed must have its high to low transition on  $\overline{WE}$  (or  $\overline{CE}$ ) within 30us of the low to high transition of  $\overline{WE}$  (or  $\overline{CE}$ ) of the preceding byte(word). A6 to A18 specify the page address, i.e., the device is page-aligned on 128 bytes(64 words) boundary. The page address must be valid during each high to low transition of  $\overline{WE}$  or  $\overline{CE}$ . A-1 to A5 specify the byte address within the page, A0 to A5 specify the word address within the page. The byte(word) may be loaded in any order; sequential loading is not required. If a high to low transition of  $\overline{CE}$  or  $\overline{WE}$  is not detected within 100us of the last low to high transition, the load period will end and the internal programming period will start. The Auto page program terminates when status on DQ7 is '1' at which time the device stays at read status register mode until the CIR contents are altered by a valid command sequence. (Refer to table 3,6 and Figure 1,7,8)

## CHIP ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command-80H. Two more "unlock" write cycles are then followed by the chip erase command-10H.

Chip erase does not require the user to program the device prior to erase.

The automatic erase begins on the rising edge of the last  $\overline{WE}$  pulse in the command sequence and terminates when the status on DQ7 is "1" at which time the device stays at read status register mode. The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.(Refer to table 3,6 and Figure 2,7,9)

**Table 5. MX29F8100 Sector Address Table  
(Byte-Wide Mode)**

|             | A19 | A18 | A17 | A16 | Address Range[A18, -1] |
|-------------|-----|-----|-----|-----|------------------------|
| <b>SA0</b>  | X   | 0   | 0   | 0   | 00000H--1FFFFH         |
| <b>SA1</b>  | X   | 0   | 0   | 1   | 20000H--3FFFFH         |
| <b>SA2</b>  | X   | 0   | 1   | 0   | 40000H--5FFFFH         |
| <b>SA3</b>  | X   | 0   | 1   | 1   | 60000H--7FFFFH         |
| <b>SA4</b>  | X   | 1   | 0   | 0   | 80000H--9FFFFH         |
|             | 1   | ... | ... | ... | .....                  |
| <b>SA17</b> | X   | 1   | 1   | 1   | E0000H--FFFFFFH        |

## SECTOR ERASE

Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command-80H. Two more "unlock" write cycles are then followed by the sector erase command-30H. The sector address is latched on the falling edge of  $\overline{WE}$ , while the command (data) is latched on the rising edge of  $\overline{WE}$ .

Sector erase does not require the user to program the device prior to erase. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins on the rising edge of the last  $\overline{WE}$  pulse in the command sequence and terminates when the status on DQ7 is "1" at which time the device stays at read status register mode. The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.(Refer to table 3,6 and Figure 3,4,7,9))

## ERASE SUSPEND

This command only has meaning while the the WSM is executing SECTOR or CHIP erase operation, and therefore will only be responded to during SECTOR or CHIP erase operation. After this command has been executed, the CIR will initiate the WSM to suspend erase operations, and then return to Read Status Register mode. The WSM will set the DQ6 bit to a "1". Once the WSM has reached the Suspend state,the WSM will set the DQ7 bit to a "1", At this time, WSM allows the CIR to respond to the Read Array, Read Status Register, Abort and Erase Resume commands only. In this mode, the CIR will not resopnd to any other comands. The WSM will continue to run, idling in the SUSPEND state, regardless of the state of all input control pins, with the exclusion of  $\overline{PWD}$ .  $\overline{PWD}$  low will immediately shut down the WSM and the remainder of the chip.

## ERASE RESUME

This command will cause the CIR to clear the suspend state and set the DQ6 to a '0', but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.

## READ STATUS REGISTER

The MXIC's 8 Mbit flash family contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status command to the CIR. After writing this command, all subsequent read operations output data from the status register until another valid command sequence is written to the CIR. A Read Array command must be written to the CIR to return to the Read Array mode.

The status register bits are output on DQ2 - DQ7 (table 6) whether the device is in the byte-wide (x8) or word-wide (x16) mode for the MX29F8100. In the word-wide mode the upper byte, DQ(8:15) is set to 00H during a Read Status command. In the byte-wide mode, DQ(8:14) are tri-stated and DQ15/A-1 retains the low order address function. DQ0-DQ1 is set to 0H in either x8 or x16 mode.

It should be noted that the contents of the status register are latched on the falling edge of  $\overline{OE}$  or  $\overline{CE}$  whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the status register change while reading the status register.  $\overline{CE}$  or  $\overline{OE}$  must be toggled with each subsequent status read, or the completion of a program or erase operation will not be evident.

The Status Register is the interface between the microprocessor and the Write State Machine (WSM). When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation. The WSM sets status bits four through seven and clears bits six and seven, but cannot clear status bits four and five. If Erase fail or Program fail status bit is detected, the Status Register is not cleared until the Clear Status Register command is written. The MX29F8100 automatically outputs Status Register data when read after Chip Erase, Sector Erase, Page Program or Read Status Command write cycle. The default state of the Status Register after powerup and return from deep power-down mode is (DQ7, DQ6, DQ5, DQ4) = 1000B. DQ3 = 0 or 1 depends on sector-protect status, can not be changed by Clear Status Register Command or Write State Machine. DQ2 = 0 or 1 depends on Sleep status, During Sleep mode or Abort mode DQ2 is set to "1"; DQ2 is reset to "0" by Read Array command.

## CLEAR STATUS REGISTER

The Erase fail status bit (DQ5) and Program fail status bit (DQ4) are set by the write state machine, and can only be reset by the system software. These bits can indicate various failure conditions (see Table 6). By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several pages or erasing multiple blocks in sequence). The status register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Additionally, once the program (erase) fail bit happens, the program (erase) operation can not be performed further. The program (erase) fail bit must be reset by system software before further page program or sector (chip) erase are attempted. To clear the status register, the Clear Status Register command is written to the CIR. Then, any other command may be issued to the CIR. Note again that before a read cycle can be initiated, a Read command must be written to the CIR to specify whether the read data is to come from the Array, Status Register or Silicon ID.

**TABLE 6. MX29F8100 STATUS REGISTER**

|                                       | STATUS                 | NOTES    | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 |
|---------------------------------------|------------------------|----------|-----|-----|-----|-----|-----|-----|
| <b>IN PROGRESS</b>                    | PROGRAM                | 1,2, 6,7 | 0   | 0   | 0   | 0   | 0/1 | 0/1 |
|                                       | ERASE                  | 1,3, 6,7 | 0   | 0   | 0   | 0   | 0/1 | 0/1 |
|                                       | SUSPEND (NOT COMPLETE) | 1,4, 6,7 | 0   | 1   | 0   | 0   | 0/1 | 0/1 |
|                                       | -----<br>(COMPLETE)    |          | 1   | 1   | 0   | 0   | 0/1 | 0/1 |
| <b>COMPLETE</b>                       | PROGRAM                | 1,2, 6,7 | 1   | 0   | 0   | 0   | 0/1 | 0/1 |
|                                       | ERASE                  | 1,3, 6,7 | 1   | 0   | 0   | 0   | 0/1 | 0/1 |
| <b>FAIL</b>                           | PROGRAM                | 1,5, 6,7 | 1   | 0   | 0   | 1   | 0/1 | 0/1 |
|                                       | ERASE                  | 1,5, 6,7 | 1   | 0   | 1   | 0   | 0/1 | 0/1 |
| <b>AFTER CLEARING STATUS REGISTER</b> |                        | 6,7      | 1   | 0   | 0   | 0   | 0/1 | *   |

**NOTES:**
**-1. DQ7 : WRITE STATE MACHINE STATUS**

1 = READY, 0 = BUSY

**DQ6 : ERASE SUSPEND STATUS**

1 = SUSPEND, 0 = NO SUSPEND

**DQ5 : ERASE FAIL STATUS**

1 = FAIL IN ERASE, 0 = SUCCESSFUL ERASE

**DQ4 : PROGRAM FAIL STATUS**

1 = FAIL IN PROGRAM, 0 = SUCCESSFUL PROGRAM

**DQ3 : SECTOR-PROTECT STATUS**

1 = SECTOR 0 OR/AND 15 PROTECTED

0 = NONE OF SECTOR PROTECTED

**DQ2 : SLEEP STATUS**

1 = DEVICE IN SLEEP STATUS

0 = DEVICE NOT IN SLEEP STATUS

**DQ1 - 0 = RESERVED FOR FUTURE ENHANCEMENTS.**

These bits are reserved for future use ; mask them out when polling the Status Register.

2. PROGRAM STATUS is for the status during Page Programming or Sector Unprotect mode.

3. ERASE STATUS is for the status during Sector/Chip Erase or Sector Protection mode.

4. SUSPEND STATUS is for both Sector and Chip Erase mode .

5. FAIL STATUS bit(DQ4 or DQ5) is provided during Page Program or Sector/Chip Erase modes respectively.

6. DQ3 = 0 or1 depends on Sector-Protect Status.

7. DQ2 = 0 or 1 depends on whether device is in the Sleep mode or not .

\* Once in the Sleep mode, DQ2 is set to "1", and is reset by read array command only.-

## HARDWARE SECTOR PROTECTION

The MX29F8100 features sector protection. This feature will disable both program and erase operations in either the top or the bottom sector (0 or 7). The sector protection feature is enabled using system software by the user (Refer to table 3). The device is shipped with both sectors unprotected. Alternatively, MXIC may protect sectors in the factory prior to shipping the device.

## SECTOR PROTECTION

To activate this mode, a six-bus cycle operation is required. There are two 'unlock' write cycles. These are followed by writing the 'set-up' command. Two more 'unlock' write cycles are then followed by the Lock Sector command - 20H. Sector address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$  of the sixth cycle of the command sequence. The automatic Lock operation begins on the rising edge of the last  $\overline{WE}$  pulse in the command sequence and terminates when the Status on DQ7 is '1' at which time the device stays at the read status register mode.

The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence (Refer to table 3,6 and Figure 10,12 ).

## VERIFY SECTOR PROTECT

To verify the Protect status of the Top and the Bottom sector, operation is initiated by writing Silicon ID read command into the command register. Following the command write, a read cycle from address XXX0H retrieves the Manufacturer code of C2H. A read cycle from XXX1H returns the Device code 88H. A read cycle from appropriate address returns information as to which sectors are protected. To terminate the operation, it is necessary to write the read/reset command sequence into the CIR.

(Refer to table 3,4 and Figure 12)

A few retries are required if Protect status can not be verified successfully after each operation.

## SECTOR UNPROTECT

It is also possible to unprotect the sector, same as the first five write command cycles in activating sector protection mode followed by the Unprotect Sector command - 40H, the automatic Unprotect operation begins on the rising edge of the last  $\overline{WE}$  pulse in the command sequence and terminates when the Status on DQ7 is '1' at which time the device stays at the read status register mode. (Refer to table 3,6 and Figure 11,12)

The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.

Either Protect or Unprotect sector mode is accomplished by keeping  $\overline{WP}$  high, i.e. protect-bit status can only be changed with a valid command sequence and  $\overline{WP}$  at high. When  $\overline{WP}$  is high, all sectors can be programmed or erased regardless of the state of the protect-bits. Protect-bit status will not be changed during chip/sector erase operations. With  $\overline{WP}$  at VIL, only unprotected sectors can be programmed or erased.

## DEEP POWER-DOWN MODE

The MXIC's 8Mbit flash family supports a typical ICC of 1uA in deep power-down mode. One of the target markets for these devices is in portable equipment where the power consumption of the machine is of prime importance. When PWD is a logic low ( $GND \pm 0.2V$ ), all circuits are turned off and the device typically draws 1uA of ICC current.

During read modes, the  $\overline{PWD}$  pin going low deselects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum of 700 nanoseconds to access valid data.

During erase or program modes,  $\overline{PWD}$  low will abort either erase or program operation. The contents of the memory are no longer valid as the data has been corrupted by the PWD function. As in the read mode above, all internal circuitry is turned off to achieve the 1uA current level.

$\overline{PWD}$  transitions to VIL or turning power off to the device will clear the status register.

$\overline{PWD}$  pin is not provided in 44-pin SOP package.

## SLEEP MODE

The MX29F8100 features two software controlled low-power modes : Sleep and Abort modes. Sleep mode is allowed during any current operations except that once Suspend command is issued, Sleep command is ignored. Abort mode is executed only during Page Program and Chip/Sector Erase mode.

To activate Sleep mode, a three-bus cycle operation is required. The C0H command (Refer to table 3) puts the device in the Sleep mode. Once in the Sleep mode and with CMOS input level applied, the power of the device is reduced to deep power-down current levels. The only power consumed is diffusion leakage, transistor sub-threshold conduction, input leakage, and output leakage.

The Sleep command allows the device to COMPLETE current operations before going into Sleep mode. Once current operation is done, device stays at read status register mode, RY/BY returns to ready state. The status registers are not reset during sleep command. Program or erase fail bit may have been set if during program/erase mode the device retry exceeds maximum count.

During Sleep mode, the status registers, Silicon ID codes remain valid and can still be read. The Device Sleep Status bit - DQ2 will indicate that the device in the sleep mode.

Writing the Read Array command wakes up the device out of sleep mode. DQ2 is reset to "0" and Device returns to standby current level.

## ABORT MODE

To activate Abort mode, a three-bus cycle operation is required. The E0H command (Refer to table 3) only stops Page program or Sector /Chip erase operation currently in progress and puts the device in Sleep mode. But unlike the sleep command, the program or erase operation will not be completed. Since the data in some page/sectors is no longer valid due to an incomplete program or erase operation, the program fail (DQ4) or erase fail (DQ5) bit will be set.

After the abort command is executed and with CMOS input level applied, the device current is reduced to the

same level as in deep power-down or sleep modes. Device stays at read status register mode, RY/BY returns to ready state.

During Abort mode, the status registers, Silicon ID codes remain valid and can still be read. The Device Sleep Status bit - DQ2 will indicate that the device in the sleep mode.

Similar to the sleep mode, A read array command MUST be written to bring the device out of the abort state without incurring any wake up latency. Note that once device is waken up, Clear status register mode is required before a program or erase operation can be executed.

## RY/BY PIN AND PROGRAM/ERASE POLLING

RY/BY is a full CMOS output that provides a hardware method of detecting page program and sector erase completion. It transitions to VIL after a program or erase command sequence is written to the MX29F8100, and returns to VOH when the WSM has finished executing the internal algorithm.

RY/BY can be connected to the interrupt input of the system CPU or controller. It is active at all times, not tristated if the CE or OE inputs are brought to VIH. RY/BY is also VOH when the device is in erase suspend or deep power-down modes.

RY/BY pin is not provided in 44-pin SOP package.

## DATA PROTECTION

The MX29F8100 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read Array mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

## **LOW VCC WRITE INHIBIT**

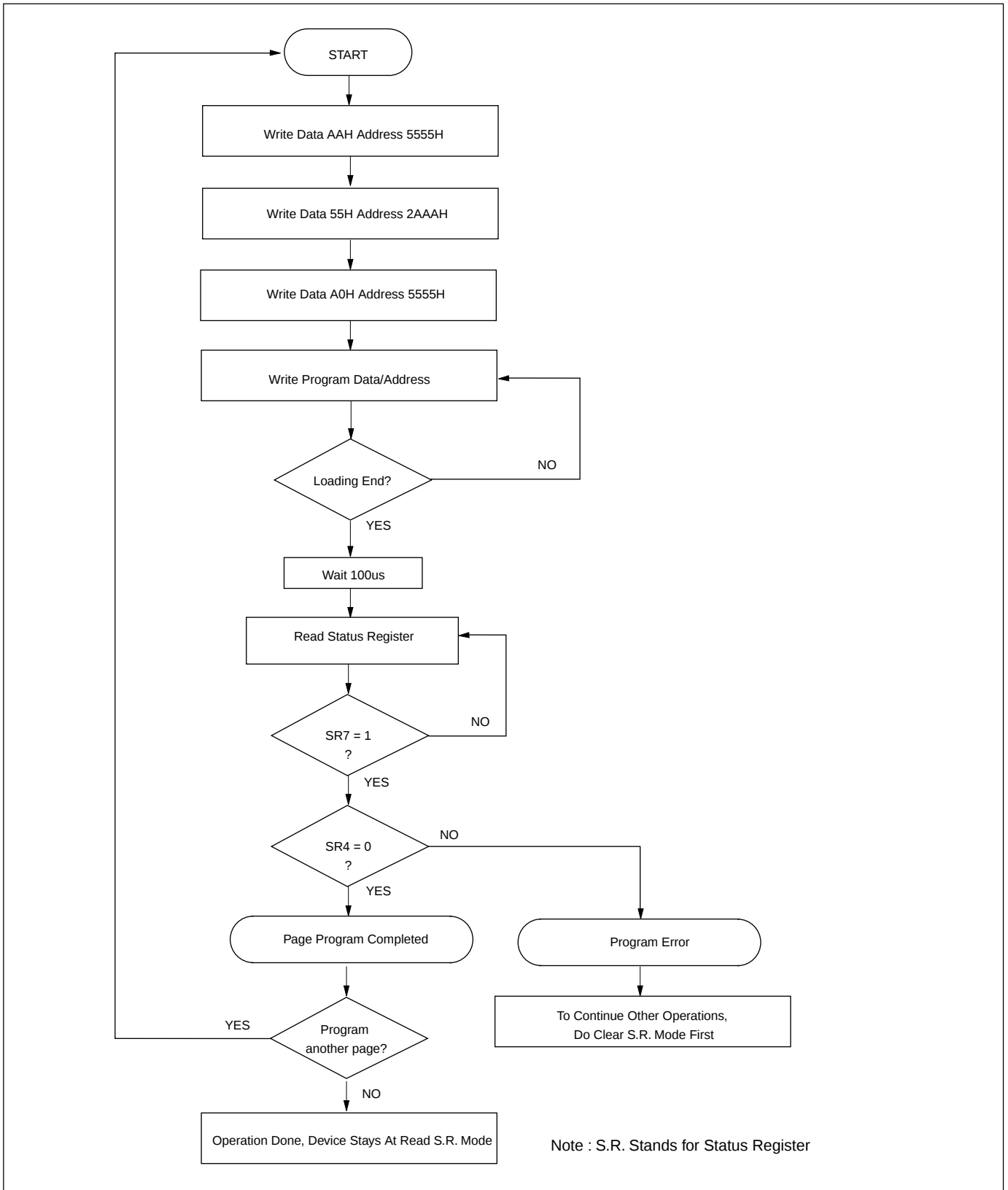
To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than VLKO(= 3.2V , typically 3.5V). If  $VCC < VLKO$ , the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VCC is above VLKO.

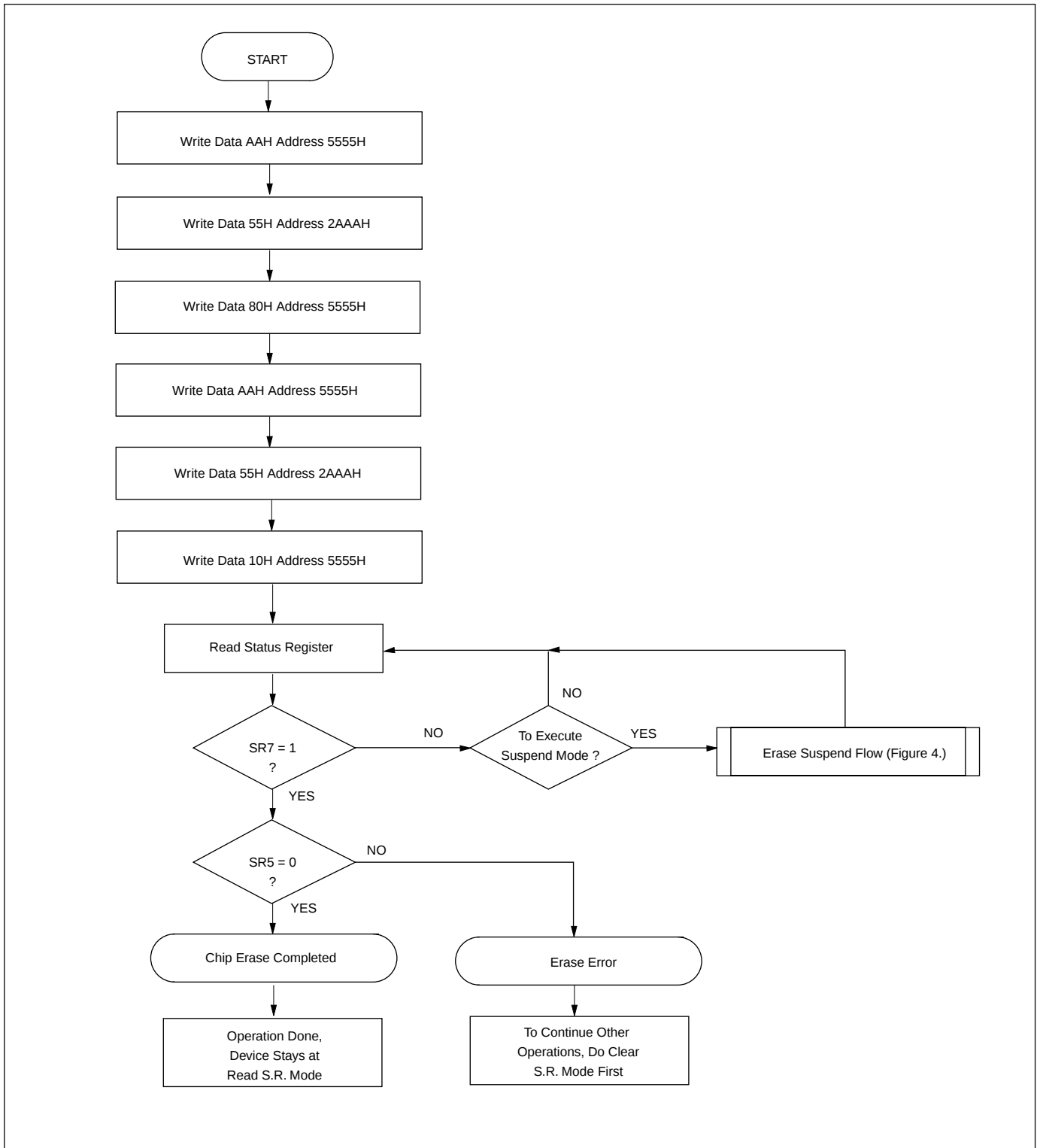
## **WRITE PULSE "GLITCH" PROTECTION**

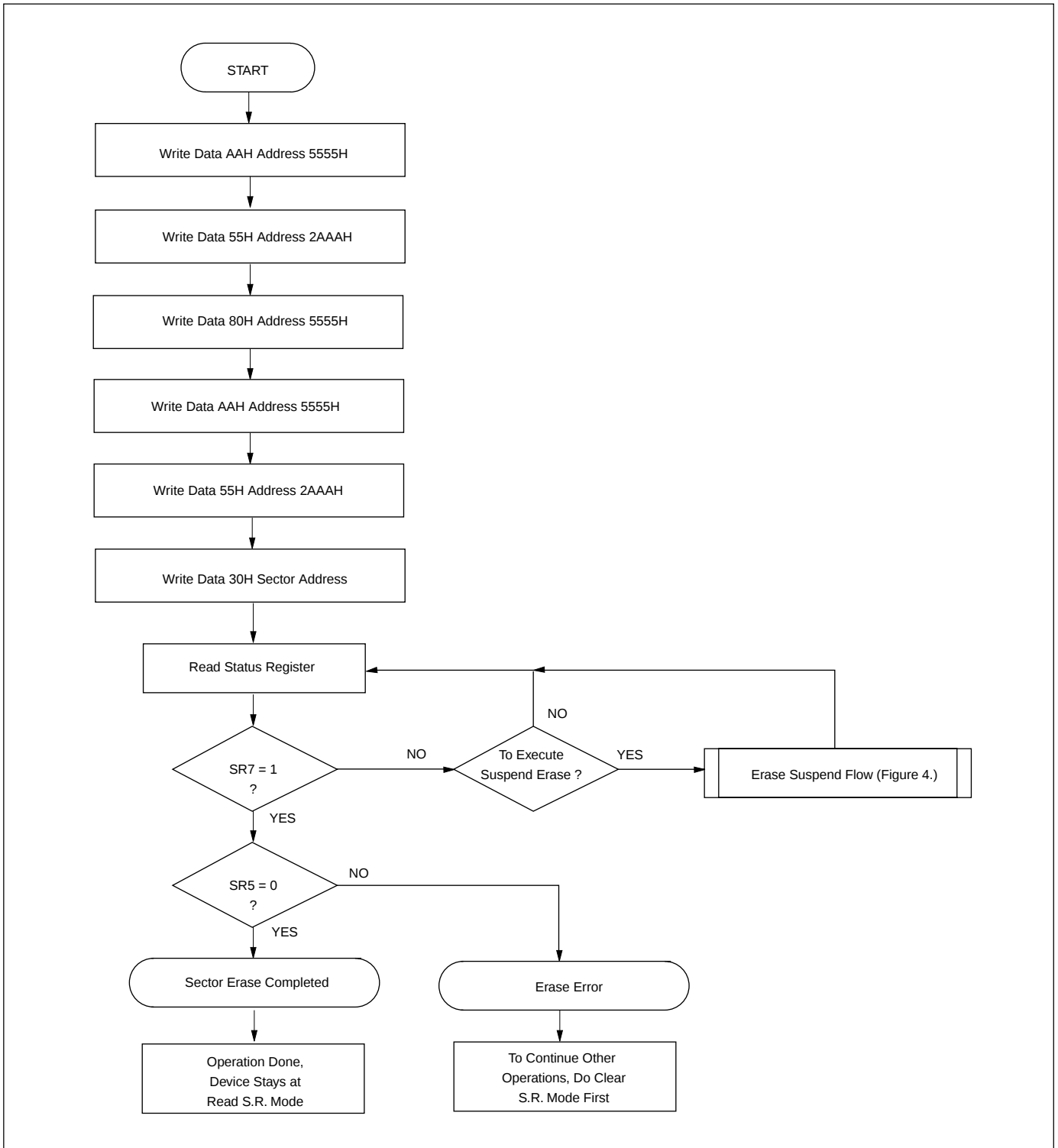
Noise pulses of less than 10ns (typical) on  $\overline{CE}$  or  $\overline{WE}$  will not initiate a write cycle.

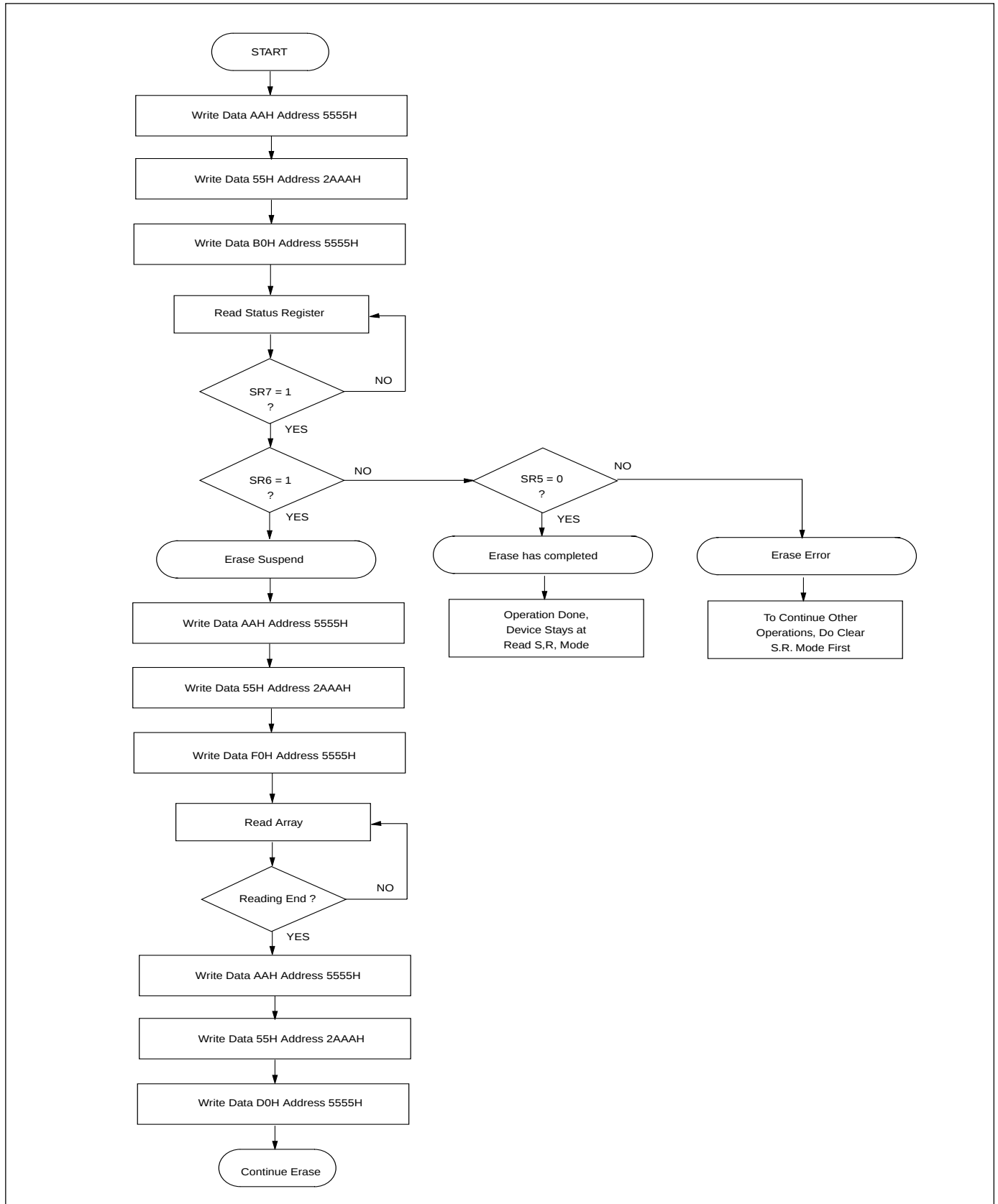
## **LOGICAL INHIBIT**

Writing is inhibited by holding any one of  $\overline{OE} = VIL$ ,  $\overline{CE} = VIH$  or  $\overline{WE} = VIH$ . To initiate a write cycle  $\overline{CE}$  and  $\overline{WE}$  must be a logical zero while  $\overline{OE}$  is a logical one.

**Figure 1. AUTOMATIC PAGE PROGRAM FLOW CHART**


**Figure 2. AUTOMATIC CHIP ERASE FLOW CHART**


**Figure 3. AUTOMATIC SECTOR ERASE FLOW CHART**


**Figure 4. ERASE SUSPEND/ERASE RESUME FLOW CHART**


## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| RATING                        | VALUE          |
|-------------------------------|----------------|
| Ambient Operating Temperature | 0°C to 70°C    |
| Storage Temperature           | -65°C to 125°C |
| Applied Input Voltage         | -0.5V to 7.0V  |
| Applied Output Voltage        | -0.5V to 7.0V  |
| VCC to Ground Potential       | -0.5V to 7.0V  |
| A9                            | -0.5V to 13.5V |

### NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

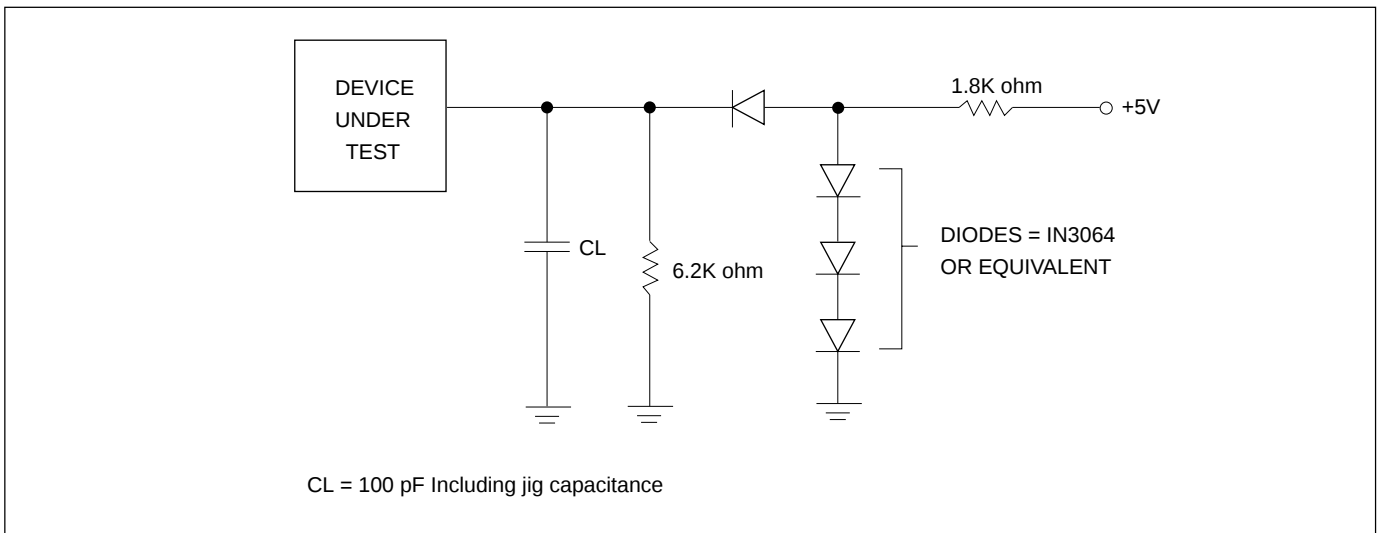
### NOTICE:

Specifications contained within the following tables are subject to change.

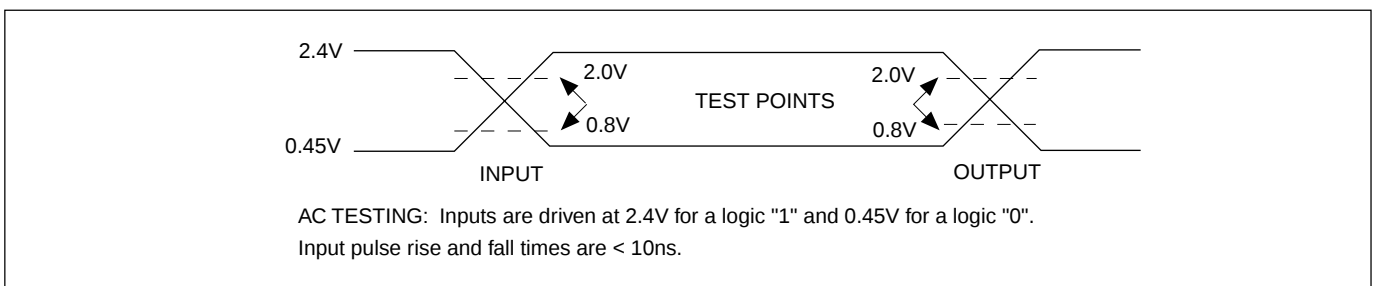
### CAPACITANCE $T_A = 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$

| SYMBOL           | PARAMETER          | MIN. | TYP. | MAX. | UNIT | CONDITIONS            |
|------------------|--------------------|------|------|------|------|-----------------------|
| C <sub>IN</sub>  | Input Capacitance  |      |      | 14   | pF   | V <sub>IN</sub> = 0V  |
| C <sub>OUT</sub> | Output Capacitance |      |      | 16   | pF   | V <sub>OUT</sub> = 0V |

### SWITCHING TEST CIRCUITS



### SWITCHING TEST WAVEFORMS



**DC CHARACTERISTICS = 0 °C to 70 °C, VCC = 5V±10%**

| SYMBOL | PARAMETER                   | NOTES | MIN. | TYP. | MAX.    | UNITS | TEST CONDITIONS                                                                                                                                                                                                      |
|--------|-----------------------------|-------|------|------|---------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IIL    | Input Load Current          | 1     |      |      | ±10     | uA    | VCC = VCC Max<br>VIN = VCC or GND                                                                                                                                                                                    |
| ILO    | Output Leakage Current      | 1     |      |      | ±10     | uA    | VCC = VCC Max<br>VIN = VCC or GND                                                                                                                                                                                    |
| ISB1   | VCC Standby Current(CMOS)   | 1     |      | 50   | 100     | uA    | VCC = VCC Max<br>CE1, CE2, PWD = VCC ± 0.2V                                                                                                                                                                          |
| ISB2   | VCC Standby Current(TTL)    |       |      | 2    | 4       | mA    | VCC = VCC Max<br>CE1, CE2, PWD = VIH                                                                                                                                                                                 |
| IDP    | VCC Deep Power-Down Current | 1     |      | 1    | 20      | uA    | PWD = GND ± 0.2V                                                                                                                                                                                                     |
| ICC1   | VCC Read Current            | 1     |      | 50   | 60      | mA    | VCC = VCC Max<br>CMOS: CE1, CE2 = GND ± 0.2V<br>BYTE = GND ± 0.2V or VCC ± 0.2V<br>Inputs = GND ± 0.2V or VCC ± 0.2V<br>TTL : CE1, CE2 = VIL,<br>BYTE = VIL or VIH<br>Inputs = VIL or VIH,<br>f = 10MHz, IOUT = 0 mA |
| ICC2   | VCC Read Current            | 1     |      | 30   | 35      | mA    | VCC = VCC Max,<br>CMOS: CE1, CE2 = GND ± 0.2V<br>BYTE = VCC ± 0.2V or GND ± 0.2V<br>Inputs = GND ± 0.2V or VCC ± 0.2V<br>TTL: CE1, CE2 = VIL,<br>BYTE = VIH or VIL<br>Inputs = VIL or VIH,<br>f = 5MHz, IOUT = 0mA   |
| ICC3   | VCC Erase Suspend Current   | 1,2   |      | 5    | 10      | mA    | CE1, CE2 = VIH<br>BBlock Erase Suspended                                                                                                                                                                             |
| ICC4   | VCC Program Current         | 1     |      | 30   | 50      | mA    | Program in Progress                                                                                                                                                                                                  |
| ICC5   | VCC Erase Current           | 1     |      | 30   | 50      | mA    | Erase in Progress                                                                                                                                                                                                    |
| VIL    | Input Low Voltage           | 3     | -0.3 |      | 0.8     | V     |                                                                                                                                                                                                                      |
| VIH    | Input High Voltage          | 4     | 2.4  |      | VCC+0.3 | V     |                                                                                                                                                                                                                      |
| VOL    | Output Low Voltage          |       |      |      | 0.45    | V     | IOL = 2.1mA                                                                                                                                                                                                          |
| VOH    | Output High Voltage         |       | 2.4  |      |         | V     | IOH = -400uA                                                                                                                                                                                                         |

**DC CHARACTERISTICS = 0°C to 70°C, VCC = 5V±10%(CONTINUE P.21)**
**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at VCC = 5.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. ICC3 is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of ICC3 and ICC1/2.
3. VIL min. = -1.0V for pulse width ≤ 50ns.  
VIL min. = -2.0V for pulse width ≤ 20ns.
4. VIH max. = VCC + 1.5V for pulse width ≤ 20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

**AC CHARACTERISTICS—READ OPERATIONS**

| SYMBOL | DESCRIPTIONS                              | 29F8100-12 |      | 29F8100-15 |      | UNIT | CONDITIONS                        |
|--------|-------------------------------------------|------------|------|------------|------|------|-----------------------------------|
|        |                                           | MIN.       | MAX. | MIN.       | MAX. |      |                                   |
| tACC   | Address to Output Delay                   |            | 120  |            | 150  | ns   | $\overline{CE}=\overline{OE}=VIL$ |
| tCE    | $\overline{CE}$ to Output Delay           |            | 120  |            | 150  | ns   | $\overline{OE}=VIL$               |
| tOE    | $\overline{OE}$ to Output Delay           |            | 60   |            | 70   | ns   | $\overline{CE}=VIL$               |
| tDF    | $\overline{OE}$ High to Output Delay      | 0          | 55   | 0          | 55   | ns   | $\overline{CE}=VIL$               |
| tOH    | Address to Output hold                    | 0          |      | 0          |      | ns   | $\overline{CE}=\overline{OE}=VIL$ |
| tBACC  | $\overline{BYTE}$ to Output Delay         |            | 120  |            | 150  | ns   | $\overline{CE}=\overline{OE}=VIL$ |
| tBHZ   | $\overline{BYTE}$ Low to Output in High Z |            | 55   |            | 55   | ns   | $\overline{CE}=VIL$               |
| tDPR   | Deep Power-Down Recovery                  |            | 700  |            | 800  | ns   |                                   |

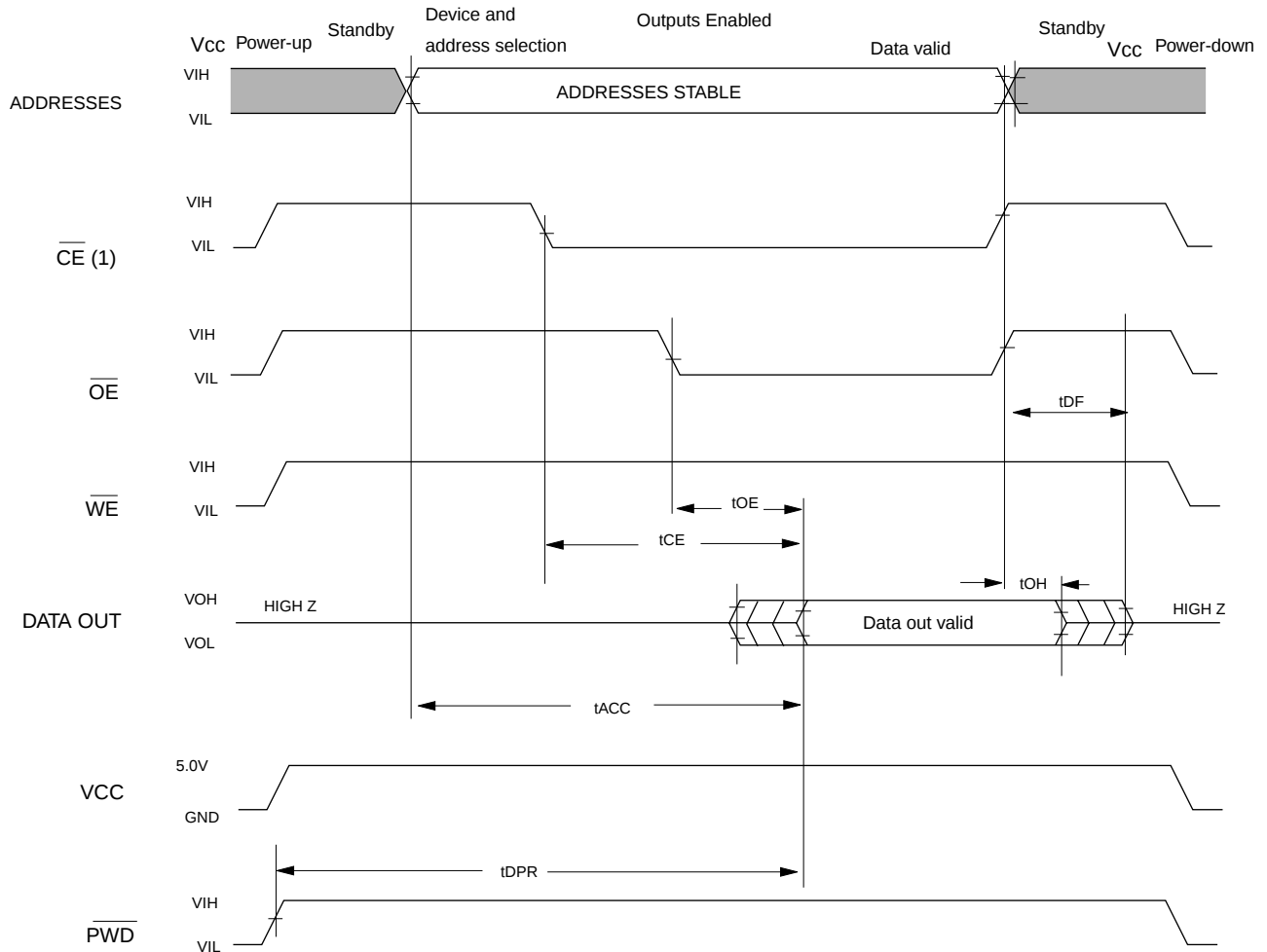
**TEST CONDITIONS:**

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: 10ns
- Output load: 1TTL gate+100pF(Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

**NOTE:**

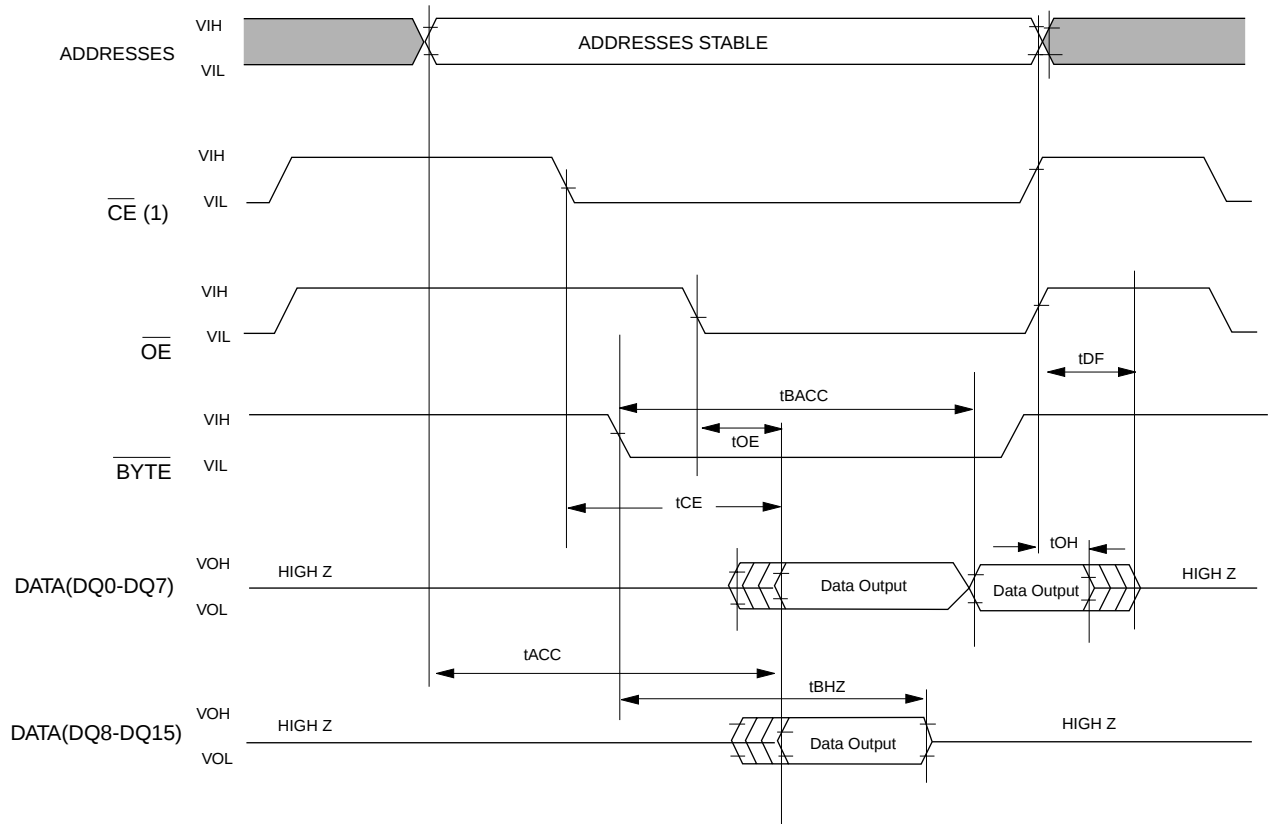
1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

**Figure 5. READ TIMING WAVEFORMS**



**NOTE:**

1.  $\overline{CE}$  is defined as the latter of  $\overline{CE1}$  or  $\overline{CE2}$  going Low or the first of  $\overline{CE1}$  or  $\overline{CE2}$  going High.
2. For real world application,  $\overline{BYTE}$  pin should be either static high (word mode) or static low (byte mode); dynamic switching of  $\overline{BYTE}$  pin is not recommended.

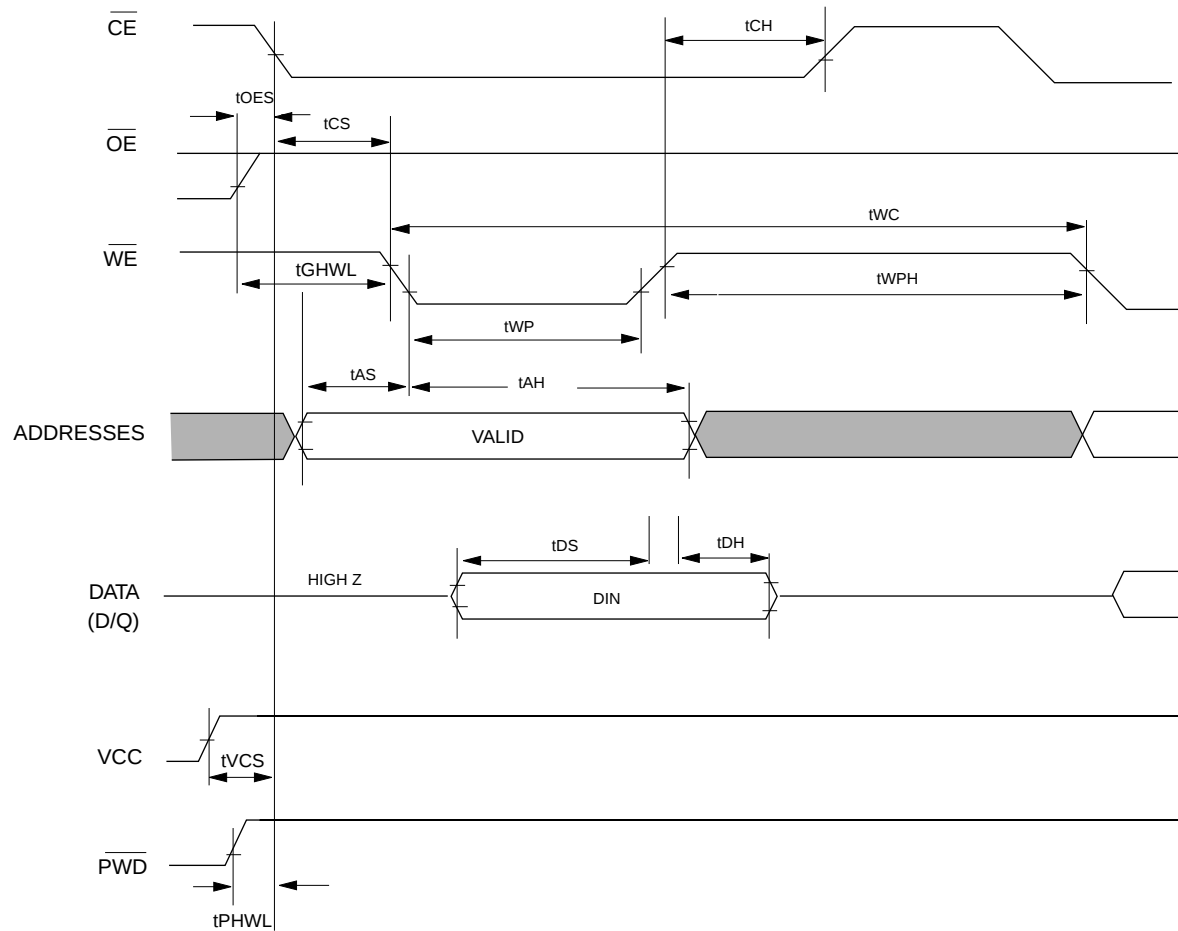
**Figure 6.  $\overline{\text{BYTE}}$  TIMING WAVEFORMS**


NOTE:

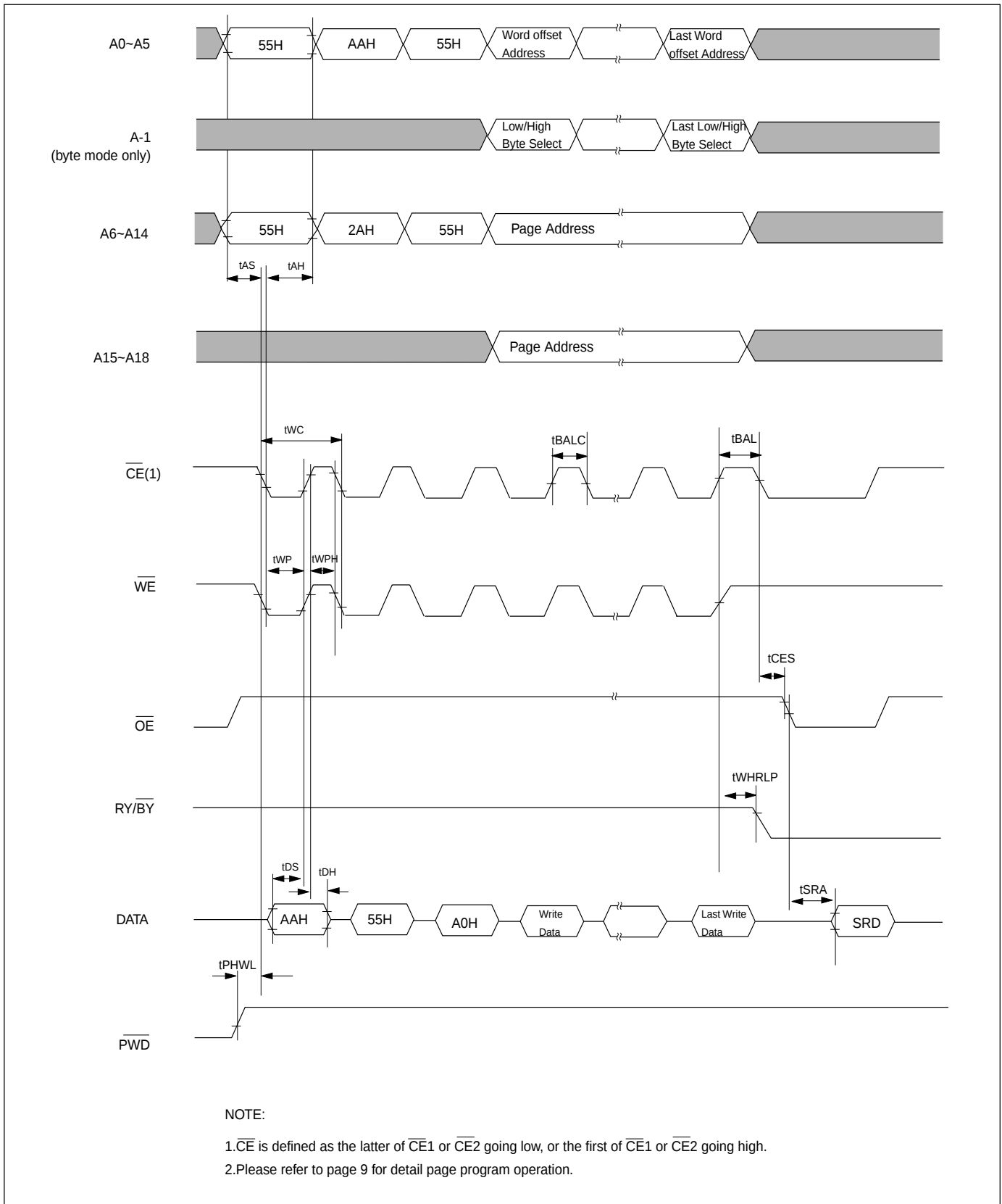
1.  $\overline{\text{CE}}$  is defined as the latter of  $\overline{\text{CE}}1$  or  $\overline{\text{CE}}2$  going Low or the first of  $\overline{\text{CE}}1$  or  $\overline{\text{CE}}2$  going High.

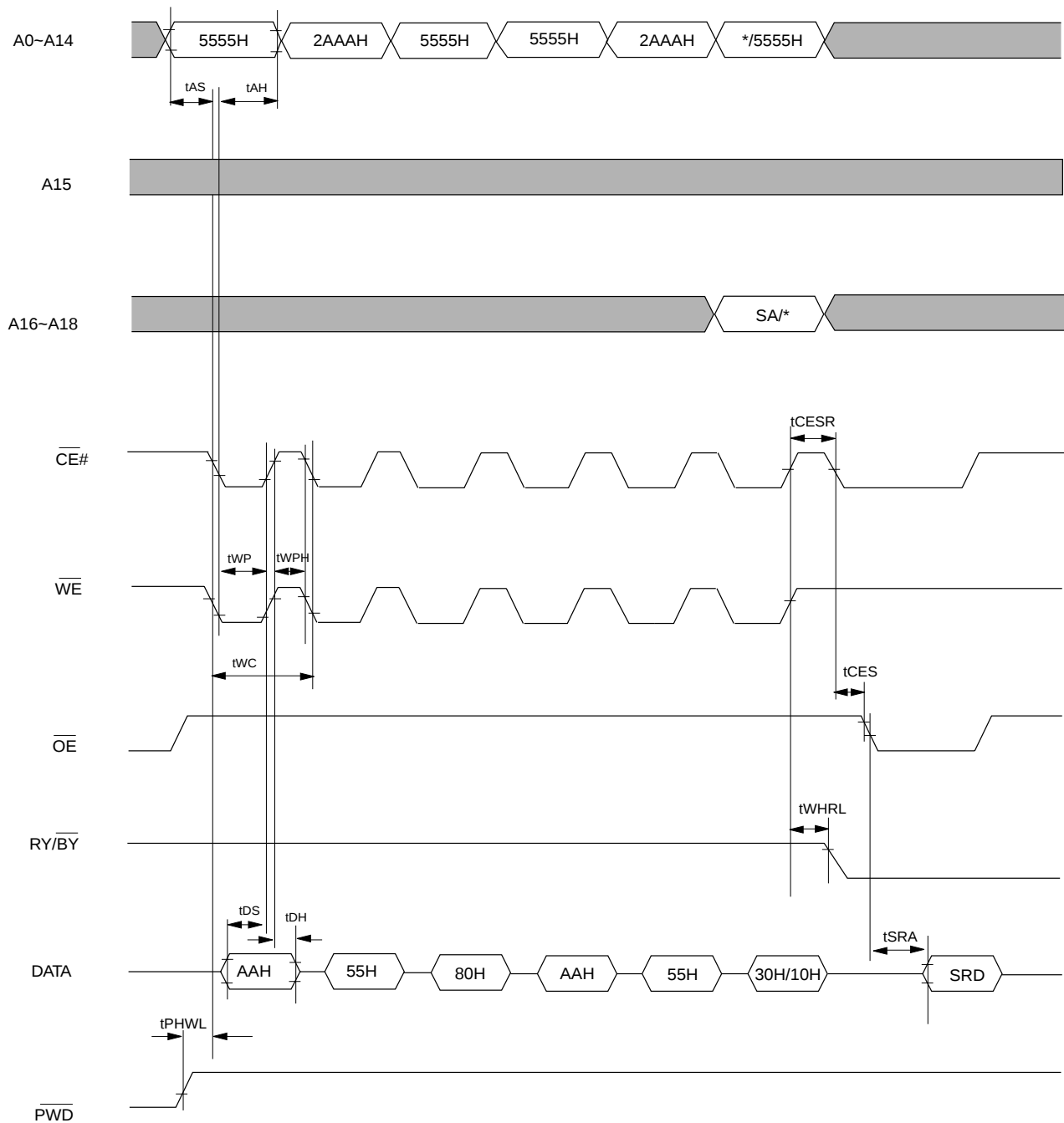
**AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS**

| SYMBOL | DESCRIPTION                                                                                                    | 29F8100-12 |      | 29F8100-15 |      | UNIT |
|--------|----------------------------------------------------------------------------------------------------------------|------------|------|------------|------|------|
|        |                                                                                                                | MIN.       | MAX. | MIN.       | MAX. |      |
| tWC    | Write Cycle Time                                                                                               | 120        |      | 150        |      | ns   |
| tAS    | Address Setup Time                                                                                             | 0          |      | 0          |      | ns   |
| tAH    | Address Hold Time                                                                                              | 50         |      | 60         |      | ns   |
| tDS    | Data Setup Time                                                                                                | 50         |      | 60         |      | ns   |
| tDH    | Data Hold Time                                                                                                 | 10         |      | 10         |      | ns   |
| tOES   | Output Enable Setup Time                                                                                       | 0          |      | 0          |      | ns   |
| tCES   | $\overline{\text{CE}}$ Setup Time                                                                              | 0          |      | 0          |      | ns   |
| tGHWL  | Read Recover TimeBefore Write                                                                                  | 0          |      | 0          |      |      |
| tCS    | $\overline{\text{CE}}$ Setup Time                                                                              | 0          |      | 0          |      | ns   |
| tCH    | $\overline{\text{CE}}$ Hold Time                                                                               | 0          |      | 0          |      | ns   |
| tWP    | Write Pulse Width                                                                                              | 50         |      | 60         |      | ns   |
| tWPH   | Write Pulse Width High                                                                                         | 50         |      | 50         |      | ns   |
| tBALC  | Byte(Word) Address Load Cycle                                                                                  | 0.3        | 30   | 0.3        | 30   | us   |
| tBAL   | Byte(Word) Address Load Time                                                                                   | 100        |      | 100        |      | us   |
| tSRA   | Status Register Access Time                                                                                    | 120        |      | 150        |      | ns   |
| tCESR  | $\overline{\text{CE}}$ Setup before S.R. Read                                                                  | 100        |      | 100        |      | ns   |
| tWHRL  | $\overline{\text{WE}}$ High to $\overline{\text{RY}}/\overline{\text{BY}}$ Going Low                           | 100        |      | 100        |      | ns   |
| tWHRLP | $\overline{\text{WE}}$ High to $\overline{\text{RY}}/\overline{\text{BY}}$ Going Low<br>(in Page Program mode) | 100.1      |      | 100.1      |      | us   |
| tPHWL  | $\overline{\text{PWD}}$ High Recovery to $\overline{\text{WE}}$ Going Low                                      | 1          |      | 1          |      | us   |
| tVCS   | VCC Setup Time                                                                                                 | 2          |      | 2          |      | us   |

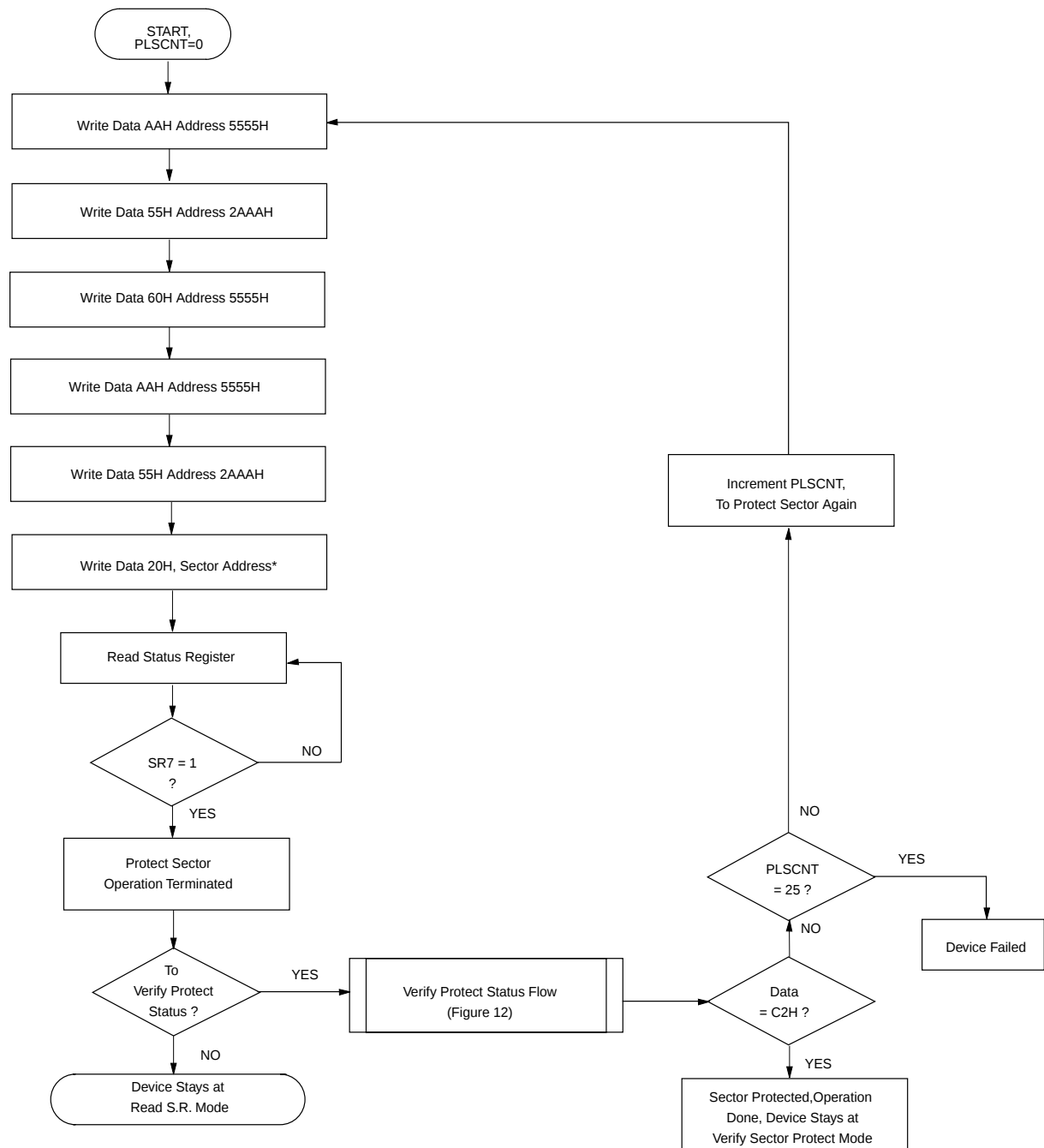
**Figure 7. COMMAND WRITE TIMING WAVEFORMS**

**NOTE:**

1.  $\overline{\text{BYTE}}$  pin is treated as Address pin. All timing specifications for  $\overline{\text{BYTE}}$  pin are the same as those for address pin.
2.  $\overline{\text{BYTE}}$  pin is sampled on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$  during the 3rd command write bus cycle; for real world application,  $\overline{\text{BYTE}}$  pin should be either static high(word mode) or static low(byte mode).

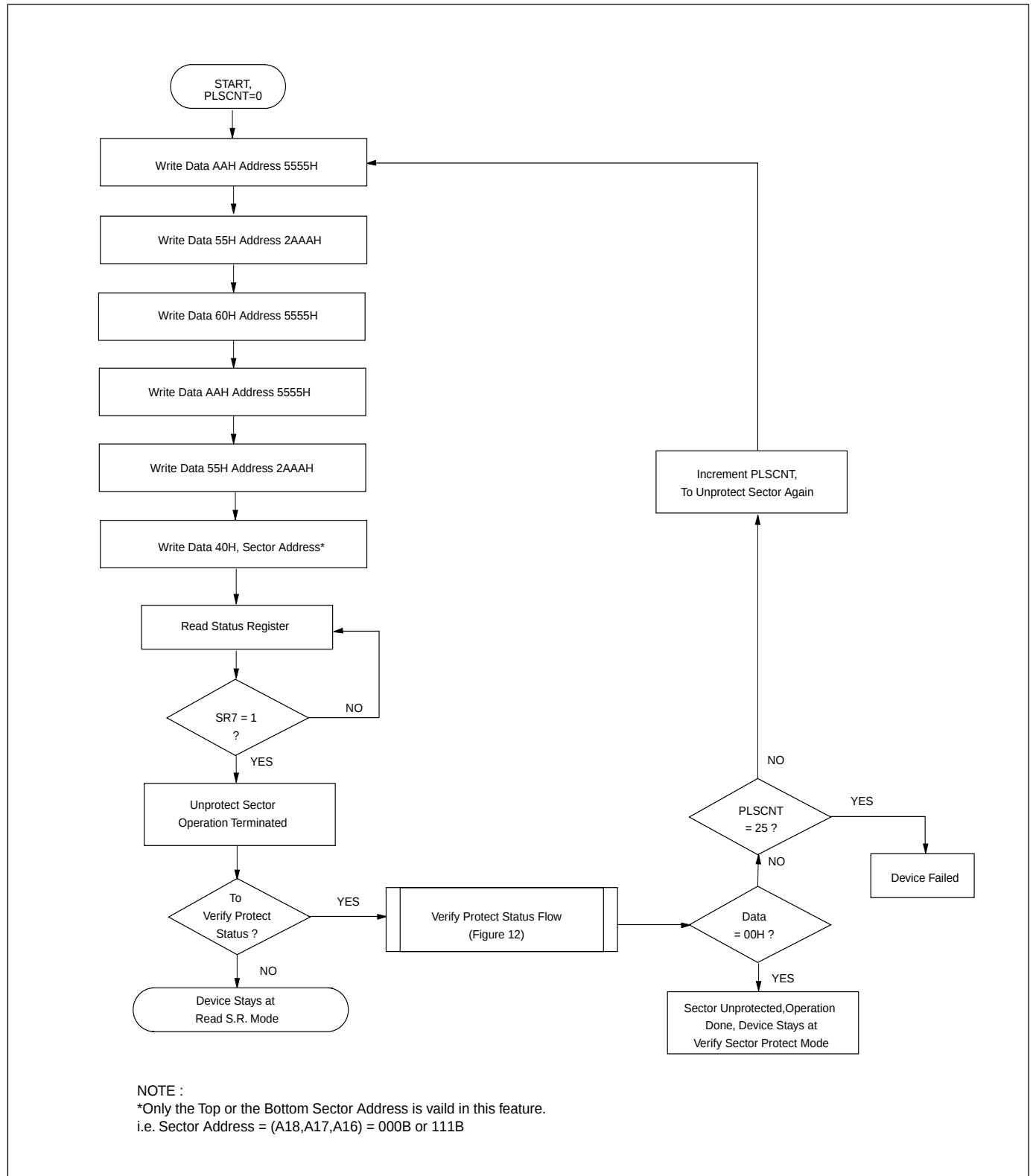
**Figure 8. AUTOMATIC PAGE PROGRAM TIMING WAVEFORMS**


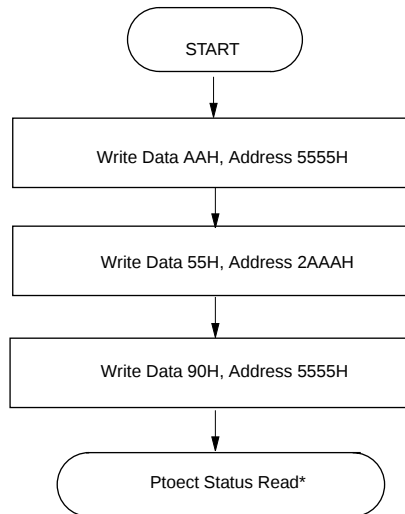
**Figure 9. AUTOMATIC SECTOR/CHIP ERASE TIMING WAVEFORMS**

**NOTES:**

1.  $\overline{CE\#}$  is defined as the latter of  $\overline{CE1}$  or  $\overline{CE2}$  going low, or the first of  $\overline{CE1}$  or  $\overline{CE2}$  going high.
2. "\*" means "don't care" in this diagram.
3. "SA" means "Sector Address".

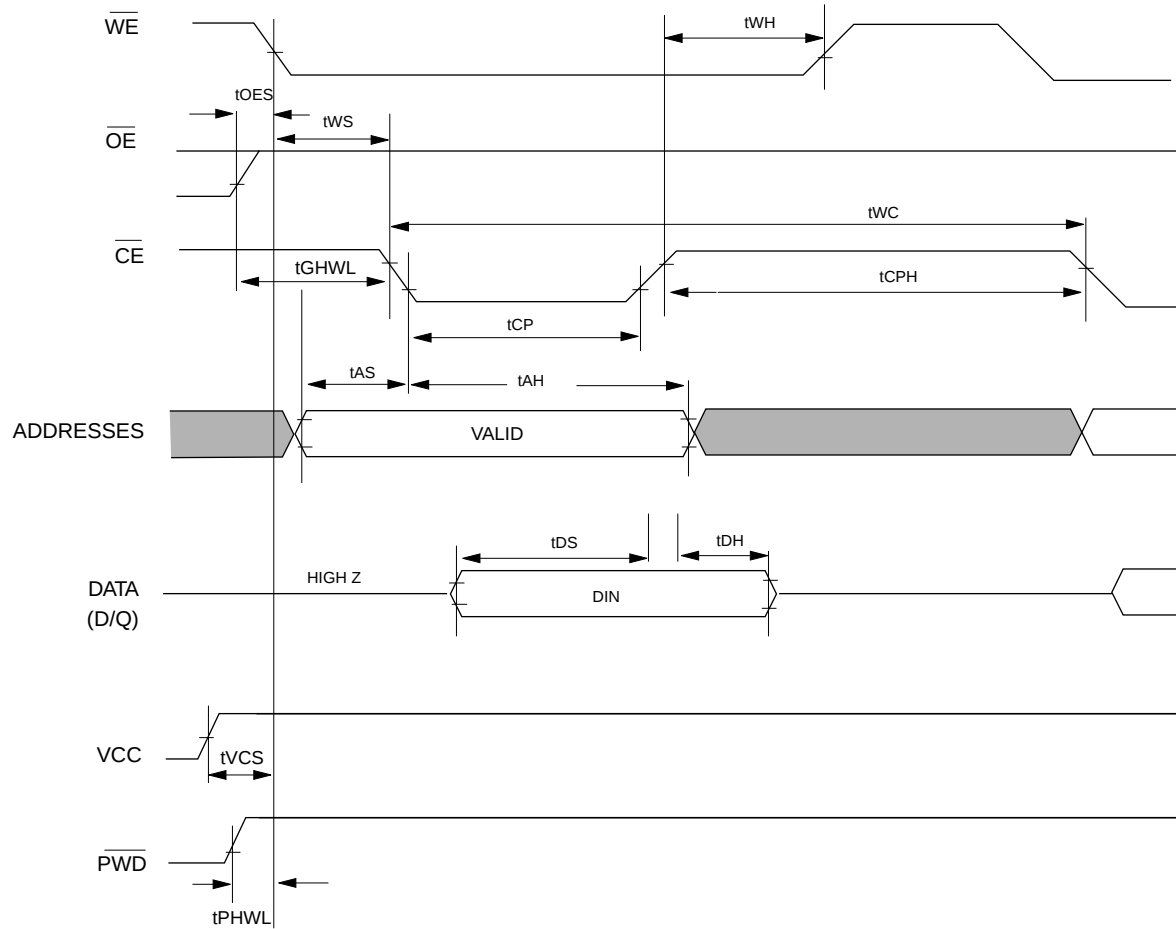
**Figure 10. SECTOR PROTECTION ALGORITHM**


**NOTE :**  
 \*Only the Top or the Bottom Sector Address is valid in this feature.  
 i.e. Sector Address = (A18,A17,A16) = 000B or 111B

**Figure 11. SECTOR UNPROTECT ALGORITHM**


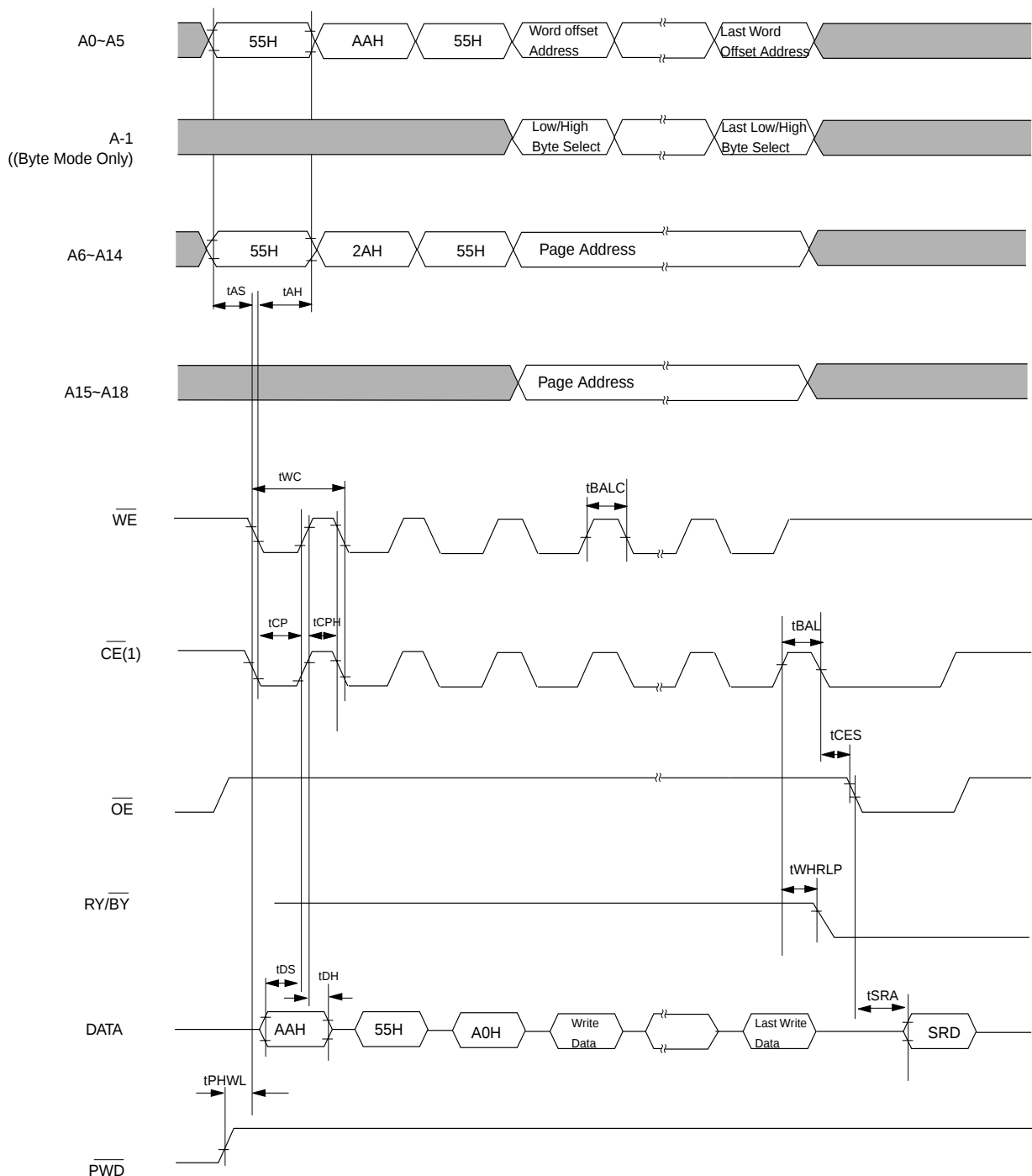
**Figure 12. VERIFY SECTOR PROTECT FLOW CHART**


- \* 1. Protect Status:  
 Data Outputs C2H as Protected Sector Verified Code.  
 Data Outputs 00H as Unprotected Sector Verified Code.
2. Sepecified address will be either  
 (A18,A17,A16,A1,A0) = (00010) or (11110),  
 the rest of the address pins are don't care.
3. Silicon ID can be read via this Flow Chart.  
 Refer to Table 4.

**Figure 13. COMMAND WRITE TIMING WAVEFORMS(Alternate  $\overline{\text{CE}}$  Controlled)**

**NOTE:**

1.  $\overline{\text{BYTE}}$  pin is treated as Address pin. All timing specifications for  $\overline{\text{BYTE}}$  pin are the same as those for address pin.
2.  $\overline{\text{BYTE}}$  pin is sampled on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$  during the 3rd command write bus cycle; for real world application,  $\overline{\text{BYTE}}$  pin should be either static high(word mode) or static low(byte mode).

**Figure 14. AUTOMATIC PAGE PROGRAM TIMING WAVEFORM(Alternate  $\overline{CE}$  Controlled)**



**NOTE:**

1.  $\overline{CE}$  is defined as the latter of  $\overline{CE1}$  or  $\overline{CE2}$  going low, or the first of  $\overline{CE1}$  or  $\overline{CE2}$  going high.
2. Please refer to page 9 for detail page program operation.

**ERASE AND PROGRAMMING PERFORMANCE(Note 2)**

| PARAMETER              | LIMITS |      |               | UNITS  |
|------------------------|--------|------|---------------|--------|
|                        | MIN.   | TYP. | MAX. (Note 1) |        |
| Chip/Sector Erase Time |        | 150  | (Note 2)      | ms     |
| Page Programming Time  |        | 3    | (Note 3)      | ms     |
| Chip Programming Time  |        | 24   | 75            | sec    |
| Erase/Program Cycles   | 10,000 |      |               | Cycles |
| Byte Program Time      |        | 24   |               | us     |

\*Note 1: MAX values are all evaluated with polling the status in stead of internal state machine time out.

\*Note 2: The IC internal state machine is set 2000 ms as maximum chip/sector erase time out.

\*Note 3: We set 60 ms as production test condition, whereas, the IC internal state machine is set 150 ms as maximum programming time out.

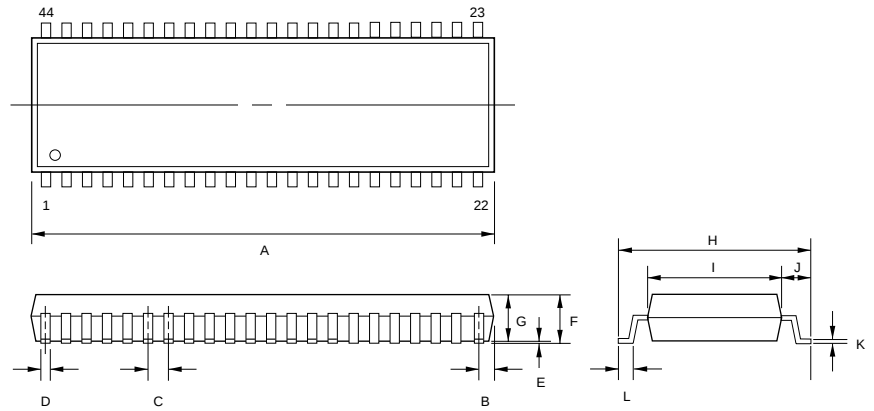
**LATCHUP CHARACTERISTICS**

|                                                                               | MIN.   | MAX.       |
|-------------------------------------------------------------------------------|--------|------------|
| Input Voltage with respect to GND on all pins except I/O pins                 | -1.0V  | 13.5V      |
| Input Voltage with respect to GND on all I/O pins                             | -1.0V  | Vcc + 1.0V |
| Current                                                                       | -100mA | +100mA     |
| Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time. |        |            |

## 44-PIN PLASTIC SOP

| ITEM | MILLIMETERS      | INCHES             |
|------|------------------|--------------------|
| A    | 28.70 max.       | 1.130 max.         |
| B    | 1.10 [REF]       | .043 [REF]         |
| C    | 1.27 [TP]        | .050 [TP]          |
| D    | .40 ± .10 [Typ.] | .016 ± .004 [Typ.] |
| E    | .010 min.        | .004 min.          |
| F    | 3.00 max.        | .118 max.          |
| G    | 2.80 ± .13       | .110 ± .005        |
| H    | 16.04 ± .30      | .631 ± .012        |
| I    | 12.60            | .496               |
| J    | 1.72             | .068               |
| K    | .15 ± .10 [Typ.] | .006 ± .004 [Typ.] |
| L    | .80 ± .20        | .031 ± .008        |

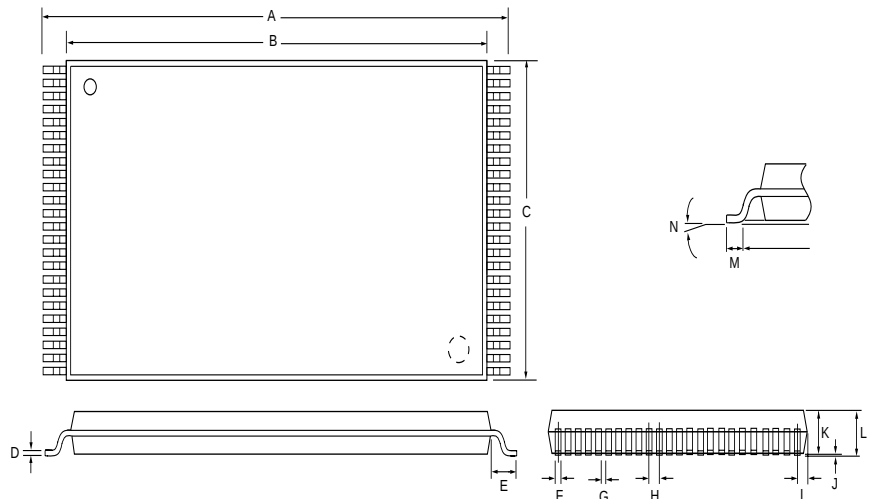
**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



## 48-PIN PLASTIC TSOP

| ITEM | MILLIMETERS | INCHES      |
|------|-------------|-------------|
| A    | 20.0 ± .20  | .787 ± .008 |
| B    | 18.40 ± .10 | .724 ± .004 |
| C    | 12.20 max.  | .480 max.   |
| D    | 0.15 [Typ.] | .006 [Typ.] |
| E    | .80 [Typ.]  | .031 [Typ.] |
| F    | .20 ± .10   | .008 ± .004 |
| G    | .30 ± .10   | .012 ± .004 |
| H    | .50 [Typ.]  | .020 [Typ.] |
| I    | .45 max.    | .018 max.   |
| J    | 0 ~ .20     | 0 ~ .008    |
| K    | 1.00 ± .10  | .039 ± .004 |
| L    | 1.27 max.   | .050 max.   |
| M    | .50         | .020        |
| N    | 0 ~ 5°      | .500        |

**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



**Note. Revision History**

| <b>Revision No.</b> | <b>Description</b>                                            | <b>Page</b> | <b>Date</b> |
|---------------------|---------------------------------------------------------------|-------------|-------------|
| 1.6                 | fast access time : 100ns                                      |             | 09/25/1996  |
| 1.7                 | removed fast access time : 100ns                              |             | 06/20/1997  |
| 1.8                 | Write-Erase cycles change from 1,000/10,000 to 100,000.       |             | 10/29/1997  |
| 1.9                 | Erase and Programming Performance table updated Endurance:10K |             | 04/09/1998  |
| 2.0                 | Modify PIN CONFIGURATIONS A19-->A19*                          | P2          | 01/22/1999  |



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