MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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M29F040

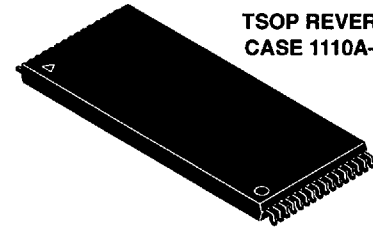
Advance Information

4M CMOS Sector Erase Flash Memory

PLCC
CASE 989A–01

TSOP
CASE 1110–01

TSOP REVERSE
CASE 1110A–01



The M29F040 is a 4M, 5 V-only, sector erase flash memory organized as 512K bytes of 8 bits each. The M29F040 is offered in JEDEC-standard 32-pin packages.

- 5.0 V ± 10% Read, Write and Erase Minimizes System Level Power Requirements
- JEDEC Industry Standard Pin-Out and Architecture
- Compatible with JEDEC-Standard (E^2PROM) Commands
- Minimum 100,000 Write/Erase Cycles
- Sector Erase Architecture:
  - Eight Equal Size Sectors of 64K Bytes Each
  - Any Combination of Sectors can be Concurrently Erased
  - Supports Full Chip Erase
- Embedded Erase™ Algorithms Allow Automatic Preprogram and Erase at any Sector
- Embedded Program™ Algorithms Allow Automatic Write and Verify of Data at a Specified Address
- $\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion
- Sector Protection Allows Hardware Disable of Sectors from Write or Erase Operations
- Low V_{CC} Write Inhibit ≤ 3.2 V
- Suspend Erase/Resume Feature to Allow a Read Cycle in Another Sector Within the Same Device
- Fast Access Time: M29F040-75 = 70 ns (Max)
  M29F040-90 = 90 ns (Max)
  M29F040-12 = 120 (Max)
- Low Active Power Dissipation: M29F040-75 = 315 mW
  M29F040-90 = 330 mW
  M29F040-12 = 330 mW
- Low Standby Power Dissipation:
  - TTL Levels: M29F040-75 = 5.3 mW
    M29F040-90 = 5.5 mW
    M29F040-12 = 5.5 mW
  - CMOS Levels: M29F040-75 = 0.53 mW
    M29F040-90 = 0.55 mW
    M29F040-12 = 0.55 mW

PIN NAMES	
A0 – A18	Address Input
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	Power Supply
V_{SS}	Ground

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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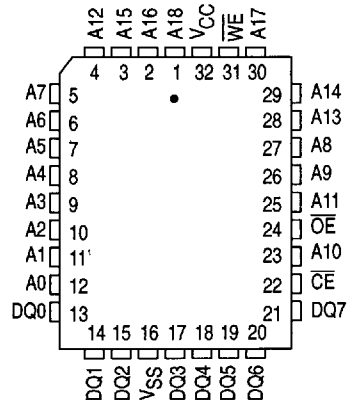
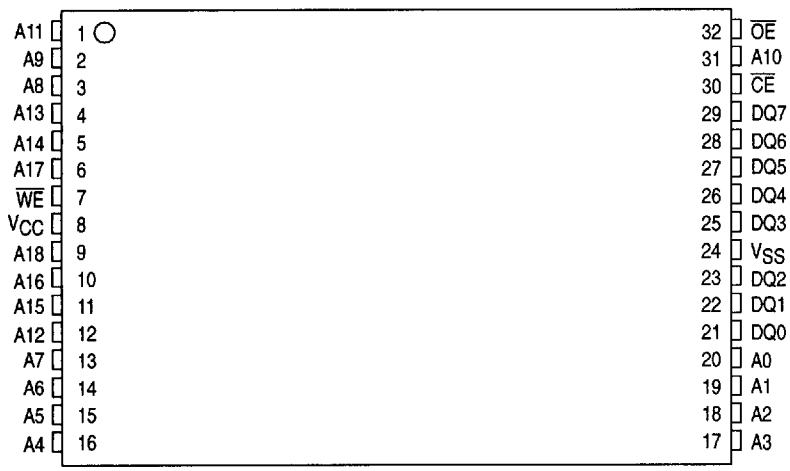
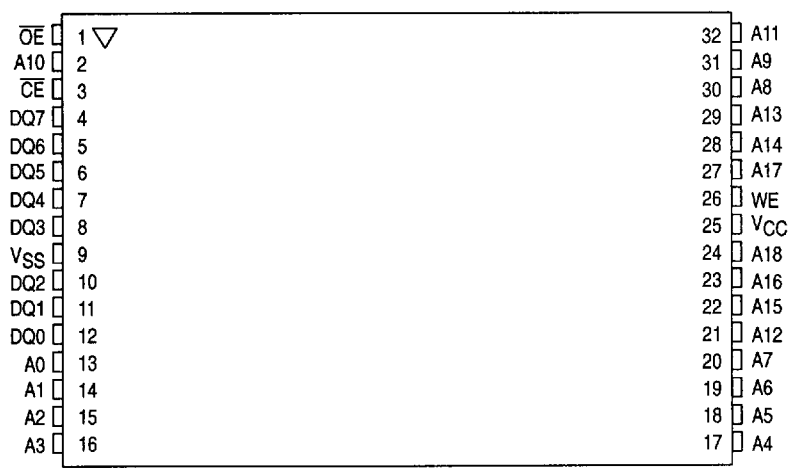
PIN ASSIGNMENTS
PLCC



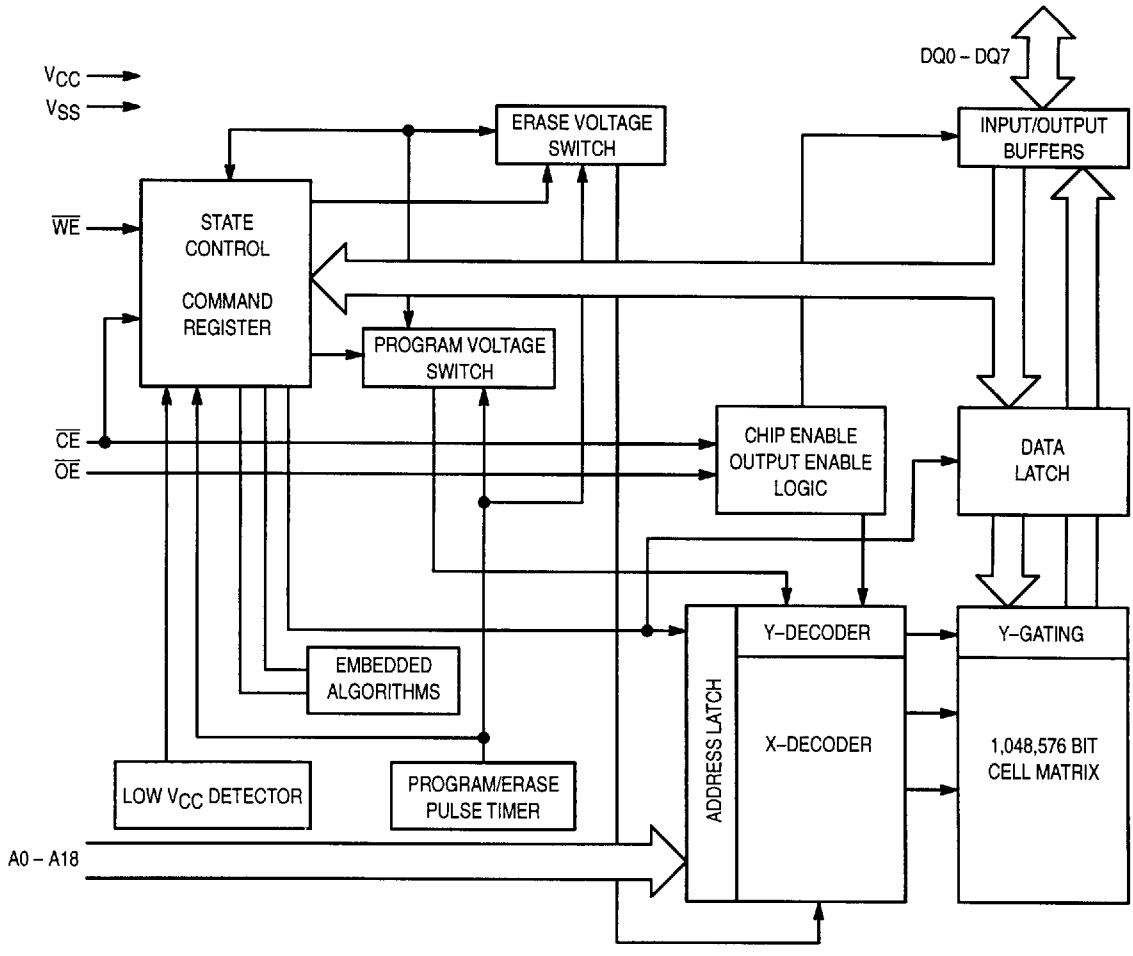
TSOP
STANDARD PINOUT



TSOP
REVERSE PINOUT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Notes 1 through 4)

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 1)	V_{CC}	– 2.0 to + 7	V
Voltage Relative to V_{SS}: All Pins Except A9, $\overline{CE}$, and $\overline{OE}$ (Note 1) A9, $\overline{CE}$, and $\overline{OE}$	V_{in}, V_{out}	 – 2.0 to + 7 – 2.0 to + 14	V
Output Short Circuit Current (Note 3)	I_{out}	200	mA
Power Dissipation	P_D	420	mW
Ambient Temperature with Power Applied	T_A	– 55 to + 125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 – 65 to + 150 – 65 to + 125	°C

NOTES:

1. Minimum dc voltage on input or I/O pins is – 0.5 V. During voltage transitions, inputs may undershoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. Minimum dc voltage on pin A9, $\overline{CE}$, and $\overline{OE}$ is – 0.5 V. During voltage transitions, A9, $\overline{CE}$, and $\overline{OE}$ may undershoot V to – 2.0 V for periods of up to 20 ns. Maximum dc input voltage on A9, $\overline{CE}$, and $\overline{OE}$ is + 13.5 V which may overshoot to 14.0 V_{SS} for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be longer than one second.
4. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

OPERATING RANGES (See Note)

Rating	Symbol	Value	Unit
Supply Voltages M29F040–75 = 70 ns M29F040–90 = 90 ns, M29F040–12 = 120 ns	V_{CC}	 + 4.75 to + 5.25 + 4.50 to + 5.50	V
Operating Temperature Range Commercial Industrial	T_C	 0 to + 70 – 40 to + 85	°C

NOTE: Operating ranges define those limits between which the functionality of the device is guaranteed.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	– 1.0 V	V_{CC} + 1.0 V
V_{CC} Current	– 100 mA	+ 100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

DC OPERATING CONDITIONS AND CHARACTERISTICS

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Active Current ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$)	I_{CC1}	—	40	mA	1
V_{CC} Active Current ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$)	I_{CC2}	—	60	mA	2, 3
V_{CC} Standby Current TTL/NMOS Levels ($V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$) CMOS Levels ($V_{CC} = V_{CC}$ max, $\overline{CE} = V_{CC} \pm 0.5$ V)	I_{CC3}	 — —	 1.0 100	 mA µA	
Input Load Current ($V_{in} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max)	I_{LI}	—	± 1.0	µA	
A9, $\overline{CE}$, and $\overline{OE}$ Input Load Current ($V_{CC} = V_{CC}$ max, A9, $\overline{CE}$, and $\overline{OE}$ = 12.5 V)	I_{LIT}	—	50	µA	
Output Leakage Current ($V_{out} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max)	I_{LO}	—	± 1.0	µA	
Input Low Level	V_{IL}	−0.5	0.8	V	
Input High Voltage TTL/NMOS Levels CMOS Levels	V_{IH}	 2 0.7 x V_{CC}	 V_{CC} + 0.5 V_{CC} + 0.3	V	
Voltage for Autoselect and Sector Protect (V_{CC} = 5.0 V)	V_{ID}	11.5	12.5	V	
Output Low Voltage (I_{OL} = 12 mA, $V_{CC} = V_{CC}$ min)	V_{OL}	—	0.45	V	
Output High Voltage TTL/NMOS Levels (I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min)	V_{OH}	 2.4	 —	V	
Output High Levels CMOS Levels (I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min) CMOS Levels (I_{OH} = −100 µA, $V_{CC} = V_{CC}$ min)	 V_{OH1} V_{OH2}	 0.85 V_{CC} V_{CC} − 0.4	 — —	V	
Low V_{CC} Lock-Out Voltage	V_{LKO}	3.2	4.2	V	

NOTES:
1. The I_{CC} current listed includes both the dc operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Not 100% tested.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

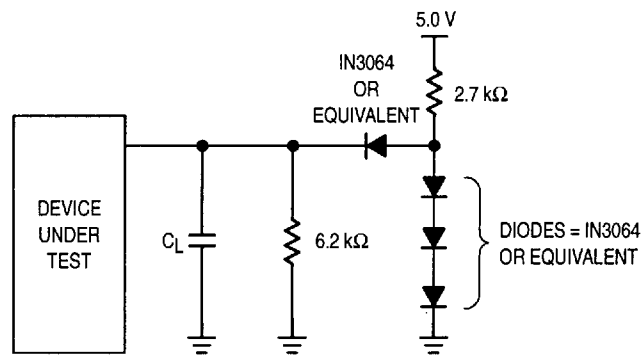
Parameter		Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0)	TSOP PLCC	C_{in}	6 4	7.5 6	pF
Control Pin Capacitance (V_{in} = 0)	TSOP PLCC	C_{in2}	7.5 8	9 12	pF
Output Capacitance (V_{out} = 0)	TSOP PLCC	C_{out}	8.5 8	12 12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ ONLY OPERATIONS CYCLE (See Note 1)

Parameter	Symbol		M29F040-75 (Note 1)		M29F040-90 (Note 2)		M29F040-12 (Note 2)		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	70	—	90	—	120	—	ns	4
Address to Output Delay, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	t_{AVQV}	t_{ACC}	—	70	—	90	—	120	ns	
Chip Enable to Output Delay, $\overline{OE}$ = V_{IL}	t_{ELQV}	t_{CE}	—	70	—	90	—	120	ns	
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	30	—	35	—	50	ns	
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	20	—	20	—	30	ns	3, 4
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	20	—	20	—	30	ns	3, 4
Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	0	—	0	—	0	—	ns	

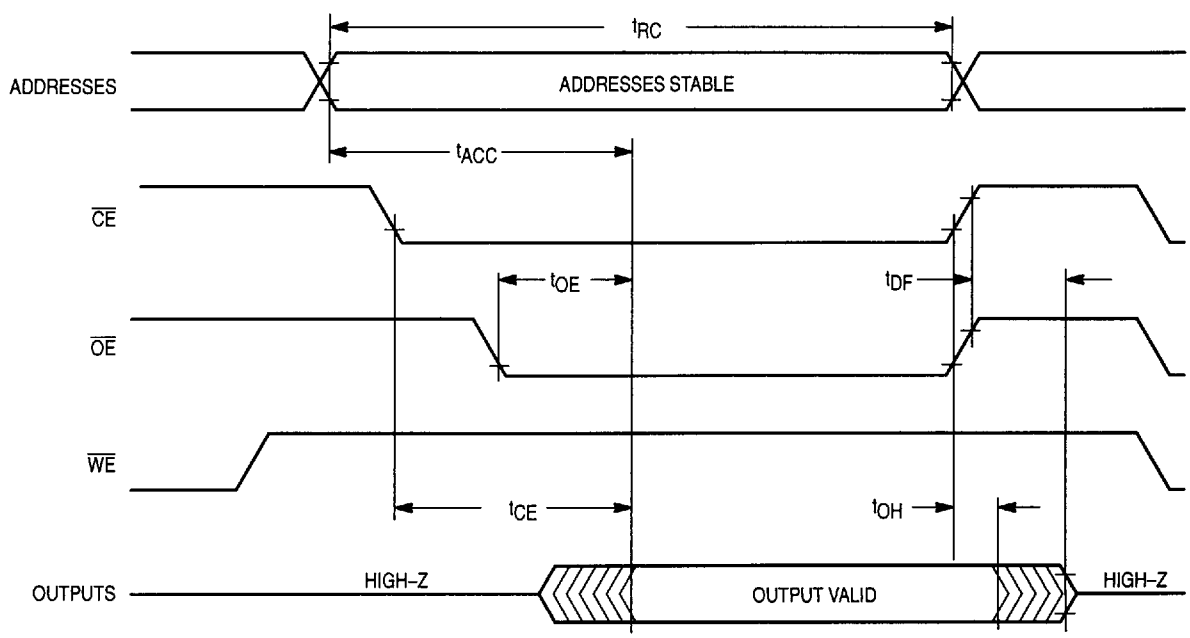
NOTES:
1. Test conditions — output load: one TTL gate and 30 pF; input rise and fall times: 5 ns; input pulse levels: 0 to 3 V; timing measurement reference level: input, 1.5 V; output, 1.5 V.
2. Test conditions — output load: one TTL gate and 100 pF; input rise and fall times: 20 ns; input pulse levels: 0.45 to 2.4 V; timing measurement reference level: input, 0.8 and 2.0 V; output, 0.8 and 2.0 V.
3. Output driver disable time.
4. Not 100% tested.



NOTE: C_L = 100 pF including jig capacitance.

Figure 1. Test Conditions

READ CYCLE

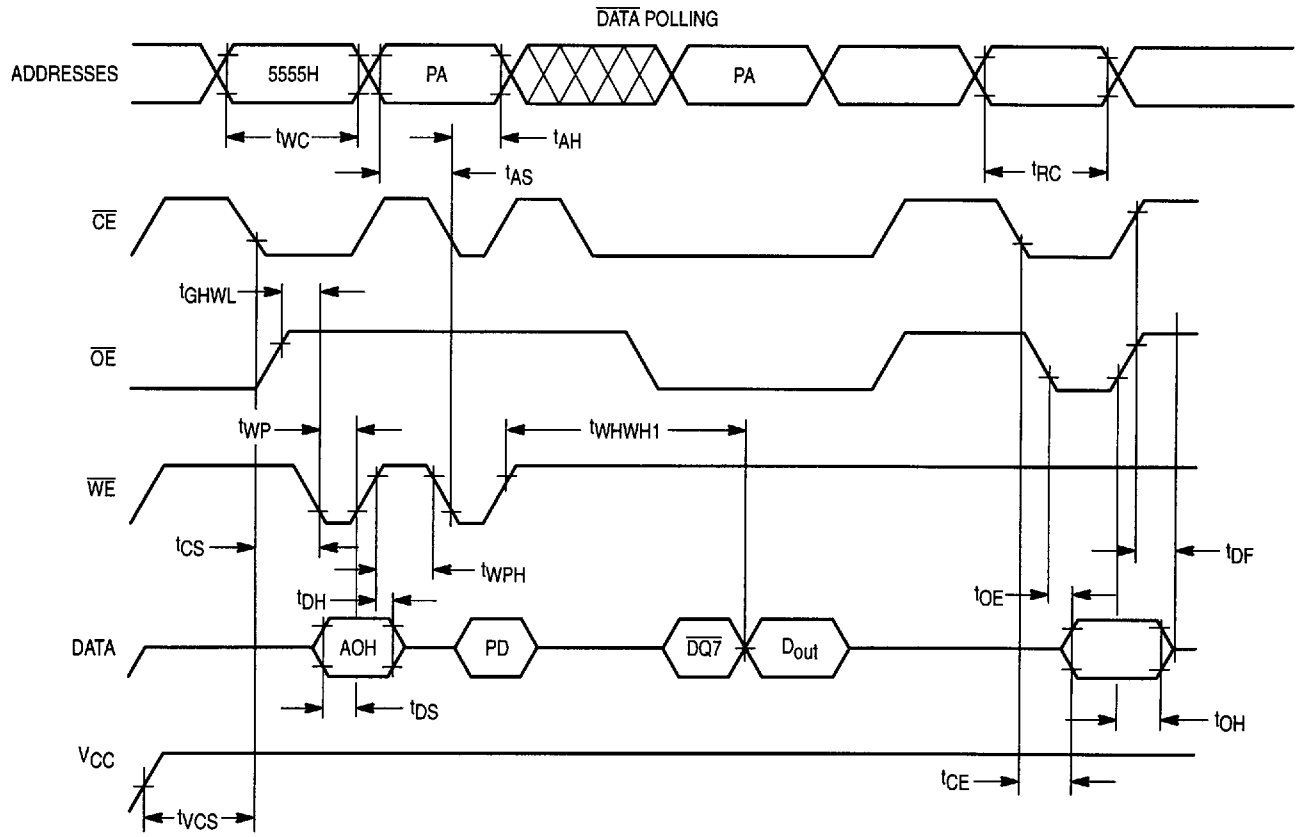


WRITE/ERASE/PROGRAM OPERATIONS (See Note 6)

Parameter	Symbol		M29F040-75		M29F040-90		M29F040-12		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	90	—	120	—	ns	1
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{WLAX}	t_{AH}	45	—	45	—	50	—	ns	
Data Setup Time	t_{DVWH}	t_{DS}	30		45		50		ns	
Data Hold Time	t_{WHQX}	t_{DH}	0	—	0	—	0	—	ns	
Output Enable Setup Time		t_{OES}	0	—	0	—	0	—	ns	
Output Enable Hold Time Read Toggle and $\overline{\text{Data}}$ Polling		t_{OEH}	0 10	— —	0 10	— —	0 10	— —	ns	1
Read Recovery Time Before Write	t_{GHWL}		0	—	0	—	0	—	ns	
$\overline{\text{CE}}$ Setup Time	t_{ELWL}	t_{CS}	0	—	0	—	0	—	ns	
$\overline{\text{CE}}$ Hold Time	t_{WHEH}	t_{CH}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	45	—	50	—	ns	
Write Pulse Width High	t_{WHWL}	t_{WPH}	20	—	20	—	20	—	ns	
Byte Programming Operation	t_{WHWH1}		16	—	16	—	16	—	µs	
Erase Operation	t_{WHWH2}		1.5	30	1.5	30	1.5	30	s	2
V_{CC} Setup Time		t_{VCS}	50	—	50	—	50	—	µs	1
Voltage Transition Time		t_{VLHT}	4	—	4	—	4	—	µs	1, 3
Write Pulse Width		t_{WPP}	100	—	100	—	100	—	µs	3
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{OESP}	4	—	4	—	4	—	µs	1, 3
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{CSP}	4	—	4	—	4	—	µs	1, 4
Chip Programming Time			—	50	—	50	—	50	s	5
Erase/Program Cycles			100k	—	100k	—	100k	—	cycles	

NOTES:
1. Not 100% tested.
2. This does not include the preprogramming time.
3. These timings are for Sector Protect/Unprotect operations.
4. This timing is only for Sector Unprotect.
5. 25°C, 5 V V_{CC}, 100,000 cycles.
6. When programming a "1" over a "0", the Embedded Algorithms allow for 48 ms byte program time.

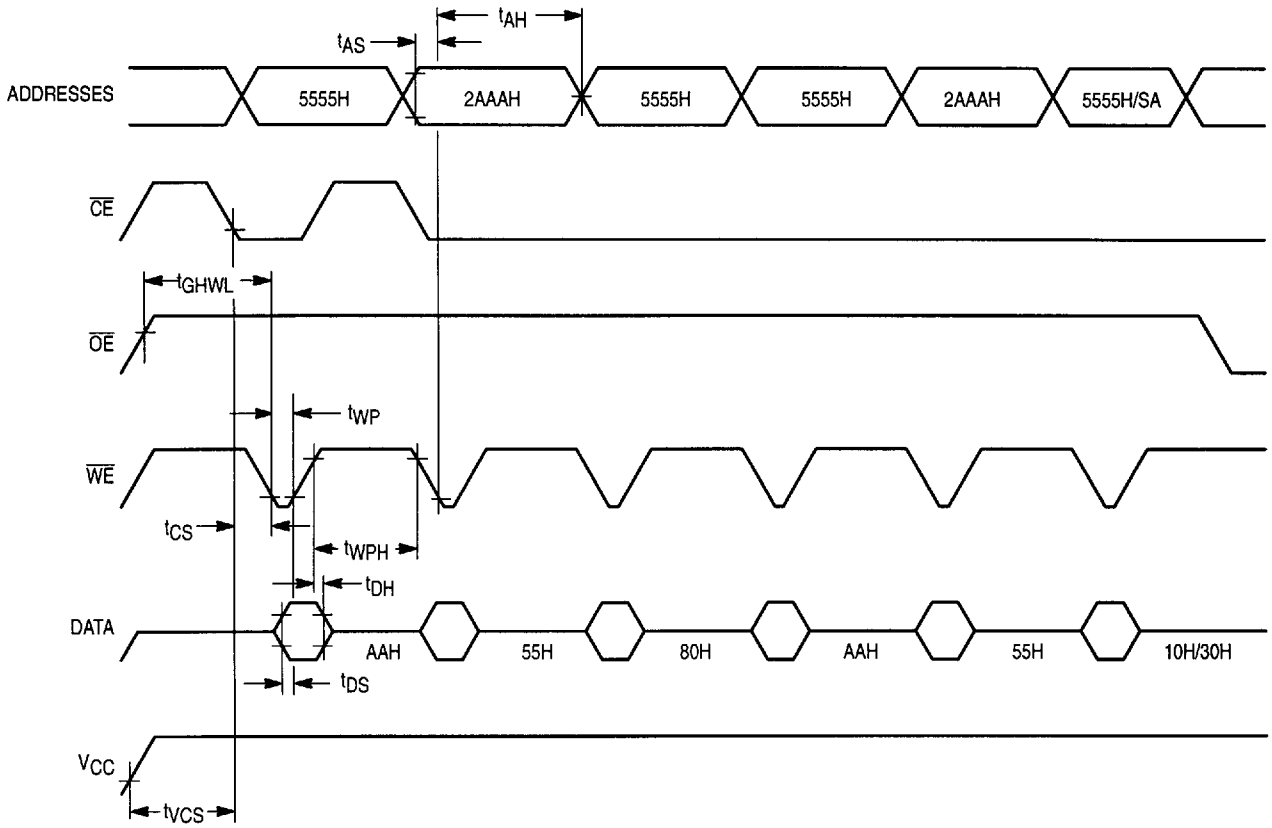
PROGRAM OPERATIONS



NOTES:

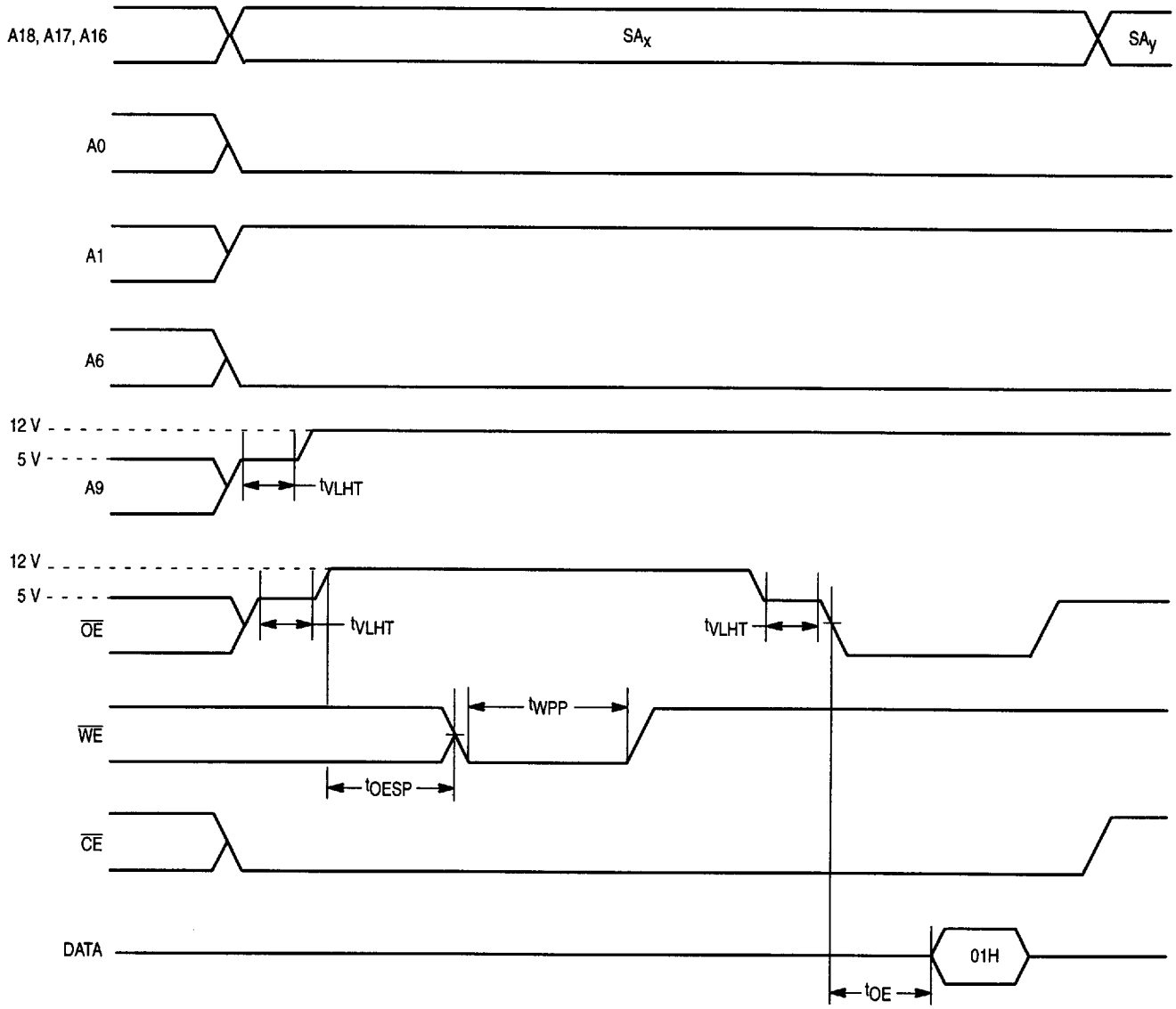
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. DQ7 is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

CHIP/SECTOR ERASE OPERATIONS



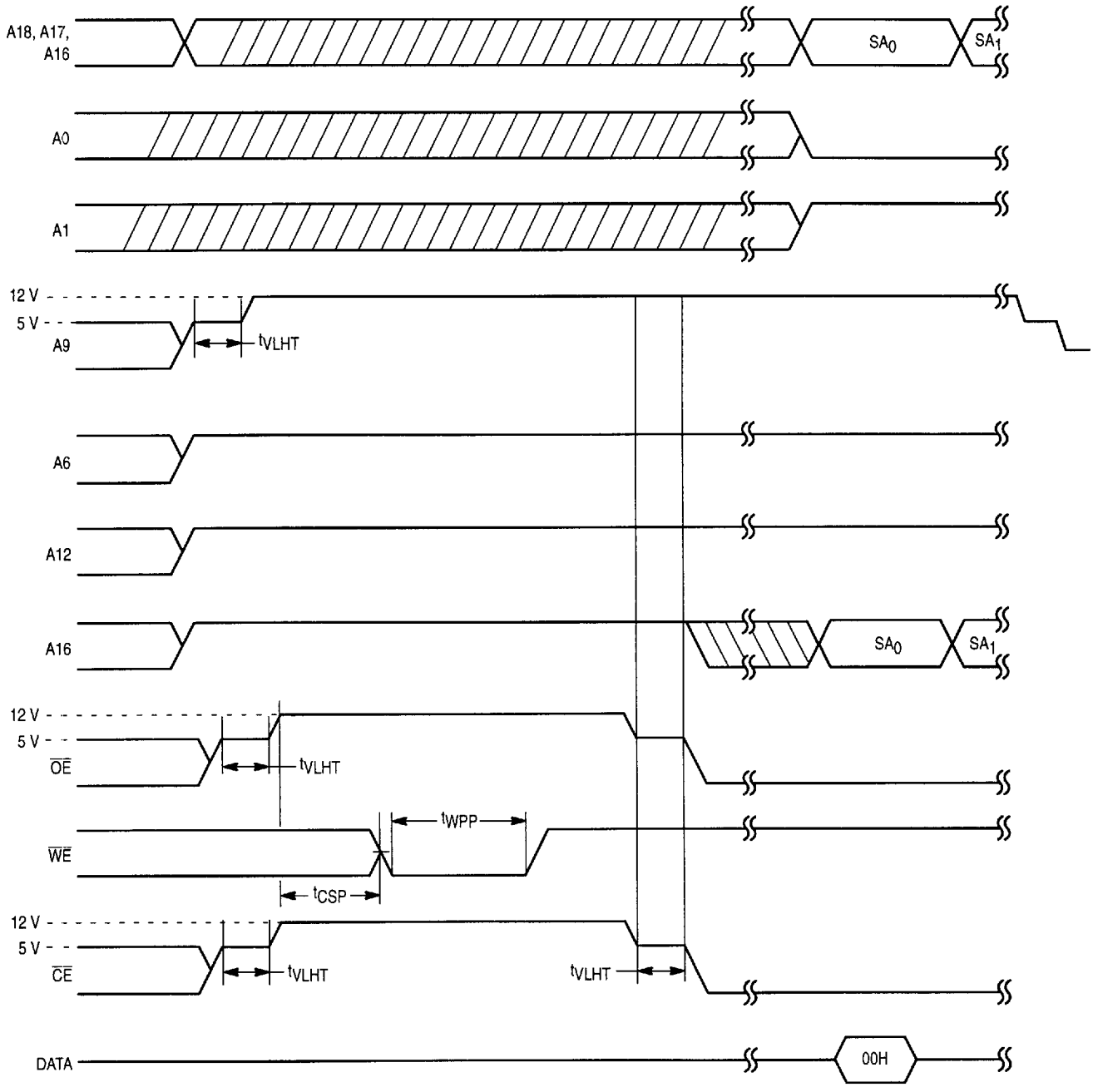
NOTE: SA is the sector address for Sector Erase.

SECTOR PROTECT CYCLE



SA_X = Sector Address for initial sector
SA_y = Sector Address for next sector

SECTOR UNPROTECT CYCLE

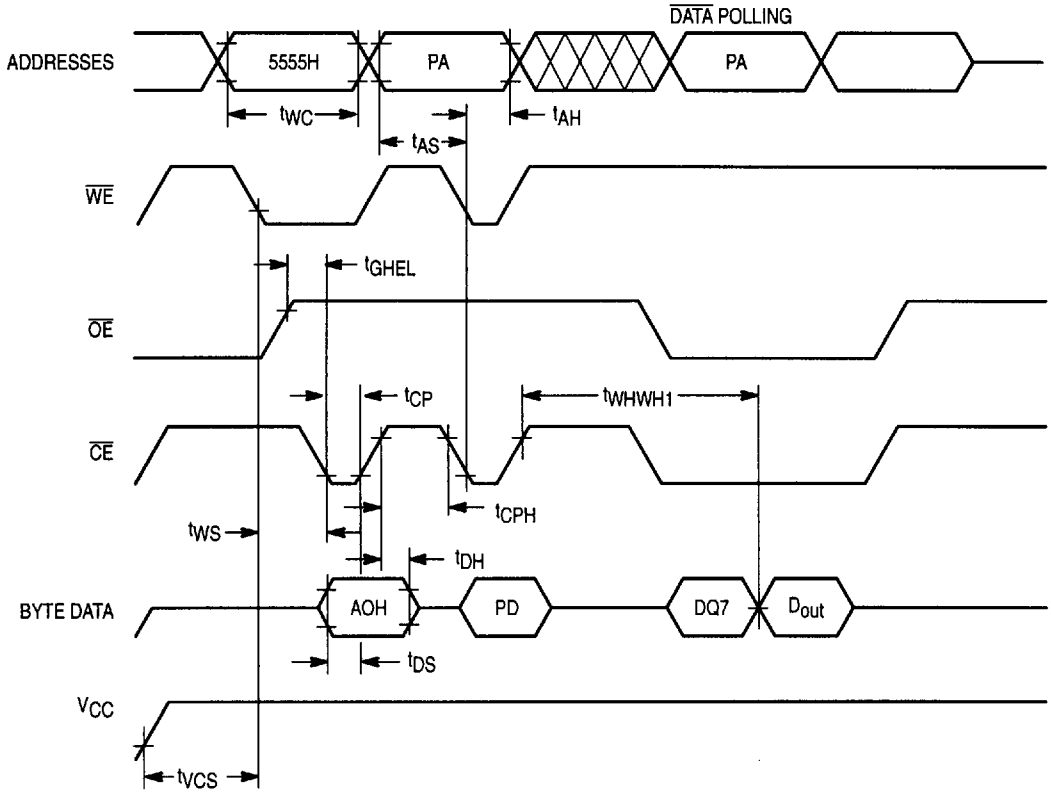


ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLES

Parameter	Symbol		M29F040-75		M29F040-90		M29F040-12		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	90	—	120	—	ns	1
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{ELAX}	t_{AH}	45	—	45	—	50	—	ns	
Data Setup Time	t_{DVEH}	t_{DS}	30		45		50		ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Output Enable Setup Time		t_{OES}	0	—	0	—	0	—	ns	
Output Enable Hold Time Read Toggle and $\overline{Data}$ Polling		t_{OEH}	0 10	— —	0 10	— —	0 10	— —	ns	1
Read Recover Time before Write		t_{GHEL}	0	—	0	—	0	—	ns	
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0		0		0		ns	
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	35	—	45	—	50	—	ns	
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	20	—	20	—	20	—	ns	
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	16	—	16	—	16	—	µs	
Erase Operation	t_{WHWH2}	t_{WHWH2}	1.5	30	1.5	30	1.5	30	s	2
V_{CC} Setup Time		t_{VCS}	50	—	50	—	50	—	µs	1

NOTES:
1. Not 100% tested.
2. This does not include the preprogramming time.

ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLE



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