FLASH MEMORY

CMOS

4M (512K × 8) BIT

MBM29F040A-90-X/-12-X
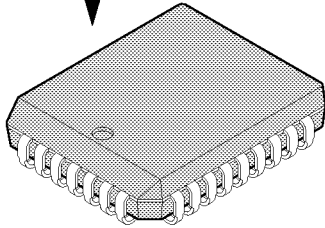
■ **FEATURES**

- **Single 5.0 V read, write, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  32-pin PLCC (Package suffix: PD)
  32-pin TSOP (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
- **Minimum 100,000 write/erase cycles**
- **High performance**
  90 ns maximum access time
- **Sector erase architecture**
  8 equal size sectors of 64 K bytes each
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low V$_{CC}$ write inhibit ≤3.2 V**
- **Sector protection**
  Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data in another sector within the same device
- **Extended operating temperature range: –40°C to +85°C**

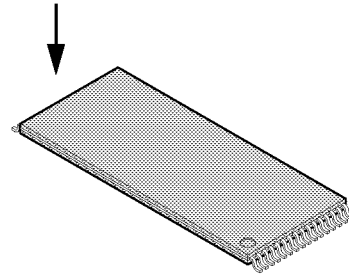> **Please refer to "MBM29F040A-70/-90/-12" in detailed specifications.**

Embedded Erase™, Embedded Program™ and ExpressFlash™ are trademarks of Advanced Micro Devices, Inc.
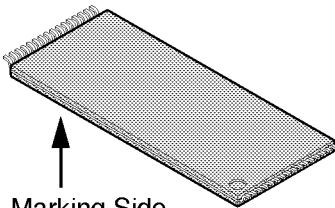
■ **PACKAGE**

Marking Side ↓

32-pin Plastic LCC
(LCC-32P-M02)

Marking Side ↓

32-pin Plastic TSOP
(FPT-32P-M24 — Assembly: Malaysia)

↑ Marking Side

32-pin Plastic TSOP
(FPT-32P-M25 — Assembly: Malaysia)

■ GENERAL DESCRIPTION

The MBM29F040A-X is a 4 M-bit, 5.0 V-only Flash memory organized as 512 K bytes of 8 bits each. The MBM29F040A-X is offered in a 32-pin PLCC and 32-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The industrial MBM29F040A-X offers access times of 90 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29F040A-X is pin and command set compatible with JEDEC standard 4 M-bit E^{2}PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F040A-X is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

A sector is typically erased and verified in 1.0 second (if already completely preprogrammed).

This device also features a sector erase architecture. The sector mode allows for 64 K byte sectors of memory to be erased and reprogrammed without affecting other sectors. The MBM29F040A-X is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^{2}PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The MBM29F040A-X memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

FLEXIBLE SECTOR-ERASE ARCHITECTURE

- 64 K byte per sector
- Individual-sector, multiple-sector, or bulk-erase capability
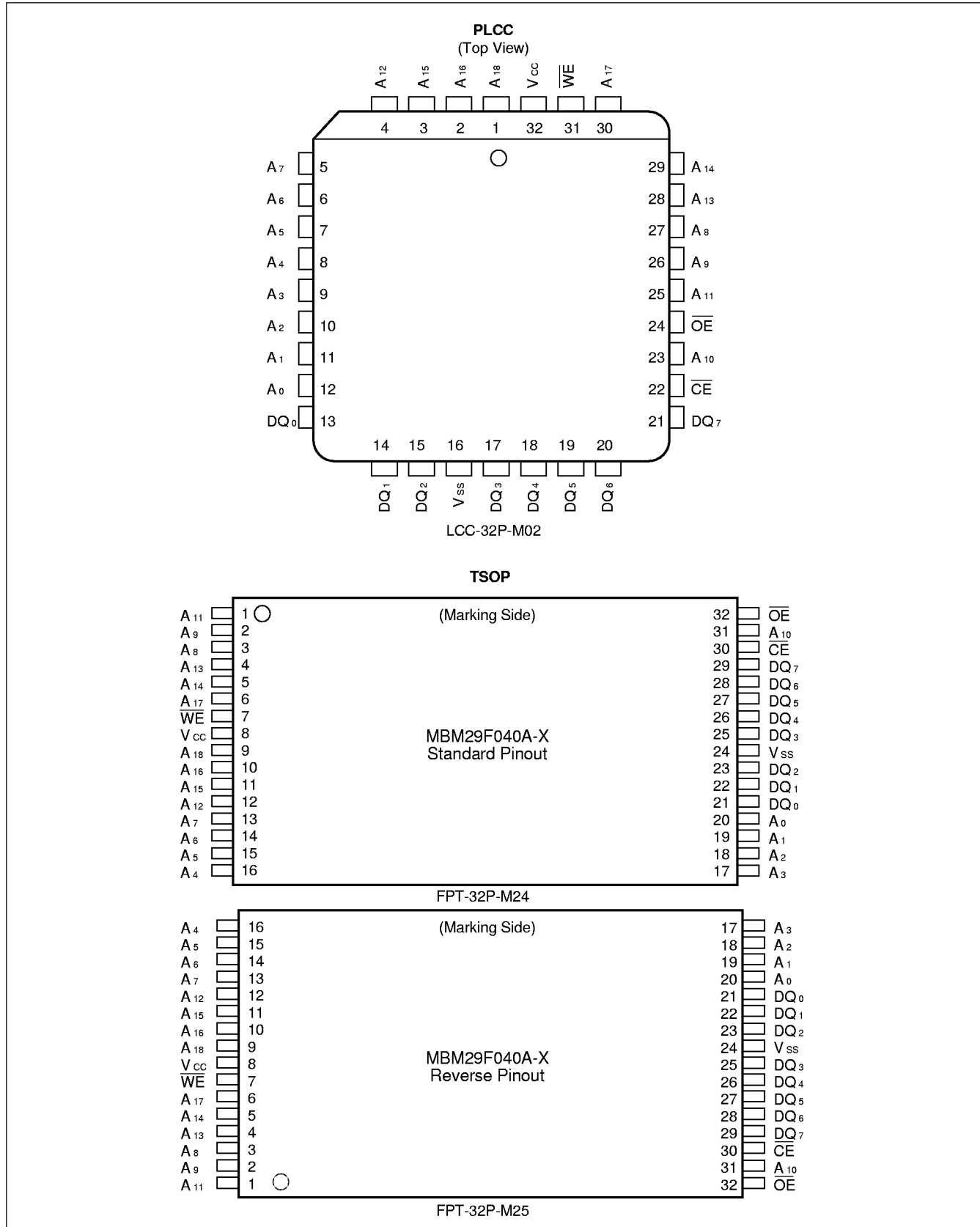- Individual or multiple-sector protection is user definable

	7FFFFH
	6FFFFH
	5FFFFH
64 K byte per sector	4FFFFH
	3FFFFH
	2FFFFH
	1FFFFH
	0FFFFH
	00000H
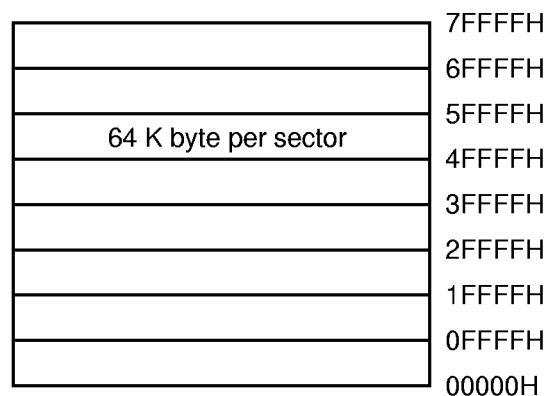
MBM29F040A-90-X/-12-X

■ **PRODUCT SELECTOR GUIDE**

Part No.	MBM29F040A	
Ordering Part No.	-90-X	-12-X
Max. Address Access Time (ns)	90	120
Max. $\overline{CE}$ Access Time (ns)	90	120
Max. $\overline{OE}$ Access Time (ns)	35	50

■ CONNECTION DIAGRAMS

PLCC
(Top View)

A12 A15 A16 A18 Vcc WE A17

	4	3	2	1	32	31	30	

A7 — 5   29 — A14
A6 — 6   28 — A13
A5 — 7   27 — A8
A4 — 8   26 — A9
A3 — 9   25 — A11
A2 — 10   24 — OE
A1 — 11   23 — A10
A0 — 12   22 — CE
DQ0 — 13   21 — DQ7

14 15 16 17 18 19 20

DQ1 DQ2 Vss DQ3 DQ4 DQ5 DQ6

LCC-32P-M02

TSOP

A11 — 1   (Marking Side)   32 — OE
A9 — 2   31 — A10
A8 — 3   30 — CE
A13 — 4   29 — DQ7
A14 — 5   28 — DQ6
A17 — 6   27 — DQ5
WE — 7   26 — DQ4
Vcc — 8   MBM29F040A-X   25 — DQ3
A18 — 9   Standard Pinout   24 — Vss
A16 — 10   23 — DQ2
A15 — 11   22 — DQ1
A12 — 12   21 — DQ0
A7 — 13   20 — A0
A6 — 14   19 — A1
A5 — 15   18 — A2
A4 — 16   17 — A3

FPT-32P-M24

A4 — 16   (Marking Side)   17 — A3
A5 — 15   18 — A2
A6 — 14   19 — A1
A7 — 13   20 — A0
A12 — 12   21 — DQ0
A15 — 11   22 — DQ1
A16 — 10   23 — DQ2
A18 — 9   24 — Vss
Vcc — 8   MBM29F040A-X   25 — DQ3
WE — 7   Reverse Pinout   26 — DQ4
A17 — 6   27 — DQ5
A14 — 5   28 — DQ6
A13 — 4   29 — DQ7
A8 — 3   30 — CE
A9 — 2   31 — A10
A11 — 1   32 — OE

FPT-32P-M25

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■ LOGIC SYMBOL

Table 1   MBM29F040A Pin Configuration

Pin	Function
A_0 to A_{18}	Address Inputs
DQ_0 to DQ_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ±10%)

■ ORDERING INFORMATION

Industrial Devices

Fujitsu industrial devices are available in several packages. The order number is formed by a combination of:

MBM29F040A   -90   PD   -X

OPERATING RANGE
Industrial Devices
Ambient Temperature (T_A): –40˚C to +85˚C

PACKAGE TYPE
PD   = 32-Pin Rectangular Plastic Leaded Chip
            Carrier (PLCC)
PFTN = 32-Pin Thin Small Outline Package
            (TSOP) Standard Pinout
PFTR = 32-Pin Thin Small Outline Package
            (TSOP) Reverse Pinout

SPEED OPTION
See Product Selector Guide

DEVICE NUMBER/DESCRIPTION
MBM29F040A
4 Mega-bit (512 K × 8-Bit) CMOS Flash Memory
5.0 V Read, Write, and Erase
64 K Byte Sectors (8 Sectors)

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■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....–55°C to +125°C

Ambient Temperature with Power Applied ....–40°C to +85°C

Voltage with Respect to Ground All pins except A_9, $\overline{OE}$ (Note 1) ....–2.0 V to +7.0 V

V_{CC} (Note 1) ....–2.0 V to +7.0 V

A_9, $\overline{OE}$ (Note 2) ....–2.0 V to +13.5 V

Notes: 1. Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.
2. Minimum DC input voltage on A_9, $\overline{OE}$ pins are –0.5 V. During voltage transitions, A_9, and $\overline{OE}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, and $\overline{OE}$ are +13.5 V which may overshoot to 14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Industrial Devices

Ambient Temperature (T_A) .... –40°C to +85°C

V_{CC} Supply Voltages .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.
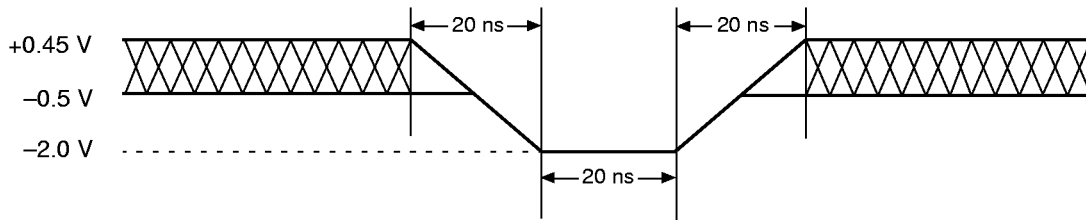
■ MAXIMUM OVERSHOOT
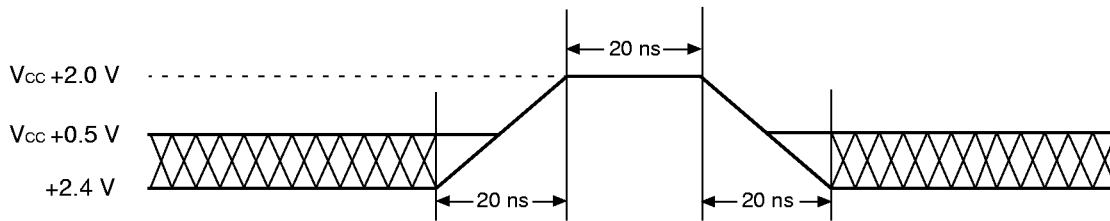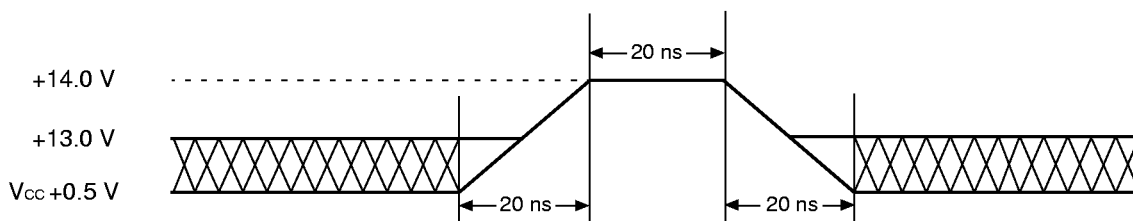

Figure 1   Maximum Negative Overshoot Waveform

Figure 2   Maximum Positive Overshoot Waveform

* : This waveform is applied for A_9 and $\overline{OE}$.

Figure 3   Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = Vss to Vcc, Vcc = Vcc Max.	—	±1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to Vcc, Vcc = Vcc Max.	—	±1.0	μA
I_{LIT}	A9, $\overline{OE}$ Inputs Leakage Current	Vcc = Vcc Max. A9, $\overline{OE}$ = 12.0 V	—	50	μA
I_{CC1}	Vcc Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	50	mA
I_{CC2}	Vcc Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	80	mA
I_{CC3}	Vcc Standby Current	Vcc = Vcc Max., $\overline{CE}$ = V_{IH}	—	1.5	mA
V_{IL}	Input Low Level	—	−0.5	0.45	V
V_{IH}	Input High Level	—	2.4	Vcc +0.5	V
V_{ID}	Voltage for Autoselect and Sector Protection (A9, $\overline{OE}$)	Vcc = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 12 mA, Vcc = Vcc Min.	—	0.45	V
V_{OH}	Output High Voltage Level	I_{OH} = −2.5 mA, Vcc = Vcc Min.	2.4	—	V
V_{LKO}	Low Vcc Lock-Out Voltage	—	3.2	4.2	V

Notes: 1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Icc active while Embedded Algorithm (program or erase) is in progress.

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1.0	μA
I_{LIT}	A_9, $\overline{OE}$ Inputs Leakage Current	$V_{CC} = V_{CC}$ Max. A_9, $\overline{OE} = 12.0$ V	—	50	μA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	50	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	80	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V	—	100	μA
V_{IL}	Input Low Level	—	−0.5	0.45	V
V_{IH}	Input High Level	—	$0.7 \times V_{CC}$	$V_{CC}+0.3$	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$)	$V_{CC} = 5.0$ V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	$I_{OL} = 12.0$ mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V
V_{OH1}	Output High Voltage Level	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min.	$0.85 \times V_{CC}$	—	V
V_{OH2}		$I_{OH} = -100$ μA, $V_{CC} = V_{CC}$ Min.	$V_{CC}-0.4$	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—	3.2	4.2	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz).
   The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

MBM29F040A-90-X/-12-X

■ AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols		Description	Test Set Up		-90-X (Note)	-12-X (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	ns

Note: Test Conditions: Output Load: 1 TTL gate and 100 pF
Input rise and fall times: 20 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 0.45 V and 2.4 V
Output: 0.8 V and 2.0 V
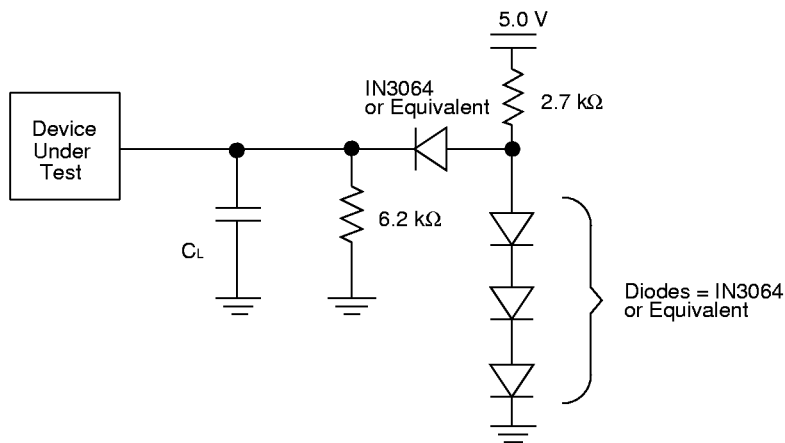
Note: C_L = 100 pF including jig capacitance

Figure 4 Test Conditions

- **Write/Erase/Program Operations**
  Alternate $\overline{\text{WE}}$ Controlled Writes

Parameter Symbols		Description		-90-X	-12-X	Unit
JEDEC	**Standard**					
t_{AVAV}	t_{WC}	Write Cycle Time	Min.	90	120	ns
t_{AVWL}	t_{AS}	Address Set Up Time	Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min.	45	50	ns
t_{DVWH}	t_{DS}	Data Set Up Time	Min.	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min.	0	0	ns
—	t_{OES}	Output Enable Set Up Time	Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time / Read	Min.	0	0	ns
		Toggle and $\overline{\text{Data}}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Set Up Time	Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time	Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min.	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min.	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ.	16	16	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ.	1.5	1.5	sec
			Max.	30	30	sec
—	t_{VCS}	Vcc Set Up Time	Min.	50	50	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)	Min.	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)	Min.	100	100	µs
—	t_{OESP}	$\overline{\text{OE}}$ Set Up Time to $\overline{\text{WE}}$ Active (Note 2)	Min.	4	4	µs
—	t_{CSP}	$\overline{\text{CE}}$ Set Up Time to $\overline{\text{WE}}$ Active (Note 2)	Min.	4	4	µs

Notes: 1. This does not include the preprogramming time.
       2. This timing is for Sector Protection operation.

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- **Write/Erase/Program Operations**
  Alternate CE Controlled Writes

Parameter Symbols		Description		-90-X	-12-X	Unit
JEDEC	Standard					
tAVAV	tWC	Write Cycle Time	Min.	90	120	ns
tAVEL	tAS	Address Set Up Time	Min.	0	0	ns
tELAX	tAH	Address Hold Time	Min.	45	50	ns
tDVEH	tDS	Data Set Up Time	Min.	45	50	ns
tEHDX	tDH	Data Hold Time	Min.	0	0	ns
—	tOES	Output Enable Set Up Time	Min.	0	0	ns
—	tOEH	Output Enable Hold Time — Read	Min.	0	0	ns
		Output Enable Hold Time — Toggle and Data Polling	Min.	10	10	ns
tGHEL	tGHEL	Read Recover Time Before Write	Min.	0	0	ns
tWLEL	tWS	WE Set Up Time	Min.	0	0	ns
tEHWH	tWH	WE Hold Time	Min.	0	0	ns
tELEH	tCP	CE Pulse Width	Min.	45	50	ns
tEHEL	tCPH	CE Pulse Width High	Min.	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation	Typ.	16	16	µs
tWHWH2	tWHWH2	Sector Erase Operation (Note)	Typ.	1.5	1.5	sec
			Max.	30	30	sec
—	tVCS	Vcc Set Up Time	Min.	50	50	µs

Note: This does not include the preprogramming time.

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■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1.5	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time	—	8	500	μs	Excludes system-level overhead
Chip Programming Time	—	8.5	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	7	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	10	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8.5	10	pF

Note: Test conditions $T_A = 25°C$, f = 1.0 MHz
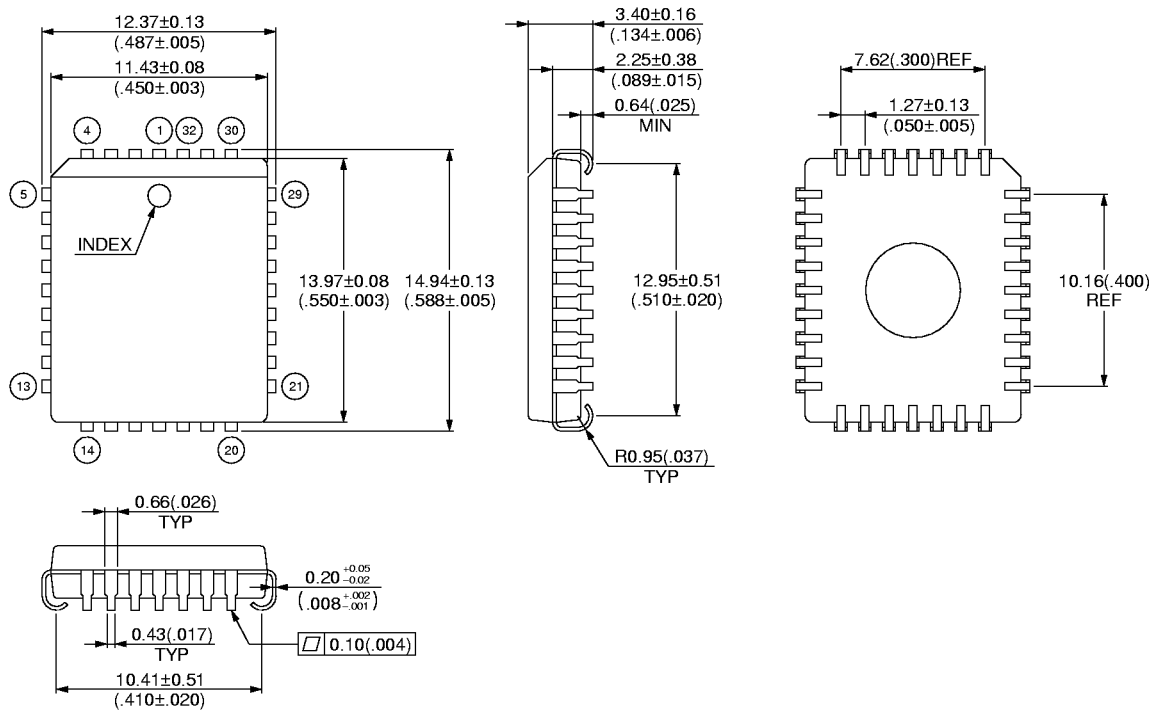
■ PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	7	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	10	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8.5	10	pF

Note: Test conditions $T_A = 25°C$, f = 1.0 MHz
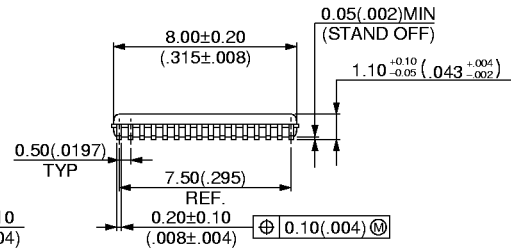
■ **PACKAGE DIMENSIONS**

32-Pin Plastic LCC
(LCC-32P-M02)

12.37±0.13
(.487±.005)

11.43±0.08
(.450±.003)

INDEX

13.97±0.08
(.550±.003)

14.94±0.13
(.588±.005)

3.40±0.16
(.134±.006)

2.25±0.38
(.089±.015)

0.64(.025)
MIN

12.95±0.51
(.510±.020)

R0.95(.037)
TYP

7.62(.300)REF

1.27±0.13
(.050±.005)

10.16(.400)
REF

0.66(.026)
TYP

0.20 +0.05 −0.02
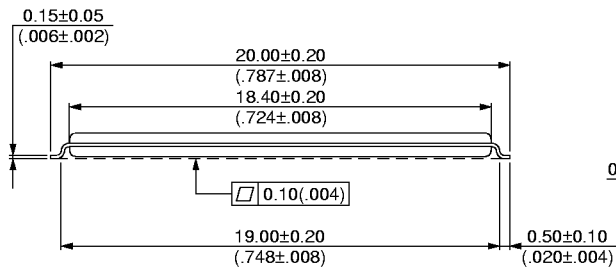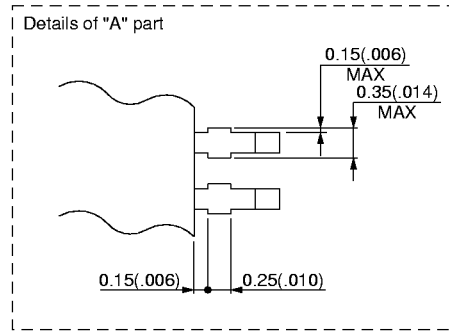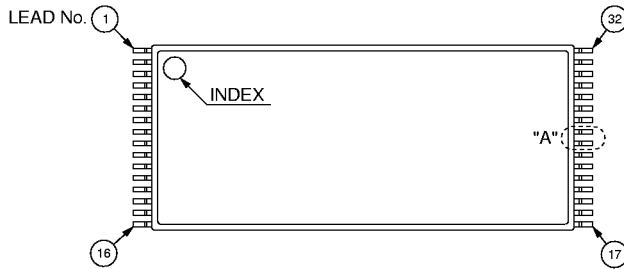(.008 +.002 −.001)

0.43(.017)
TYP

0.10(.004)

10.41±0.51
(.410±.020)

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Dimensions in mm(inches)

32-Pin Plastic TSOP
(FPT-32P-M24 — Assembly: Malaysia)

LEAD No. ①   ㉜

INDEX

"A"

⑯   ⑰

Details of "A" part

0.15(.006)
MAX
0.35(.014)
MAX

0.15(.006)   0.25(.010)

0.15±0.05
(.006±.002)

20.00±0.20
(.787±.008)
18.40±0.20
(.724±.008)

☐ 0.10(.004)

19.00±0.20
(.748±.008)

0.50±0.10
(.020±.004)

8.00±0.20
(.315±.008)

0.05(.002)MIN
(STAND OFF)

$1.10^{+0.10}_{-0.05}(.043^{+.004}_{-.002})$
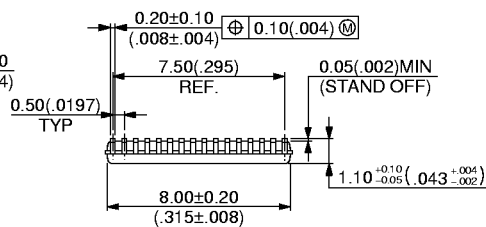
0.50(.0197)
TYP

7.50(.295)
REF.

0.20±0.10
(.008±.004)

⊕ 0.10(.004) Ⓜ
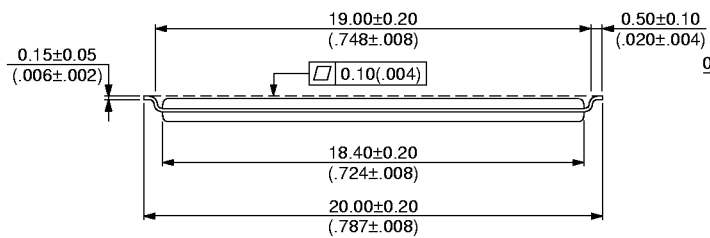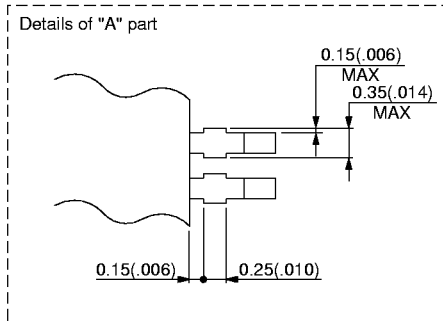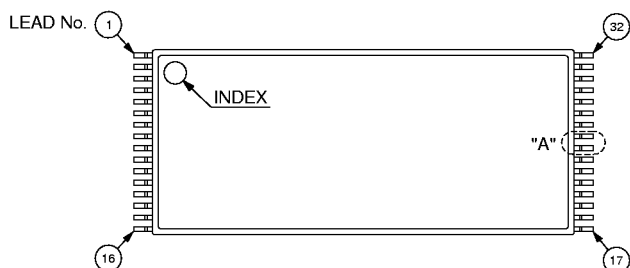
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Dimensions in mm(inches)

32-Pin Plastic TSOP
(FPT-32P-M25 — Assembly: Malaysia)

LEAD No. ①

INDEX

"A"

Details of "A" part

0.15(.006) MAX
0.35(.014) MAX
0.15(.006)   0.25(.010)

19.00±0.20
(.748±.008)

0.50±0.10
(.020±.004)

0.15±0.05
(.006±.002)

0.10(.004)

18.40±0.20
(.724±.008)

20.00±0.20
(.787±.008)

0.20±0.10
(.008±.004)
0.10(.004) Ⓜ

7.50(.295) REF.

0.05(.002)MIN
(STAND OFF)

0.50(.0197) TYP

8.00±0.20
(.315±.008)

1.10 +0.10/-0.05 (.043 +.004/-.002)

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Dimensions in mm(inches)