KM28C16/KM28C17 CMOS EEPROM

2K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **KM28C16/KM28C17: Commercial**
  - **KM28C16I/KM28C17I: Industrial**
- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Write Timing**
  - **Automatic Internal Erase-Before-Write**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C17)**
  - **$\overline{\text{Data}}$-Polling and Verification**
- **32-byte page Write 2ms**
  - **Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **100,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

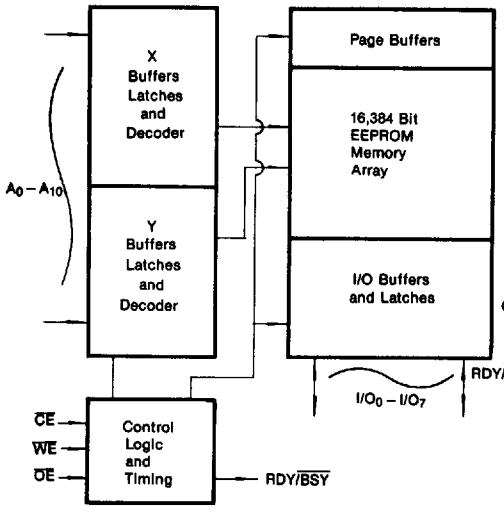
The KM28C16/C17 is a 2,048 x 8 bit Electrically Erasable Programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C16/C17 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 2ms write period. A 32-byte page write enables an entire chip written in 128ms.

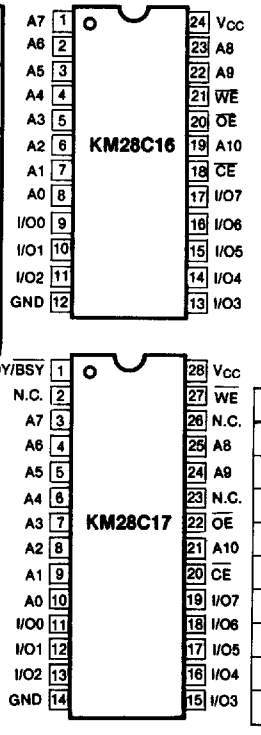
The KM28C16/C17 features $\overline{\text{Data}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM28C17 features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

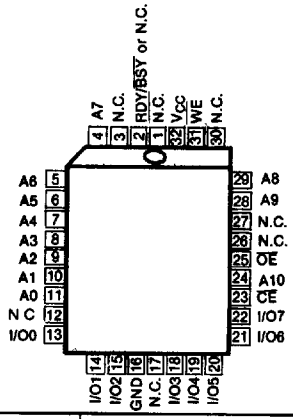
The KM28C16/C17 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION





Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	°C
Storage Temperature		T_{stg}	−65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

KM28C16/C17: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C16I/C17I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Input High Voltage, all Inputs	V_{IH}		2.0	$V_{CC} + 0.3$	V
Input Low Voltage, all Inputs	V_{IL}		−0.3	0.8	V
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.0	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C16/C17: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C16I/C17I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C16-15 KM28C16I-15 KM28C17-15 KM28C17I-15		KM28C16-20 KM28C16I-20 KM28C17-20 KM28C17I-20		KM28C16-25 KM28C16I-25 KM28C17-25 KM28C17I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		30		40		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns

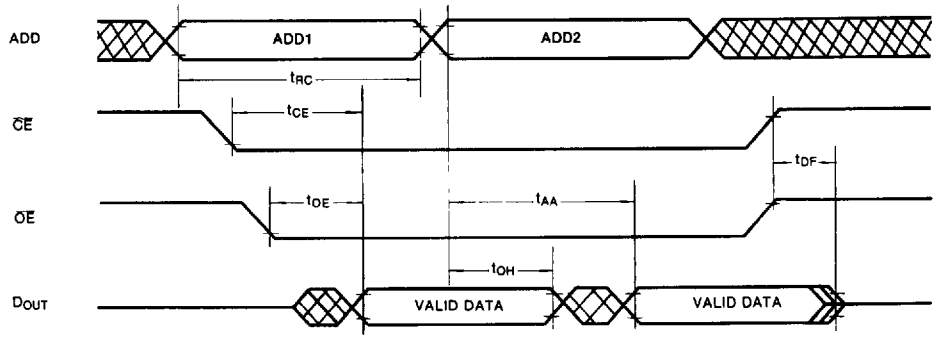
WRITE CYCLE

Parameter		Symbol	Min	Max	Unit
Write Cycle Time	Commercial	t_{WC}		2	ms
	Industrial			5	ms
Address Set-Up Time		t_{AS}	0		ns
Address Hold Time		t_{AH}	80		ns
Write Set-Up Time		t_{CS}	0		ns
Write Hold Time		t_{CH}	0		ns
$\overline{CE}$ Pulse Width		t_{CW}	100		ns
Output Enable Set-Up Time		t_{OES}	10		ns
Output Enable Hold Time		t_{OEH}	10		ns
$\overline{WE}$ Pulse Width		t_{WP}	100		ns
Data Set-Up Time		t_{DS}	50		ns
Data Hold Time		t_{DH}	10		ns
Time to Device Busy		t_{DB}		100	ns
Busy to Write Recovery Time		t_{BWR}	50		ns
Byte Load Cycle Time		t_{BLC}	0.2	100	μs
Last Byte Loaded to $\overline{Data}$ Polling		t_{LP}		200	ns

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and restarts at a rising edge of $\overline{WE}$.

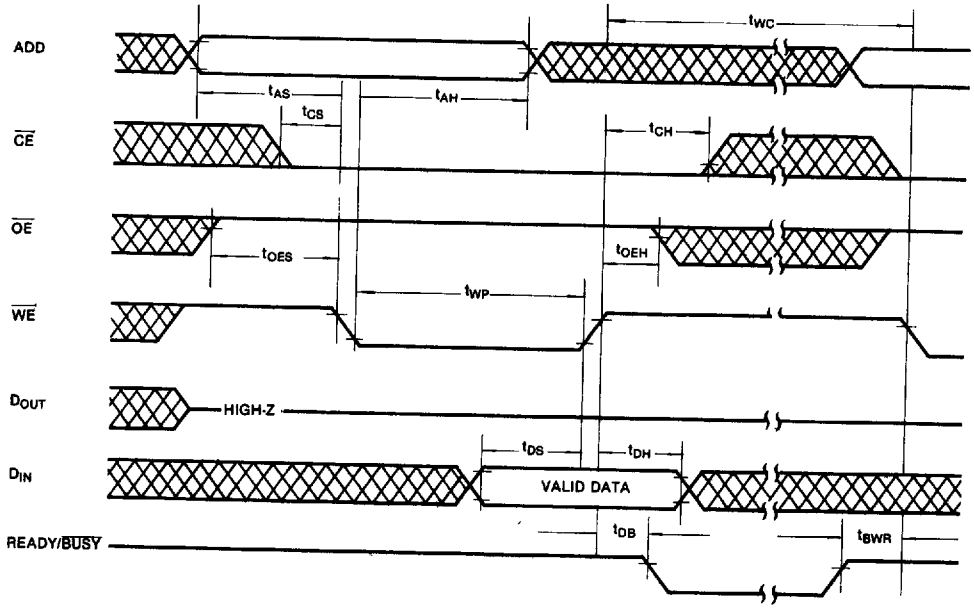
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

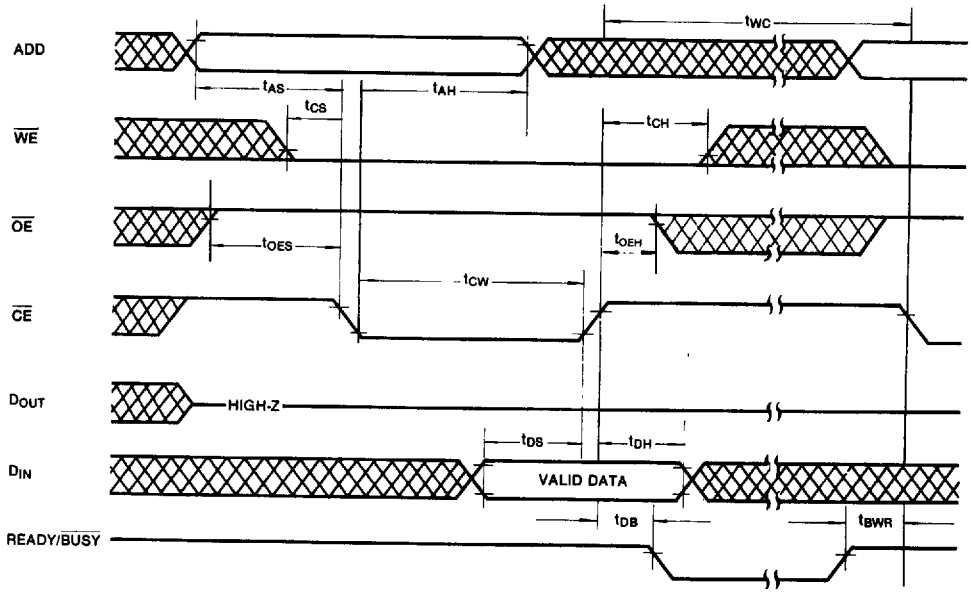


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

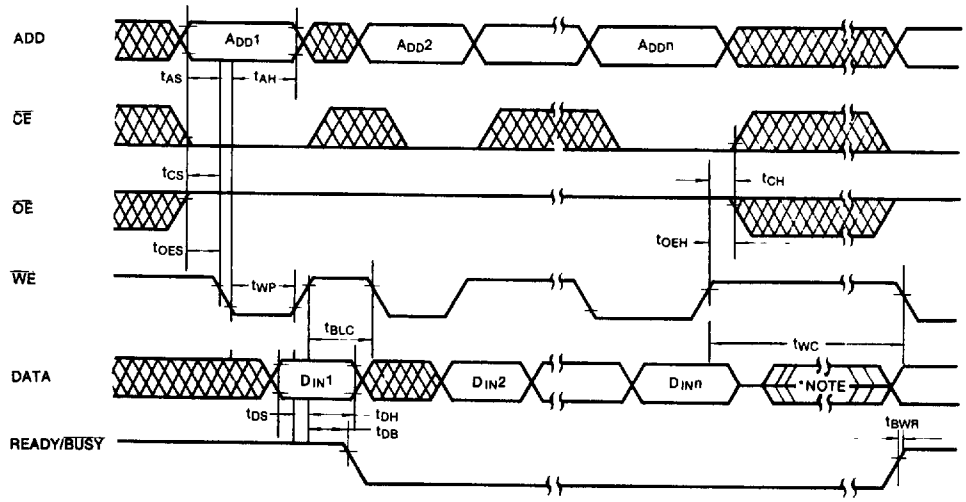


$\overline{CE}$ CONTROLLED WRITE

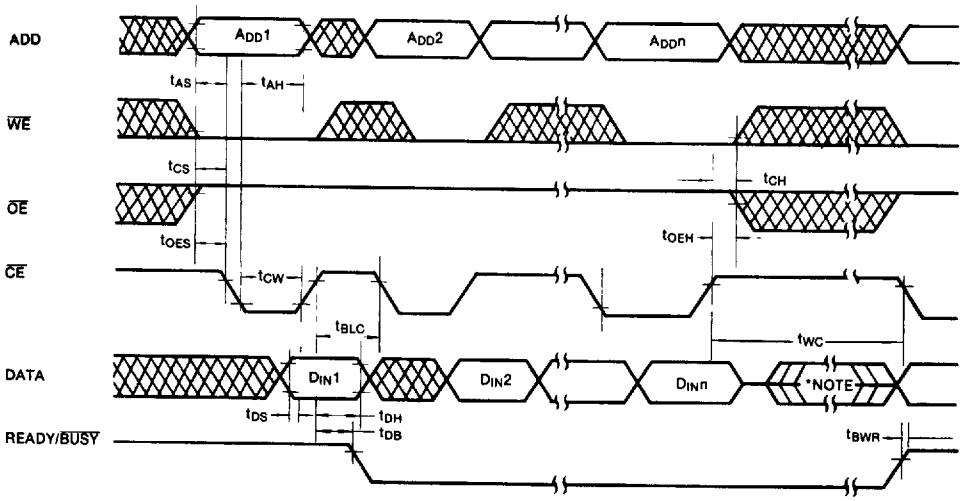


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1 I/O_7 Outputs $\overline{D_{INn}}$ when the chip is read
I/O_0-I/O_6 have high impedance

DEVICE OPERATION

READ

Reading data from the KM28C16/C17 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C16/C17 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write of the KM28C16/C17 is only a part of the page write. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM28C16/C17.

**** PAGE WRITE MODE ****

The KM28C16/C17 allows up to 32 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 bytes of data are loaded into the KM28C16/C17 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C16/C17 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. For each addressed location in the page, address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The data can be loaded in any "Y" address (A_0-A_4) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for loading the data (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue loading the data is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by the $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A_5-A_{10}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C16/C17 also supports a $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch the address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C16/C17 to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C16/C17 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise, the width shorter than 20ns (typ.) will not start any unwanted write cycle.

Write cycles are also inhibited when V_{CC} is less than V_{WI} = 3.0 volts, the write inhibits V_{CC} level.

During power-up, the KM28C16/C17 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The KM28C16C/C17 features Data polling at I/O_7 to detect the completion of a write cycle using a simple require any extemal hardware. During the write period, any data attempt to read of the last byte the EEPROM will produce, at I/O_7, an inverted value of the last I/O_7 data loaded in to the EEPROM (I/O_0-I/O_6 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION (Continued)

READY/BUSY

The KM28C17 has a Ready/Busy output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low. The Ready/Busy output is configured as an open-drain driver there-by allowing two or more Ready/Busy outputs to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + \Sigma I_L} = \frac{5.1V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready/Busy pin.

ENDURANCE AND DATA RETENTION

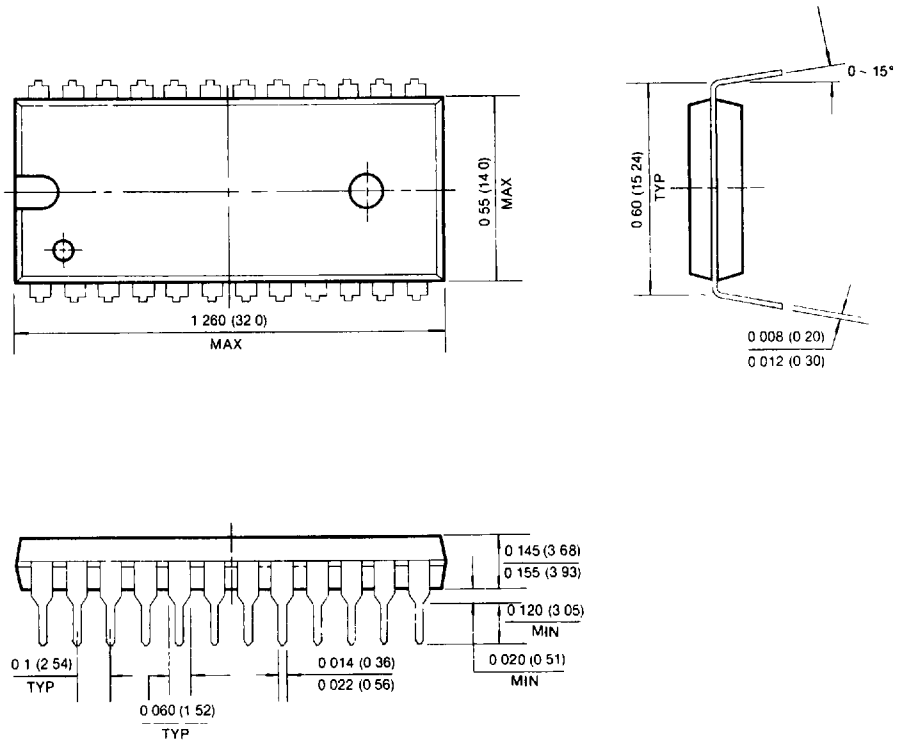
KM28C16/C17 is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation, and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

2

PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

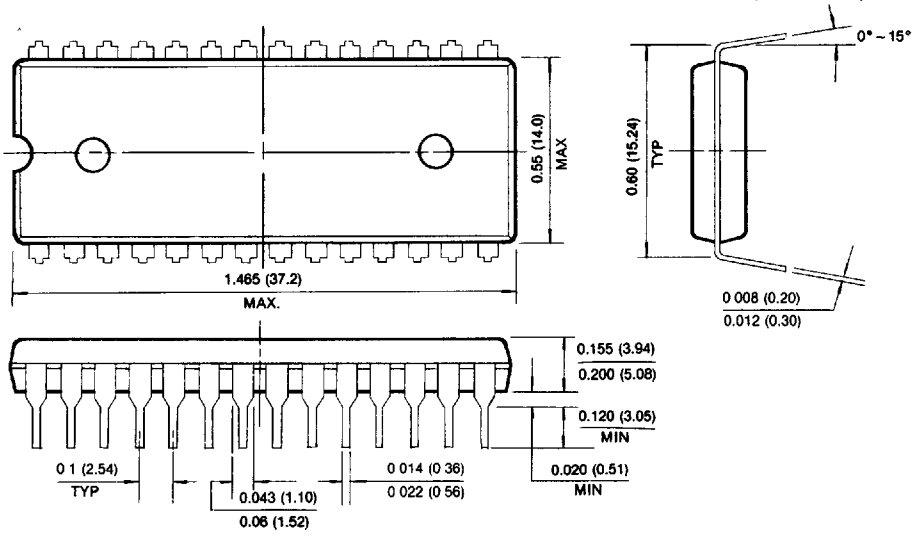
Units: Inches (millimeters)



PACKAGE DIMENSIONS (Continued)

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADED CHIP CARRIER