Features

- **Single Voltage Operation**
  - **5V Read**
  - **5V Reprogramming**
- **Fast Read Access Time - 55 ns**
- **Internal Program Control and Timer**
- **Sector Architecture**
  - **One 16K Byte Boot Block with Programming Lockout**
  - **Two 8K Byte Parameter Blocks**
  - **Two Main Memory Blocks (32K, 64K) Bytes**
- **Fast Erase Cycle Time - 10 seconds**
- **Byte By Byte Programming - 10 µs/Byte Typical**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Program Detection**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **100 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**

Description

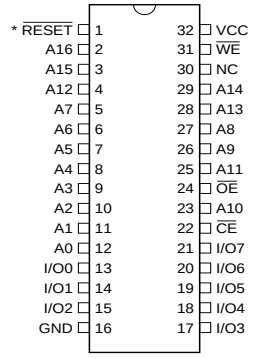
The AT49F001(N)(T) is a 5-volt-only in-system reprogrammable Flash Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 275 mW over the commercial temperature range.

(continued)

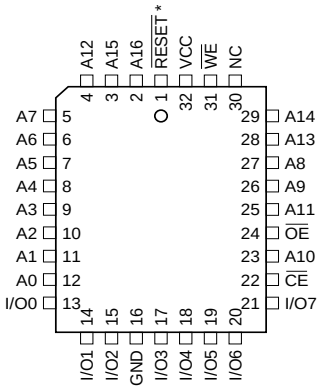
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	RESET
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

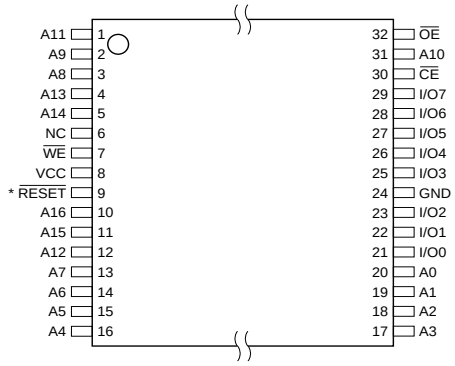
DIP Top View



PLCC Top View



VSOP Top View (8 x 14 mm) or
TSOP Top View (8 x 20 mm)
Type 1



*Note: This pin is a DC on the AT49F001N(T).

1-Megabit (128K x 8) 5-volt Only Flash Memory

AT49F001
AT49F001N
AT49F001T
AT49F001NT

Rev. 1008B–07/98

When the device is deselected, the CMOS standby current is less than 100 µA. For the AT49F001NT pin 1 for the DIP and PLCC packages and pin 9 for the TSOP package are don't connect pins.

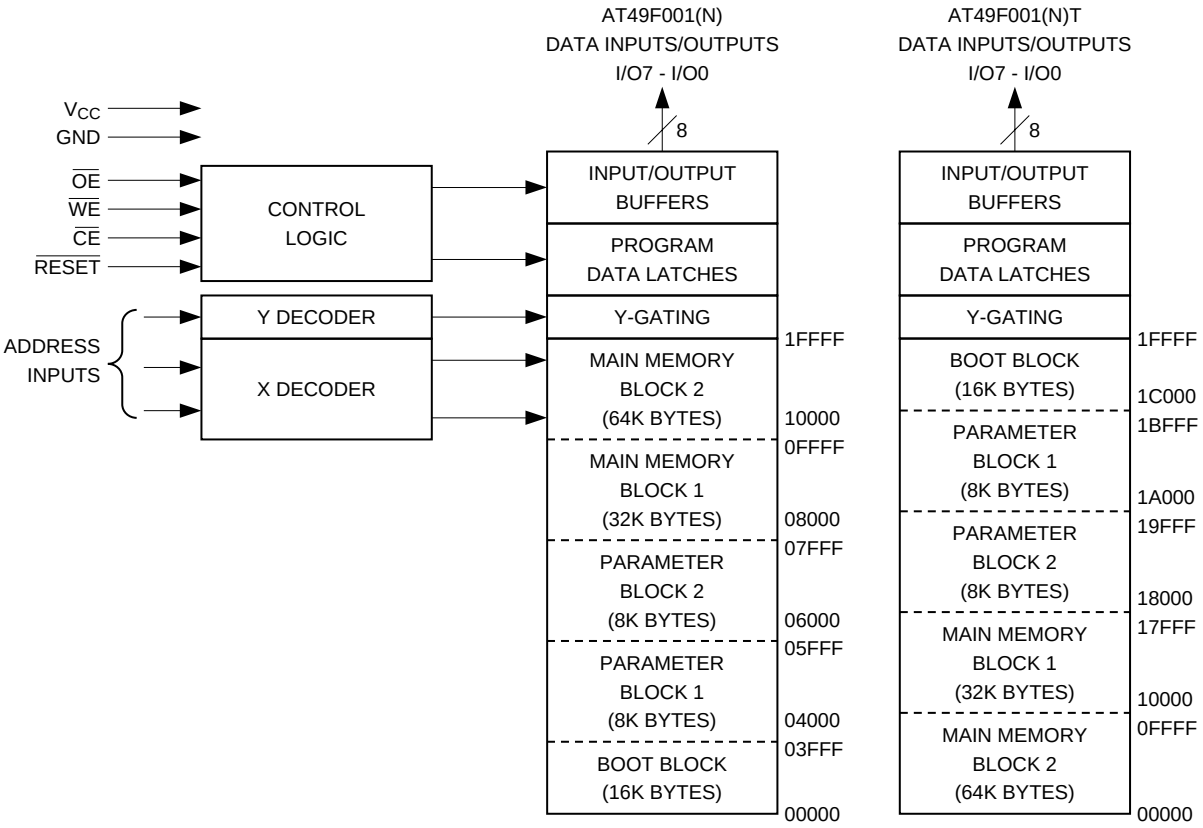
To allow for simple in-system reprogrammability, the AT49F001(N)(T) does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49F001(N)(T) is performed by erasing a block of data and then programming on a byte by byte basis. The byte programming time is a fast 50 µs. The end of a program cycle can be optionally detected by the $\overline{DATA}$ polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The device is erased by executing the erase command sequence; the device internally controls the erase operations. There are two 8K byte parameter block sections and two main memory blocks.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. The 16K-byte boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

In the AT49F001N(T), once the boot block programming lockout feature is enabled, the contents of the boot block are permanent and cannot be changed. In the AT49F001(T), once the boot block programming lockout feature is enabled, the contents of the boot block cannot be changed with input voltage levels of 5.5 volts or less.

Block Diagram



Device Operation

READ: The AT49F001(N)(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table. The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedence state. If the $\overline{RESET}$ pin makes a high to low transition during a program or erase operation, the operation may not be sucessfully completed and the operation will have to be repeated after a high level is applied to the $\overline{RESET}$ pin. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs. By applying a 12V $\pm$ 0.5V input signal to the $\overline{RESET}$ pin, the boot block array can be reprogrammed even if the boot block lockout feature has been enabled (see Boot Block Programming Lockout Override section). The RESET feature is not available for the AT49F001N(T).

ERASURE: Before a byte can be reprogrammed, the main memory block or parameter block which contains the byte must be erased. The erased state of the memory bits is a logical “1”. The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}. If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function will erase Parameter Block 1, Parameter Block 2, Main Memory Block 1, and Main Memory Block 2 but not the boot block. If the Boot Block Lockout has not been enabled, the Chip Erase function will erase the entire chip. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into sectors that can be individually erased. There are two 8K-byte parameter block sections and two main memory blocks. The 8K-byte parameter block sections can be independently erased and reprogrammed. The two main memory sections are designed to be used as alternative memory sectors. That is, whenever one of the blocks has been erased and reprogrammed, the other block should be erased and reprogrammed before the first block is again erased. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

BYTE PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical “0”) on a byte-by-byte basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 16K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block’s usage as a write protected region is optional to the user. The address range of the boot block is 00000 to 03FFF for the AT49F001(N) while the address

range of the boot block is 1C000 to 1FFFF for the AT49F001(N)T.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed with input voltage levels of 5.5V or less. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out for the AT49F001(N) and a read from address 1C002H will show if programming the boot block is locked out for the AT49F001(N)T. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{\text{RESET}}$ pin to 12 volts. By doing this, protected boot block data can be altered through a chip erase, sector erase or word programming. When the $\overline{\text{RESET}}$ pin is brought back to TTL levels the boot block programming lockout feature is again active. This feature is not available on the AT49F001N(T).

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F001(N)(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F001(N)(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F001(N)(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

Command Definition (in Hex)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[4]	30
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout[2]	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[3]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[3]	1	XXXX	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O7 - I/O0 (Hex)
2. The 16K byte boot sector has the address range 00000H to 03FFFH for the AT49F001(N) and 1C000H to 1FFFFH for the AT49F001(N)T.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses
   For the AT49F001(N):
   SA = 10000 to 1FFFF for BOOT BLOCK
   Nothing will happen and the device goes back to the read mode in 100 ns
   SA = 04000 to 05FFF for PARAMETER BLOCK 1
   SA = 06000 to 07FFF for PARAMETER BLOCK 2
   SA = 08000 to 0FFFF for MAIN MEMORY ARRAY BLOCK 1
   This command will erase - PB1, PB2 and MMB1
   SA = 10000 to 1FFFF for MAIN MEMORY ARRAY BLOCK 2

   For the AT49F001(N)T:
   SA = 1C000 to 1FFFF for BOOT BLOCK
   Nothing will happen and the device goes back to the read mode in 100 ns
   SA = 1A000 to 1BFFF for PARAMETER BLOCK 1
   SA = 18000 to 19FFF for PARAMETER BLOCK 2
   SA = 10000 to 17FFF for MAIN MEMORY ARRAY BLOCK 1
   This command will erase - PB1, PB2 and MMB1
   SA = 00000 to 0FFFF for MAIN MEMORY ARRAY BLOCK 2

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F001(N)(T)-55	AT49F001(N)(T)-70	AT49F001(N)(T)-90	AT49F001(N)(T)-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$[6]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}		A1 - A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
					A1 - A16 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]
Software[5]					A0 = V_{IL}, A1 - A16=V_{IL}	Manufacturer Code[4]
					A0 = V_{IH}, A1 - A16=V_{IL}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 05H - AT49F001(N), 04H - AT49F001(N)T
5. See details under Software Product Identification Entry/Exit.
6. This pin is not available on the AT49F001N(T).

DC Characteristics

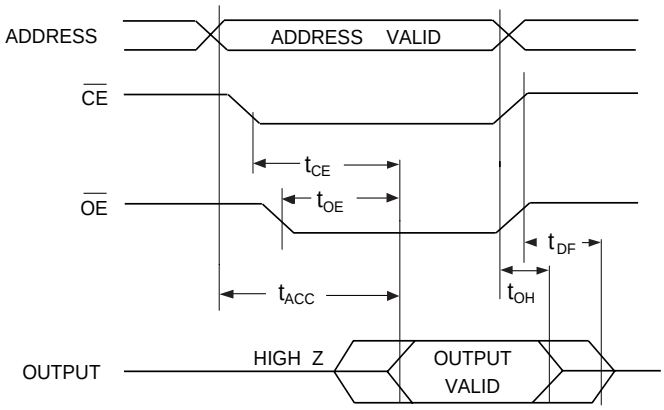
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		100	µA
			Ind.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			3	mA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V		4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

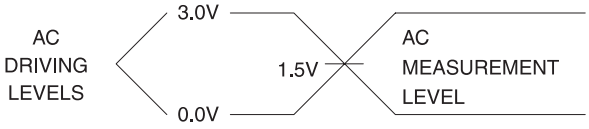
Symbol	Parameter	AT49F001(N)(T)-50		AT49F001(N)(T)-70		AT49F001(N)(T)-90		AT49F001(N)(T)-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		50		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		50		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1)(2)(3)(4)



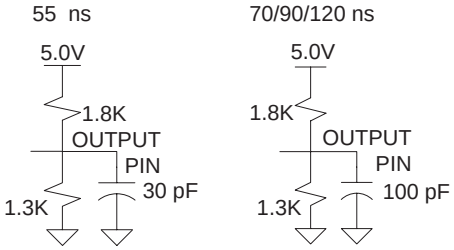
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveform and Measurement Level



t_R, t_F < 5 ns

Output Load Test



Pin Capacitance

(f = 1 MHz, T = 25°C)[1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

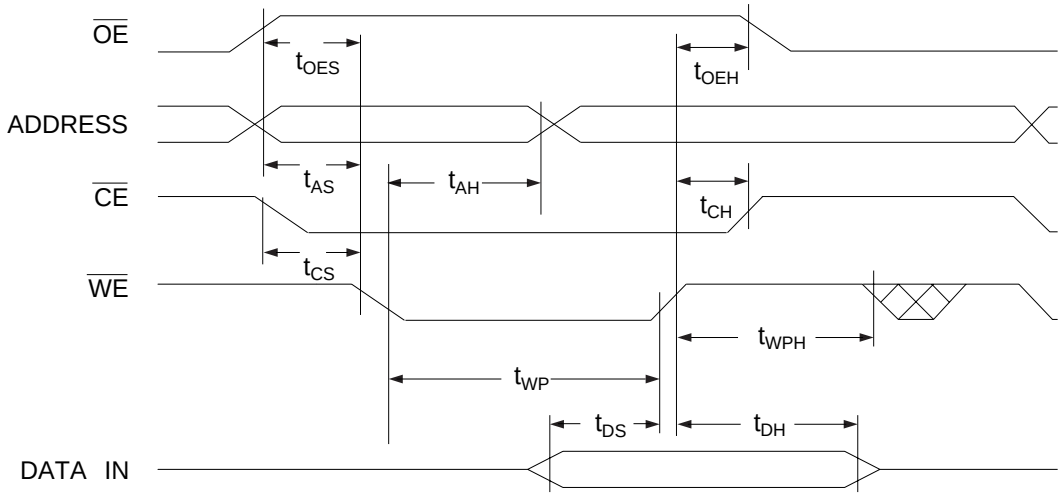
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

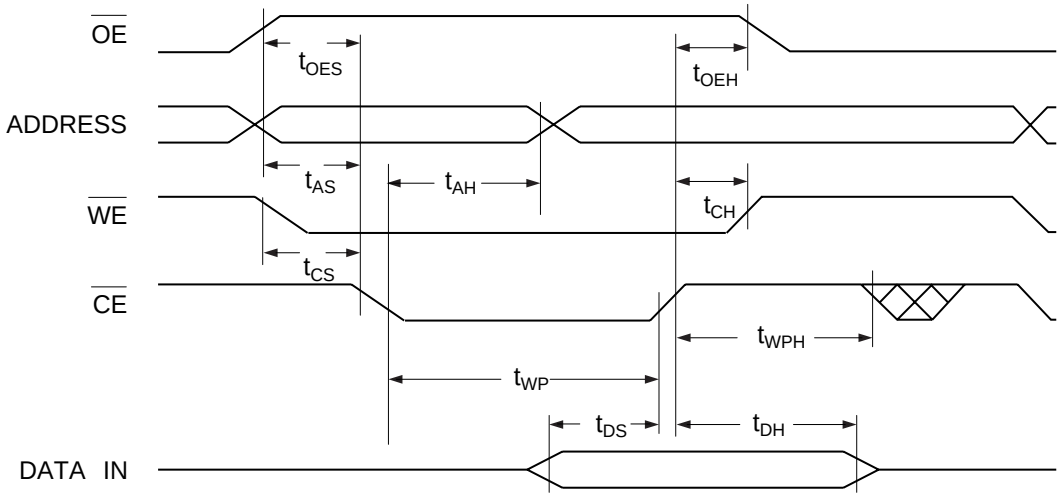
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



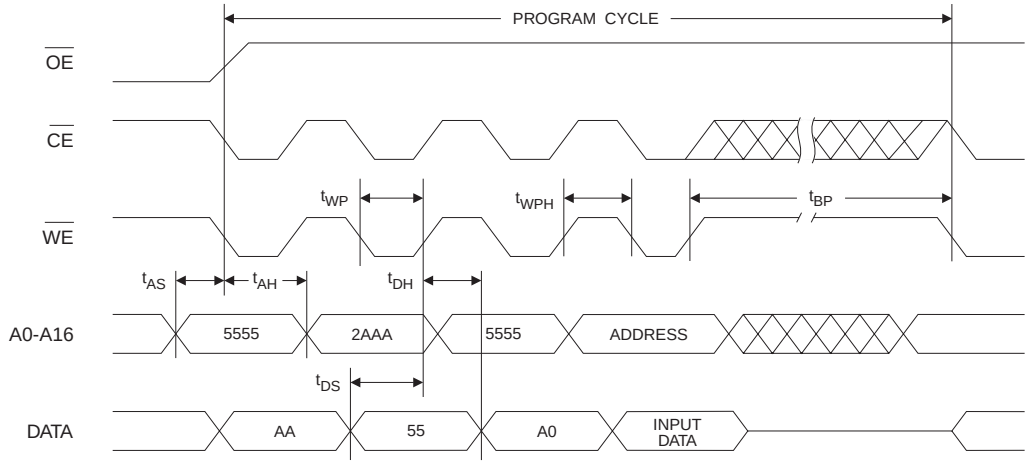
$\overline{CE}$ Controlled



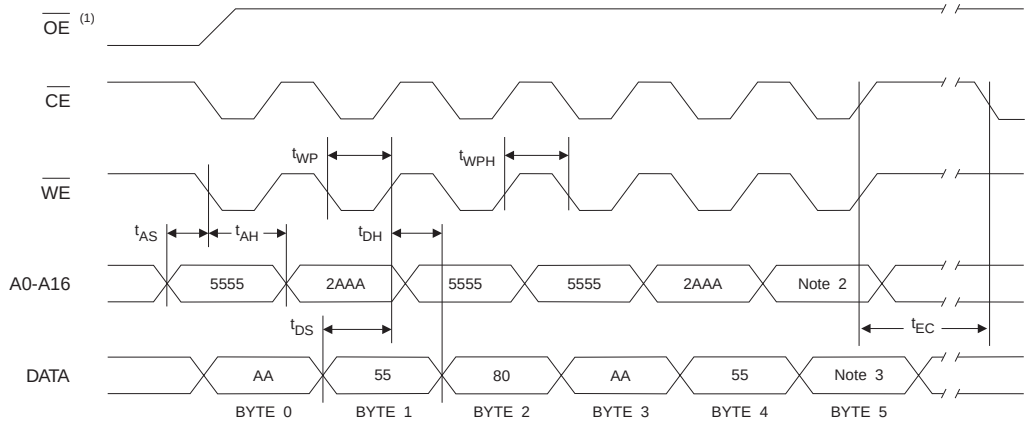
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte Programming Time		10	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	90			ns
t_{WPH}	Write Pulse Width High	90			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)

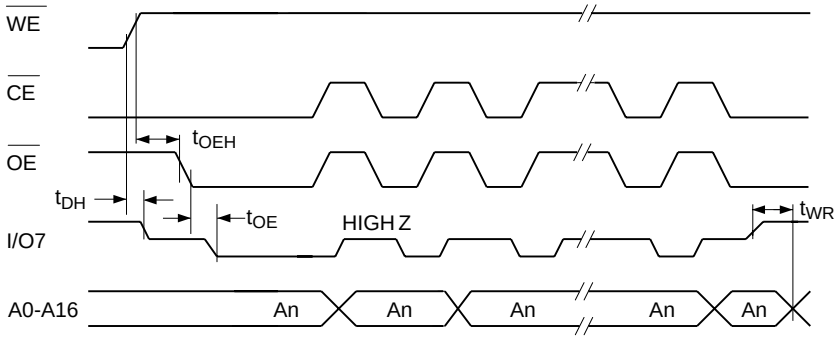
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

Data Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{DATA}$ Polling Waveforms

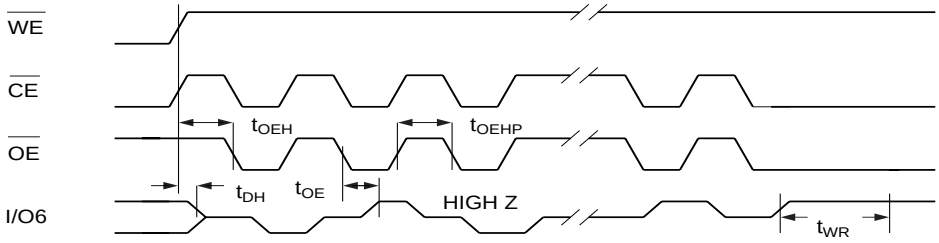


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

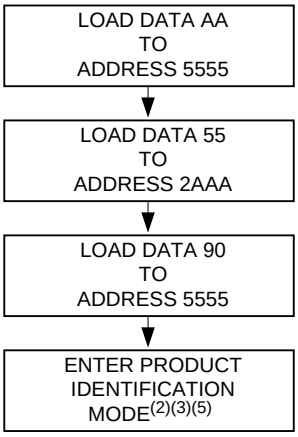
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)

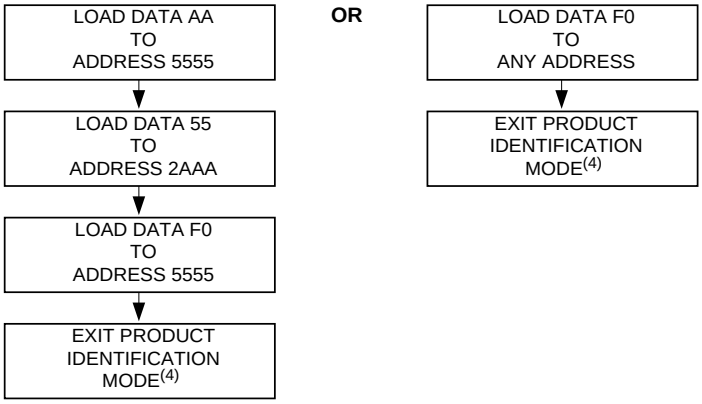


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]



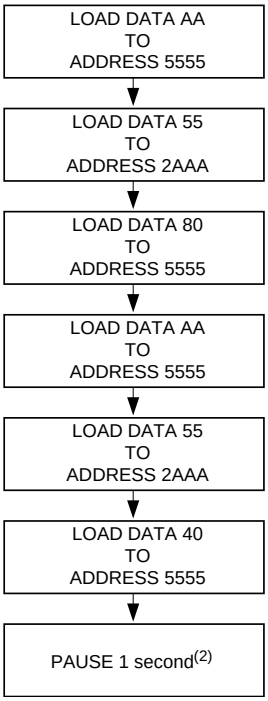
Software Product Identification Exit[1]



Notes for software product identification

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A16 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 05H - AT49F001(N)
   04H - AT49F001(N)T

Boot Block Lockout Feature Enable Algorithm[1]



Notes for boot block lockout feature enable:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

AT49F001 Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	0.1	AT49F001-55JC AT49F001-55PC AT49F001-55TC AT49F001-55VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001-55JI AT49F001-55PI AT49F001-55TI AT49F001-55VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
70	50	0.1	AT49F001-70JC AT49F001-70PC AT49F001-70TC AT49F001-70VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001-70JI AT49F001-70PI AT49F001-70TI AT49F001-70VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
90	50	0.1	AT49F001-90JC AT49F001-90PC AT49F001-90TC AT49F001-90VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001-90JI AT49F001-90PI AT49F001-90TI AT49F001-90VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
120	50	0.1	AT49F001-12JC AT49F001-12PC AT49F001-12TC AT49F001-12VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001-12JI AT49F001-12PI AT49F001-12TI AT49F001-12VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)

Package Type	
32J	32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
32V	32-Lead, Plastic Thin Small Outline Package (TSOP) (8 x 14 mm)

AT49F001N Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	0.1	AT49F001N-55JC AT49F001N-55PC AT49F001N-55TC AT49F001N-55VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001N-55JI AT49F001N-55PI AT49F001N-55TI AT49F001N-55VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
70	50	0.1	AT49F001N-70JC AT49F001N-70PC AT49F001N-70TC AT49F001N-70VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001N-70JI AT49F001N-70PI AT49F001N-70TI AT49F001N-70VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
90	50	0.1	AT49F001N-90JC AT49F001N-90PC AT49F001N-90TC AT49F001N-90VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001N-90JI AT49F001N-90PI AT49F001N-90TI AT49F001N-90VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
120	50	0.1	AT49F001N-12JC AT49F001N-12PC AT49F001N-12TC AT49F001N-12VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001N-12JI AT49F001N-12PI AT49F001N-12TI AT49F001N-12VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)

Package Type	
32J	32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
32V	32-Lead, Plastic Thin Small Outline Package (TSOP) (8 x 14 mm)

AT49F001T Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	0.1	AT49F001T-55JC AT49F001T-55PC AT49F001T-55TC AT49F001T-55VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001T-55JI AT49F001T-55PI AT49F001T-55TI AT49F001T-55VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
70	50	0.1	AT49F001T-70JC AT49F001T-70PC AT49F001T-70TC AT49F001T-70VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001T-70JI AT49F001T-70PI AT49F001T-70TI AT49F001T-70VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
90	50	0.1	AT49F001T-90JC AT49F001T-90PC AT49F001T-90TC AT49F001T-90VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001T-90JI AT49F001T-90PI AT49F001T-90TI AT49F001T-90VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
120	50	0.1	AT49F001T-12JC AT49F001T-12PC AT49F001T-12TC AT49F001T-12VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001T-12JI AT49F001T-12PI AT49F001T-12TI AT49F001T-12VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)

Package Type	
32J	32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
32V	32-Lead, Plastic Thin Small Outline Package (TSOP) (8 x 14 mm)

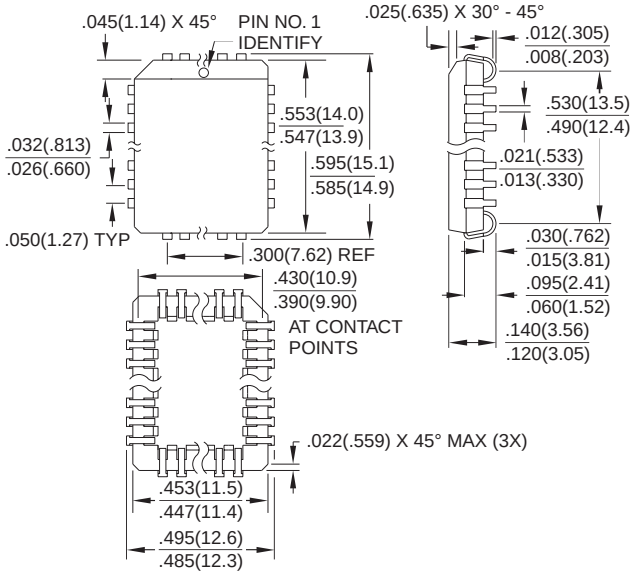
AT49F001NT Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
55	50	0.1	AT49F001NT-55JC AT49F001NT-55PC AT49F001NT-55TC AT49F001NT-55VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001NT-55JI AT49F001NT-55PI AT49F001NT-55TI AT49F001NT-55VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
70	50	0.1	AT49F001NT-70JC AT49F001NT-70PC AT49F001NT-70TC AT49F001NT-70VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001NT-70JI AT49F001NT-70PI AT49F001NT-70TI AT49F001NT-70VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
90	50	0.1	AT49F001NT-90JC AT49F001NT-90PC AT49F001NT-90TC AT49F001NT-90VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001NT-90JI AT49F001NT-90PI AT49F001NT-90TI AT49F001NT-90VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)
120	50	0.1	AT49F001NT-12JC AT49F001NT-12PC AT49F001NT-12TC AT49F001NT-12VC	32J 32P6 32T 32V	Commercial (0° to 70°C)
	50	0.3	AT49F001NT-12JI AT49F001NT-12PI AT49F001NT-12TI AT49F001NT-12VI	32J 32P6 32T 32V	Industrial (-40° to 85°C)

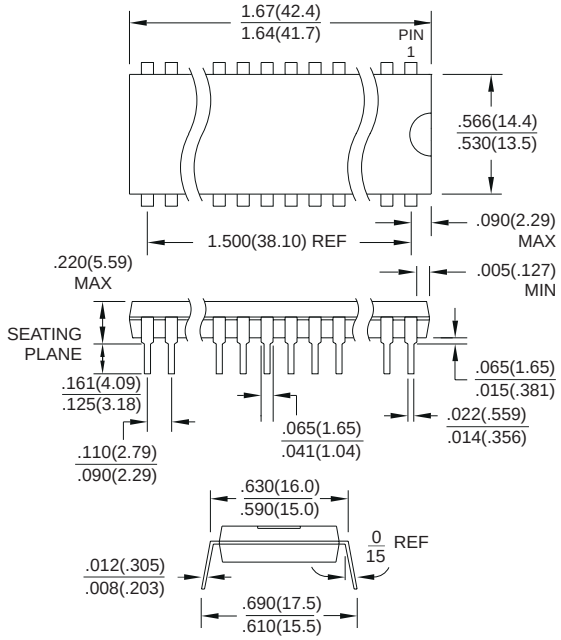
Package Type	
32J	32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual In-line Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
32V	32-Lead, Plastic Thin Small Outline Package (TSOP) (8 x 14 mm)

Packaging Information

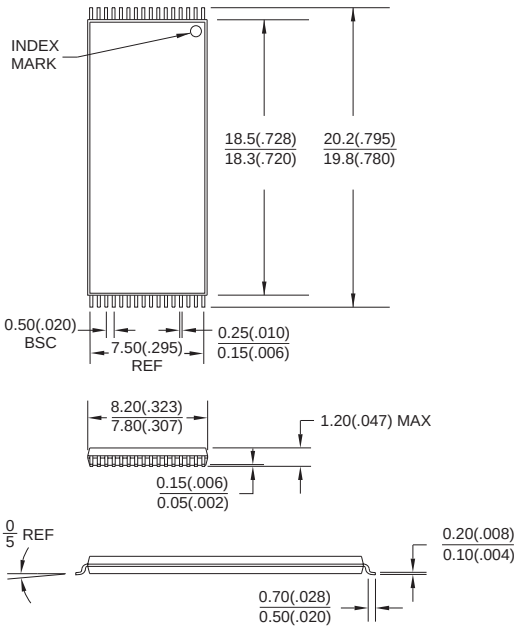
32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



32P6, 32-Lead, 0.600" Wide,
Plastic Dual In-line Package (PDIP)
Dimensions in Inches and (Millimeters)

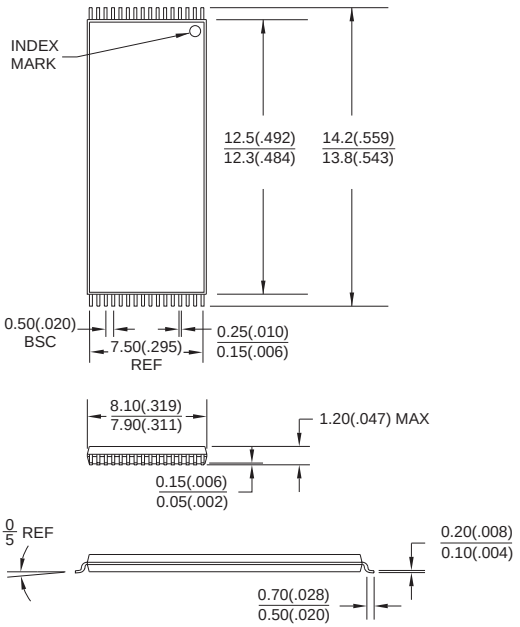


32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

32V, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 BA



*Controlling dimension: millimeters