FM24C16A

16Kb FRAM Serial Memory

Features

16K bit Ferroelectric Nonvolatile RAM

- Organized as 2,048 x 8 bits
- High Endurance (10^{12}) Read/Write Cycles
- 45 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Fast Two-wire Serial Interface

- Up to 1MHz maximum bus frequency
- Direct hardware replacement for EEPROM

Low Power Operation

- 5V operation
- 150 µA Active Current (100 kHz)
- 10 µA Standby Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 8-pin SOIC (-S)
- "Green" 8-pin SOIC (-G)

Description

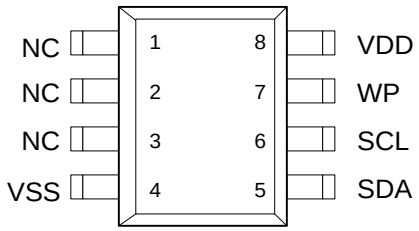
The FM24C16A is a 16-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for over 45 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike serial EEPROMs, the FM24C16A performs write operations at bus speed. No write delays are incurred. The next bus cycle may commence immediately without the need for data polling. The FM24C16A is capable of supporting 10^{12} read/write cycles, or a million times more write cycles than EEPROM.

These capabilities make the FM24C16A ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows the system to write data more frequently, with less system overhead.

The FM24C16A provides substantial benefits to users of serial EEPROM, and these benefits are available as a hardware drop-in replacement. The FM24C16A is available in an industry standard 8-pin SOIC and uses a two-wire protocol. The specifications are guaranteed over the industrial temperature range from -40°C to +85°C.

Pin Configuration



Pin Names	Function
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
VDD	Supply Voltage 5V
VSS	Ground

Ordering Information	
FM24C16A-S	8-pin SOIC
FM24C16A-G	"Green" 8-pin SOIC

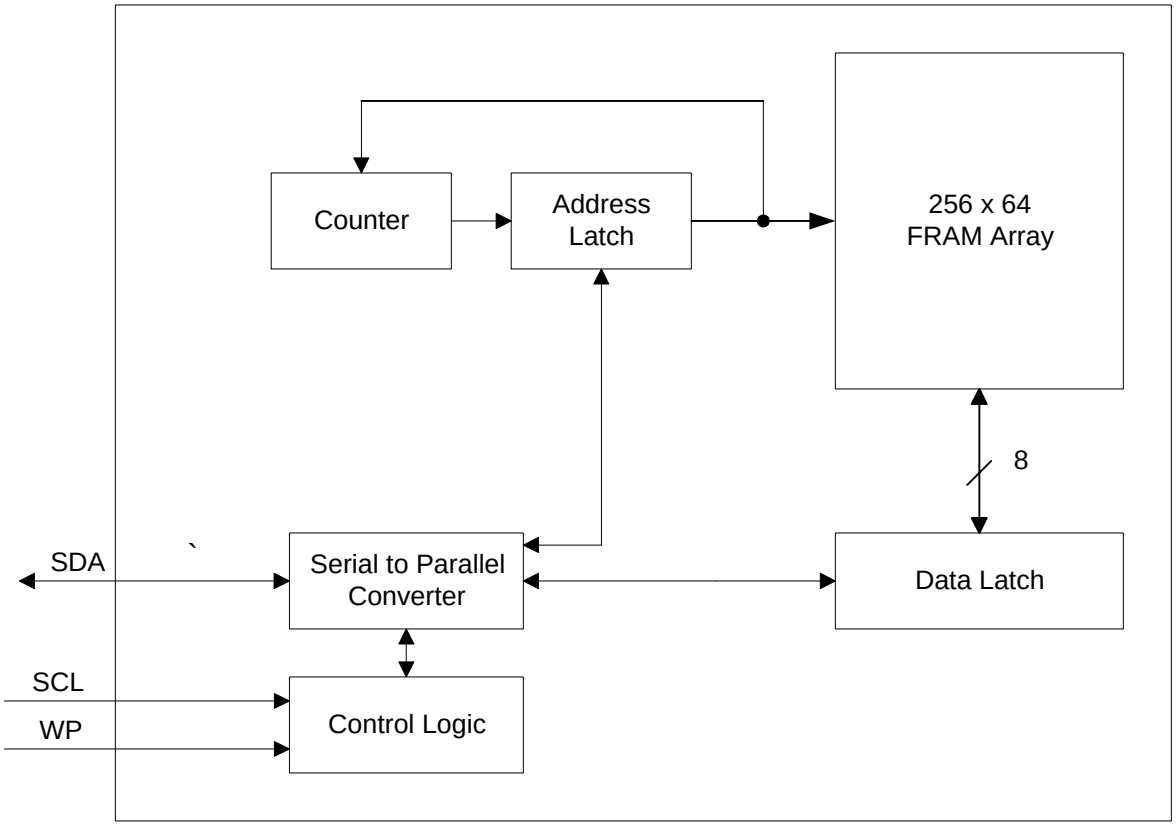


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
SDA	I/O	Serial Data Address: This is a bi-directional data pin for the two-wire interface. It employs an open-drain output and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. A pull-up resistor is required.
SCL	Input	Serial Clock: The serial clock input for the two-wire interface. Data is clocked-out on the falling edge and clocked-in on the rising edge.
WP	Input	Write Protect: When WP is high, the entire array is write-protected. When WP is low, all addresses may be written. This pin is internally pulled down.
VDD	Supply	Supply Voltage (5V)
VSS	Supply	Ground
NC	-	No connect

Overview

The FM24C16A is a serial FRAM memory. The memory array is logically organized as a 2,048 x 8 memory array and is accessed using an industry standard two-wire interface. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM24C16A and a serial EEPROM with the same pinout relates to its superior write performance.

Memory Architecture

When accessing the FM24C16A, the user addresses 2,048 locations each with 8 data bits. These data bits are shifted serially. The 2,048 addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish from other non-memory devices), a row address, and a segment address. The row address consists of 8-bits that specify one of 256 rows. The 3-bit segment address specifies one of 8 segments within each row. The complete 11-bit address specifies each byte uniquely.

Most functions of the FM24C16A either are controlled by the two-wire interface or handled automatically by on-board circuitry. The memory is read or written at the speed of the two-wire bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation is complete. This is explained in more detail in the interface section below.

Note that the FM24C16A contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Two-wire Interface

The FM24C16A employs a bi-directional two-wire bus protocol using few pins and little board space. Figure 2 illustrates a typical system configuration using the FM24C16A in a microcontroller-based system. The industry standard two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24C16A is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including Start, Stop, Data bit, and Acknowledge. Figure 3 illustrates the signal conditions that define the four states. Detailed timing diagrams are shown in the Electrical Specifications section.

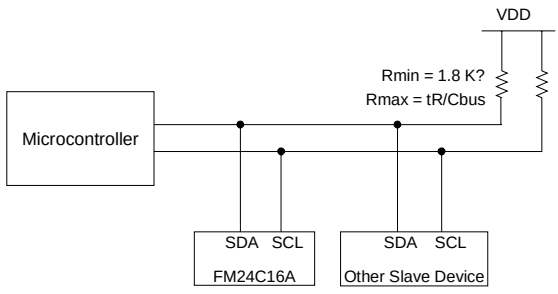


Figure 2. Typical System Configuration

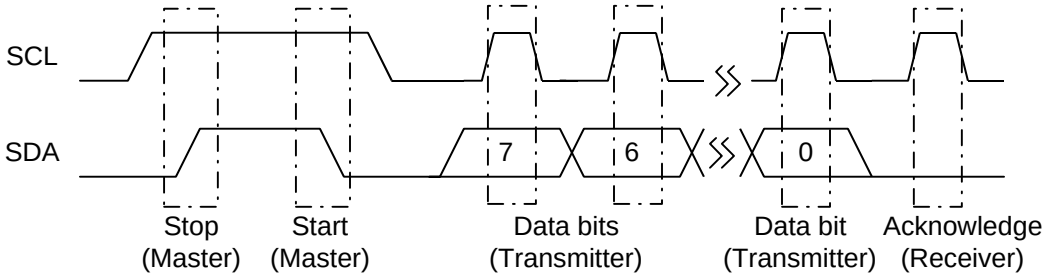


Figure 3. Data Transfer Protocol

Stop Condition

A stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations using the FM24C16A must end with a Stop condition. If an operation is pending when a Stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a Stop condition.

Start Condition

A Start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All read and write transactions begin with a Start condition. An operation in progress can be aborted by asserting a Start condition at any time. Aborting an operation using the Start condition will prepare the FM24C16A for a new operation.

If during operation the power supply drops below the specified VDD minimum, the system should issue a Start condition prior to performing another operation.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high. For system design considerations, keeping SCL in a low state while idle improves robustness.

Acknowledge

The Acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state, the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a No-Acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the No-Acknowledge ends the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24C16A will continue to place data onto the bus as long as the receiver sends Acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24C16A to attempt to drive the bus on the next clock while the master is sending a new command such as a Stop.

Slave Address

The first byte that the FM24C16A expects after a Start condition is the slave address. As shown in Figure 4, the slave address contains the device type, the page of memory to be accessed, and a bit that specifies if the transaction is a read or a write.

Bits 7-4 are the device type and should be set to 1010b for the FM24C16A. The device type allows other types of functions to reside on the 2-wire bus within an identical address range. Bits 3-1 are the page select. They specify the 256-byte block of memory that is targeted for the current operation. Bit 0 is the read/write bit. A 0 indicates a write operation.

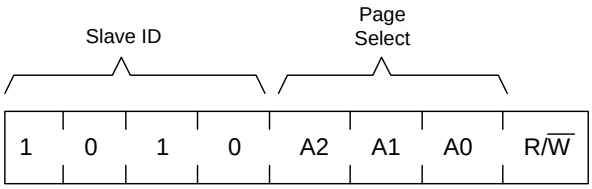


Figure 4. Slave Address

Word Address

After the FM24C16A (as receiver) acknowledges the slave ID, the master will place the word address on the bus for a write operation. The word address is the lower 8-bits of the address to be combined with the 3-bits of the page select to specify the exact byte to be written. The complete 11-bit address is latched internally.

No word address occurs for a read operation, though the 3-bit page select is latched internally. Reads always use the lower 8-bits that are held internally in the address latch. That is, reads always begin at the address following the previous access. A random read address can be loaded by doing a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24C16A increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFh) is reached, the address latch will roll over to 000h. There is no limit on the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After all address information has been transmitted, data transfer between the bus master and the FM24C16A can begin. For a read operation the device will place 8 data bits on the bus then wait for an acknowledge. If the acknowledge occurs, the next sequential byte will be transferred. If the acknowledge is not sent, the read operation is concluded. For a write operation, the FM24C16A will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24C16A is designed to operate in a manner very similar to other 2-wire interface memory products. The major differences result from the higher performance write capability of FRAM technology. These improvements result in some differences between the FM24C16A and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave ID then a word address as previously mentioned. The bus master indicates a write operation by setting the LSB of the Slave Address to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFh to 000h.

Unlike other nonvolatile memory technologies, there is no write delay with FRAM. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ‘ready’ condition.

An actual memory array write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using start or stop condition prior to the 8th data bit. The FM24C16A needs no page buffering.

The memory array can be write protected using the WP pin. Setting the WP pin to a high condition (VDD) will write-protect all addresses. The FM24C16A will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a low state (VSS) will deactivate this feature.

Figure 5 and 6 below illustrates both a single-byte and multiple-byte writes.

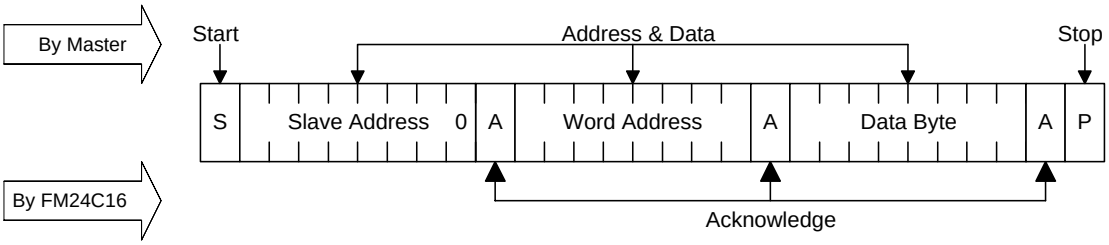


Figure 5. Single Byte Write

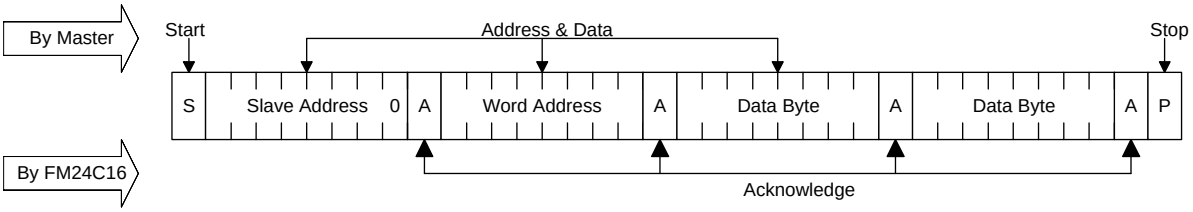


Figure 6. Multiple Byte Write

Read Operation

There are two types of read operations. They are current address read and selective address read. In a current address read, the FM24C16A uses the internal address latch to supply the lower 8 address bits. In a selective read, the user performs a procedure to set these lower address bits to a specific value.

Current Address & Sequential Read

As mentioned above the FM24C16A uses an internal latch to supply the lower 8 address bits for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. This is the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to 1. This indicates that a read operation is requested. The 3 page select bits in the slave ID specify the block of memory that is used for the read operation. On the next clock, the FM24C16A will begin shifting out data from the current address. The current address is the 3 bits from the slave ID combined with the 8 bits that were in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte, the internal address counter will be incremented. Each time the bus master acknowledges a byte this indicates that the FM24C16A should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24C16A attempts to read out additional data onto the bus. The four valid methods are as follows.

1. The bus master issues a no-acknowledge in the 9th clock cycle and a stop in the 10th clock cycle. This is illustrated in the diagrams below. This is the preferred method.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a start in the 10th.
3. The bus master issues a stop in the 9th clock cycle. Bus contention may result.
4. The bus master issues a start in the 9th clock cycle. Bus contention may result.

If the internal address reaches 7FFh it will wrap around to 000h on the next read cycle. Figures 7 and 8 show the proper operation for current address reads.

Selective (Random) Read

A simple technique allows a user to select a random address location as the starting point for a read operation. It uses the first two bytes of a write operation to set the internal address byte followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the word address byte that is loaded into the internal address latch. After the FM24C16A acknowledges the word address, the bus master issues a start condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address set to 1.

The operation is now a current address read. This operation is illustrated in Figure 9.

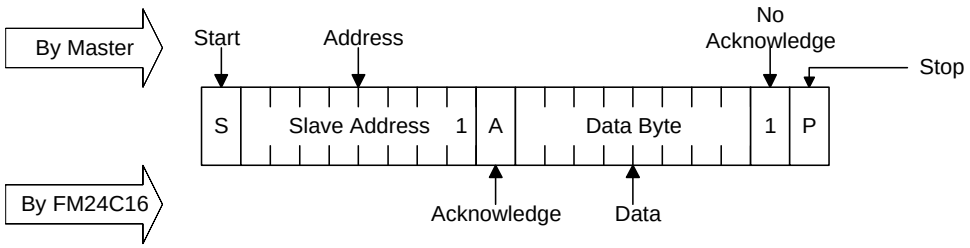


Figure 7. Current Address Read

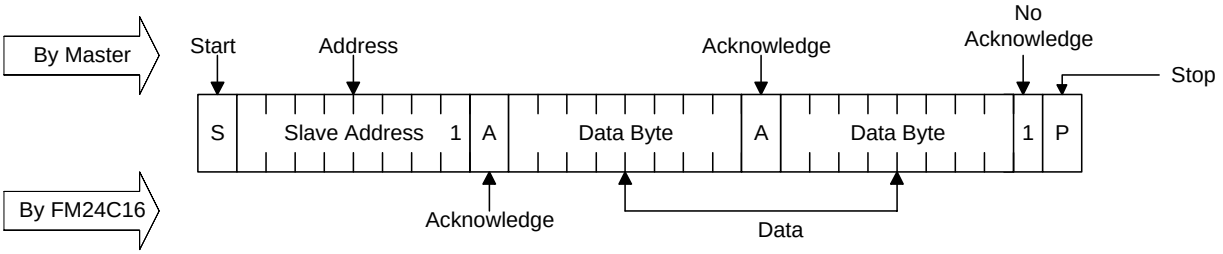


Figure 8. Sequential Read

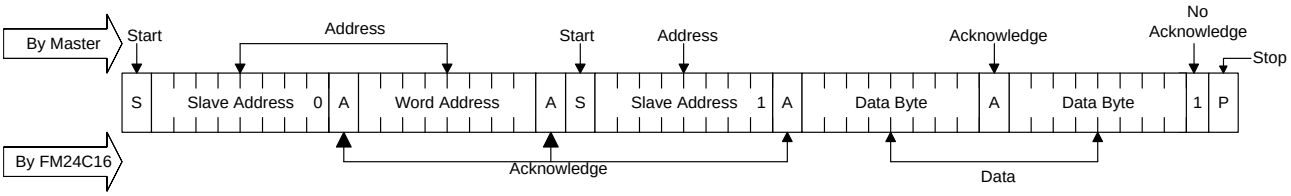


Figure 9. Selective (Random) Read

Endurance

The FM24C16A internally operates with a read and restore mechanism. Therefore, endurance cycles are applied for each read or write cycle. The FRAM architecture is based on an array of rows and columns. Rows are defined by A10-A3. Each access causes an endurance cycle for a row. Endurance can be optimized by ensuring frequently accessed data is placed in different rows. Regardless, FRAM read and write endurance is effectively unlimited at the 1MHz two-wire speed. Even at 3000 accesses per second to the same row, 10 years time will elapse before 1 trillion endurance cycles occur.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V *
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	 4kV 1kV 300V
	Package Moisture Sensitivity Level	MSL-1

* Exception: The "$V_{IN} < V_{DD}$+1.0V" restriction does not apply to the SCL and SDA inputs.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	4.5	5.0	5.5	V	
I_{DD}	VDD Supply Current @ SCL = 100 kHz @ SCL = 400 kHz @ SCL = 1 MHz		 115 400 800	 150 500 1000	 µA µA µA	1
I_{SB}	Standby Current		1	10	µA	2
I_{LI}	Input Leakage Current			±1	µA	3
I_{LO}	Output Leakage Current			±1	µA	3
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage @ I_{OL} = 3 mA			 0.4	 V	
R_{IN}	Input Resistance (WP pin) For $V_{IN} = V_{IL}$ (max) For $V_{IN} = V_{IH}$ (min)	 50 1			 KΩ MΩ	 5
V_{HYS}	Input Hysteresis	0.05 V_{DD}			V	4

Notes

1. SCL toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V.
3. 2. SCL = SDA = V_{DD}. All inputs V_{SS} or V_{DD}. Stop command issued.
4. 3. V_{IN} or $V_{OUT} = V_{SS}$ to V_{DD}. Does not apply to WP pin.
5. 4. This parameter is characterized but not tested.
6. 5. The input pull-down circuit is strong (50KΩ) when the input voltage is below V_{IL} and much weaker (1MΩ) when the input voltage is above V_{IH}.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz	1
t_{LOW}	Clock Low Period	4.7		1.3		0.6		µs	
t_{HIGH}	Clock High Period	4.0		0.6		0.4		µs	
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9		0.55	µs	
t_{BUF}	Bus Free Before New Transmission	4.7		1.3		0.5		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		0.25		µs	
$t_{SU:STA}$	Start Condition Setup for Repeated Start	4.7		0.6		0.25		µs	
$t_{HD:DAT}$	Data In Hold Time	0		0		0		ns	
$t_{SU:DAT}$	Data In Setup Time	250		100		100		ns	
t_R	Input Rise Time		1000		300		300	ns	2
t_F	Input Fall Time		300		300		100	ns	2
$t_{SU:STO}$	Stop Condition Setup	4.0		0.6		0.25		µs	
t_{DH}	Data Output Hold (from SCL @ V_{IL})	0		0		0		ns	
t_{SP}	Noise Suppression Time Constant on SCL, SDA		50		50		50	ns	

Notes : All SCL specifications as well as start and stop conditions apply to both read and write operations.
1 The speed-related specifications are guaranteed characteristic points from DC to 1 MHz.
2 This parameter is periodically sampled and not 100% tested.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	1
C_{IN}	Input Capacitance	6	pF	1

Notes
1 This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Equivalent AC Load Circuit

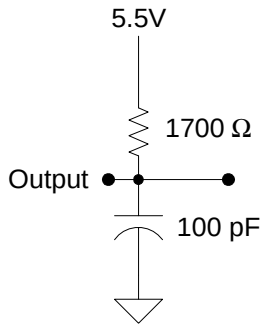
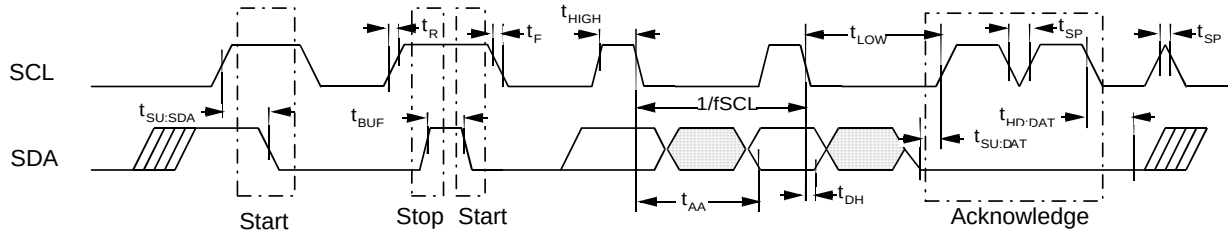


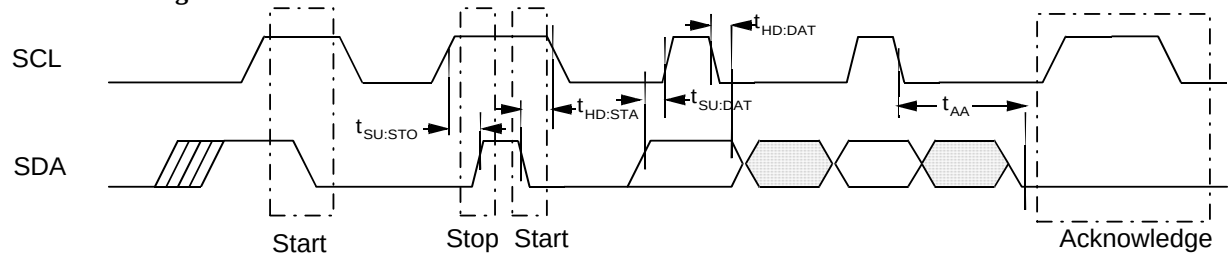
Diagram Notes

All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

Read Bus Timing



Write Bus Timing

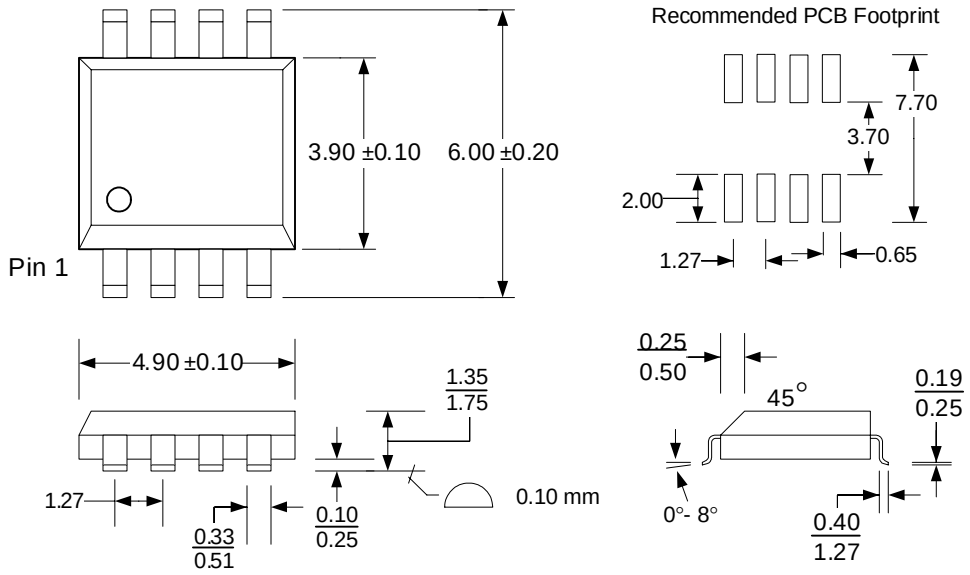


Data Retention (V_{DD} = 4.5V to 5.5V, +85° C)

Parameter	Min	Units	Notes
Data Retention	45	Years	

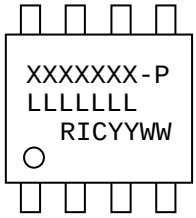
Mechanical Drawing

8-pin SOIC (JEDEC Standard MS-012 variation AA)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme



Legend:
XXXX= part number, P= package type
LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM24C16A, Standard SOIC package, Year 2004, Work Week 39
FM24C16A-S
A40003S
RIC0439

Revision History

Revision	Date	Summary
0.1	6/26/02	Initial Release
2.0	7/23/03	Changed to Production status.
2.1	3/17/04	Added “green” package. Updated package drawing.
3.0	3/29/05	Changed Data Retention spec. Added ESD and package MSL ratings. Added pcb footprint drawing. New rev. number and 1st page footer to comply with new scheme.