# HN27C4096AHG/AHCC Series —— Preliminary

**262144-word x 16-bit CMOS UV Erasable and Programmable ROM**

The Hitachi HN27C4096AHG/AHCC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring burst access mode to get very high speed 4-word serial access. Fabricated on advanced fine process and high speed circuitry technique including burst access, the HN27C4096AHG/AHCC makes high speed access time possible. Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 80286 and 68020. The HN27C4096AHG/AHCC offers high speed programming using page programming mode. This device has the package variation of cerdip-40pin and JLCC-44pin.

## Features

- High speed: Access time 85 ns (max)
  Burst access time: 45 ns (max)
- Low power dissipation:
  Active mode; 35 mW/MHz (typ)
- Fast high reliability page programming and fast high-reliability programming
  Programming voltage; +12.5 V D.C.
  Program time; 3.5 sec (min)
  (Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 40-pin JEDEC standard
  44-pin JLCC JEDEC standard
- Device identifier mode: Manufacturer code and device code
- Fully compatible with the HN27C4096HG/HCC Series, without burst access mode

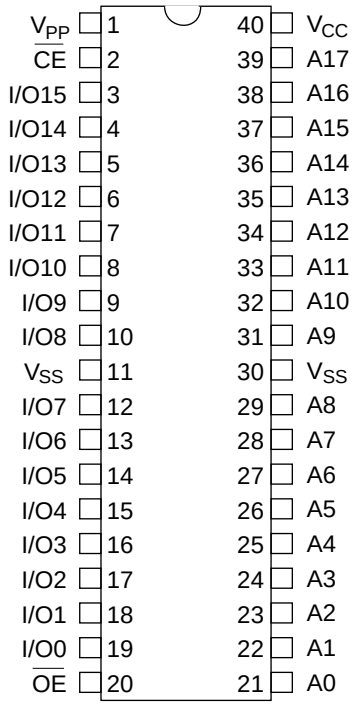
## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HN27C4096AHG-85 | 85 ns | 600-mil 40-pin cerdip (DG-40A) |
| HN27C4096AHCC-85 | 85 ns | 44-pin J-bend leaded chip carrier (CC-44) |

Note: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

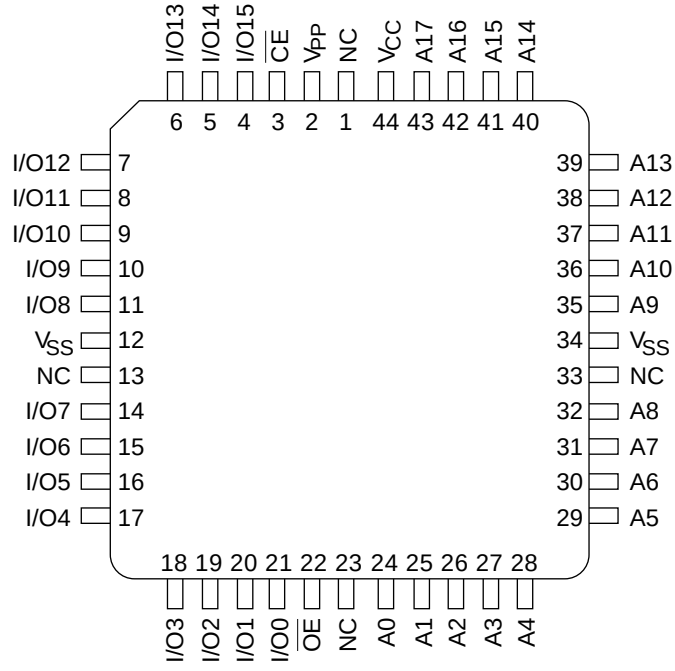
## Pin Arrangement

HN27C4096AHG Series




(Top view)

HN27C4096AHCC Series

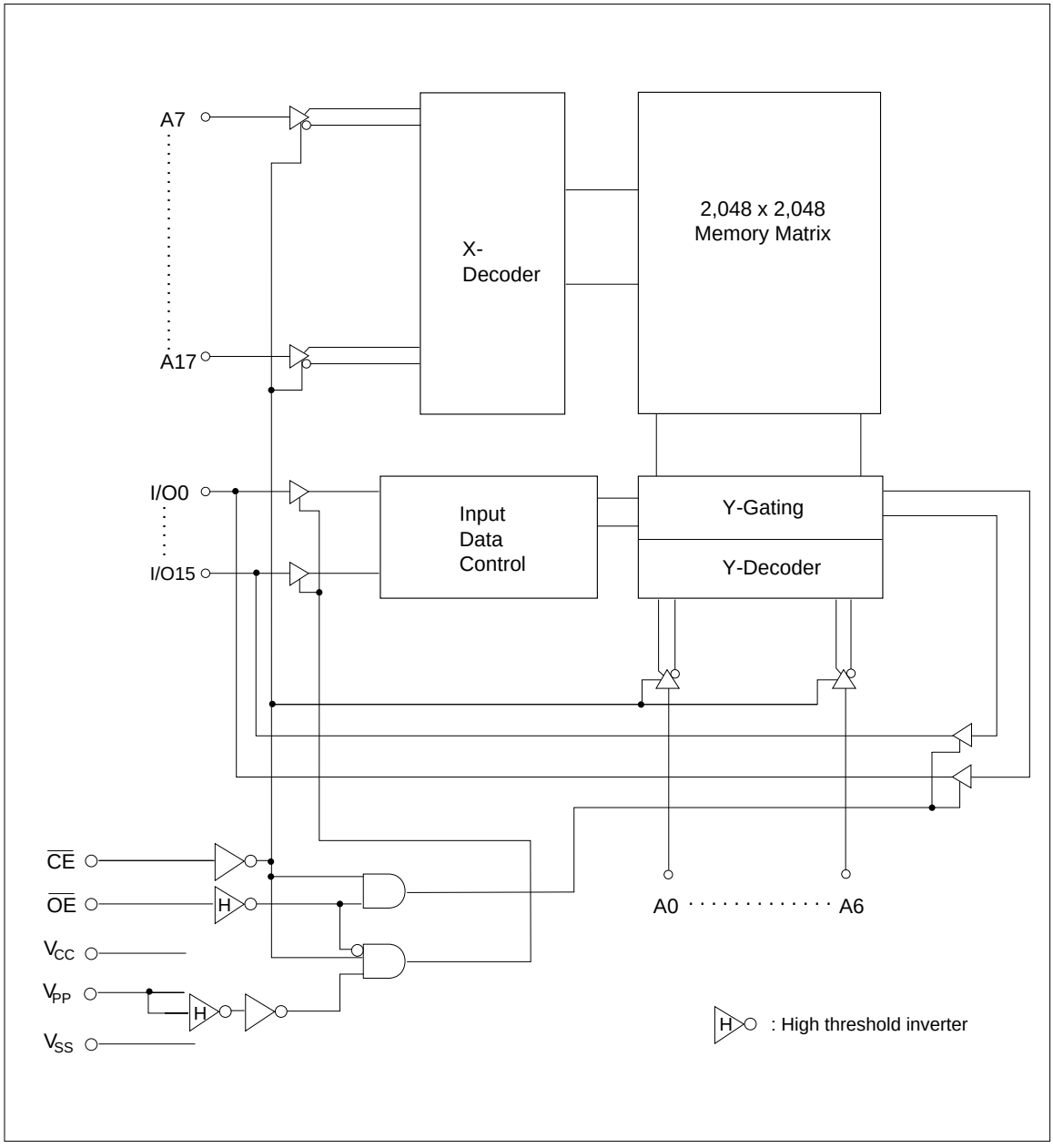



(Top view)

## Pin Description

| Pin name | Function |
|---|---|
| A0 – A17 | Address |
| I/O0 – I/O15 | Input/output |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{PP}$ | Programming power supply |
| $V_{SS}$ | Ground |

## Block Diagram



## Mode Selection

| Mode | | Pin | $\overline{CE}$ | $\overline{OE}$ | A9 | $V_{PP}$ | $V_{CC}$ | I/O |
|---|---|---|---|---|---|---|---|---|
| | | CC-44 | (3) | (22) | (35) | (2) | (44) | (4 – 11, 14 – 21) |
| | | DG-40A | (2) | (20) | (31) | (1) | (40) | (3 – 10, 12 – 19) |
| Read | | | $V_{IL}$ | $V_{IL}$ | X | $V_{SS}$ – $V_{CC}$ | $V_{CC}$ | Dout |
| Output disable | | | $V_{IL}$ | $V_{IH}$ | X | $V_{SS}$ – $V_{CC}$ | $V_{CC}$ | High-Z |
| Standby | | | $V_{IH}$ | X | X | $V_{SS}$ – $V_{CC}$ | $V_{CC}$ | High-Z |
| Page program | Page program set | | $V_{IH}$ | $V_H$*2 | X | $V_{PP}$ | $V_{CC}$ | High-Z |
| | Page data latch | | $V_{IL}$ | $V_H$*2 | X | $V_{PP}$ | $V_{CC}$ | Din |
| | Page program | | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | High-Z |
| | Page program verify | | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | Dout |
| | Page program reset | | $V_{IH}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | High-Z |
| Word program | Program | | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | Din |
| | Program verify | | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | Dout |
| | Optional verify | | $V_{IL}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | Dout |
| | Program inhibit | | $V_{IH}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | High-Z |
| Identifier | | | $V_{IL}$ | $V_{IL}$ | $V_H$*2 | $V_{SS}$ – $V_{CC}$ | $V_{CC}$ | Code |

Notes: 1. X: Don't care.
2. $V_H$: 12.0 V ± 0.5 V

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| All input and output voltages*1 | Vin, Vout | –0.6*2 to +7.0 | V |
| Voltage on pin A9 and $\overline{OE}$ | $V_{ID}$ | –0.6*2 to +13.0 | V |
| $V_{PP}$ voltage *1 | $V_{PP}$ | –0.6 to +13.5 | V |
| $V_{CC}$ voltage *1 | $V_{CC}$ | –0.6 to +7.0 | V |
| Operating temperature range | Topr | 0 to +70 | °C |
| Storage temperature range *3 | Tstg | –65 to +125 | °C |
| Storage temperature under bias | Tbias | –20 to +80 | °C |

Notes: 1. Relative to $V_{SS}$.
2. Vin, Vout, $V_{ID}$ min = –2.0 V for pulse width $\leq$ 20 ns
3. Storage temperature range of device before programming.

## Capacitance (Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance | Cin | — | — | 12 | pF | Vin = 0 V |
| Output capacitance | Cout | — | — | 20 | pF | Vout = 0 V |

## Read Operation

**DC Characteristics** ($V_{CC}$ = 5 V ± 10%, $V_{PP}$ = $V_{SS}$ to $V_{CC}$, Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | — | — | 2 | µA | Vin = 5.5 V |
| Output leakage current | $I_{LO}$ | — | — | 2 | µA | Vout = 5.5 V/0.45 V |
| $V_{PP}$ current | $I_{PP1}$ | — | 1 | 20 | µA | $V_{PP}$ = 5.5 V |
| Standby $V_{CC}$ current | $I_{SB}$ | — | — | 30 | mA | $\overline{CE}$ = $V_{IH}$ |
| Operating $V_{CC}$ current | $I_{CC1}$ | — | — | 35 | mA | Iout = 0 mA, f = 1 MHz |
| | $I_{CC2}$ | — | — | 140 | mA | Iout = 0 mA, f = 11.8 MHz |
| Input voltage | $V_{IL}$ | –0.3*[1] | — | 0.8 | V | |
| | $V_{IH}$ | 2.2 | — | $V_{CC}$+1*[2] | V | |
| Output voltage | $V_{OL}$ | — | — | 0.45 | V | $I_{OL}$ = 2.1 mA |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –400 µA |

Notes: 1. $V_{IL}$ min = –1.0 V for pulse width ≤ 50 ns
$V_{IL}$ min = –2.0 V for pulse width ≤ 20 ns
2. $V_{IH}$ max = $V_{CC}$ +1.5 V for pulse width ≤ 20 ns
If $V_{IH}$ is over the specified maximum value, read operation cannot be guaranteed.

**AC Characteristics** ($V_{CC}$ = 5 V ± 10%, $V_{PP}$ = $V_{SS}$ to $V_{CC}$, Ta = 0 to +70°C)

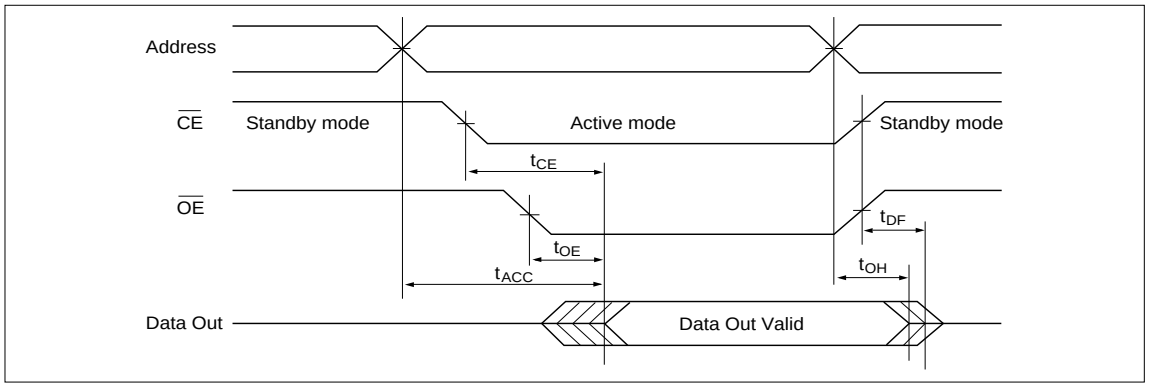
**Test Conditions**
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 1.5 V

**AC Characteristics** ($V_{CC}$ = 5 V ± 10%, $V_{PP}$ = $V_{SS}$ to $V_{CC}$, Ta = 0 to +70°C) (cont.)

| | | HN27C4096AHG/AHCC-85 | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Test conditions** |
| Address to output delay | $t_{ACC}$ | — | 85 | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ |
| $\overline{CE}$ to output delay | $t_{CE}$ | — | 85 | ns | $\overline{OE}$ = $V_{IL}$ |
| $\overline{OE}$ to output delay | $t_{OE}$ | — | 45 | ns | $\overline{CE}$ = $V_{IL}$ |
| Burst address output delay | $t_{BAC}$ | — | 45 | ns | $\overline{CE}$ = $V_{IL}$ |
| $\overline{OE}$ high to output float *1 | $t_{DF}$ | 0 | 30 | ns | $\overline{CE}$ = $V_{IL}$ |
| Address to output hold | $t_{OH}$ | 5 | — | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ |

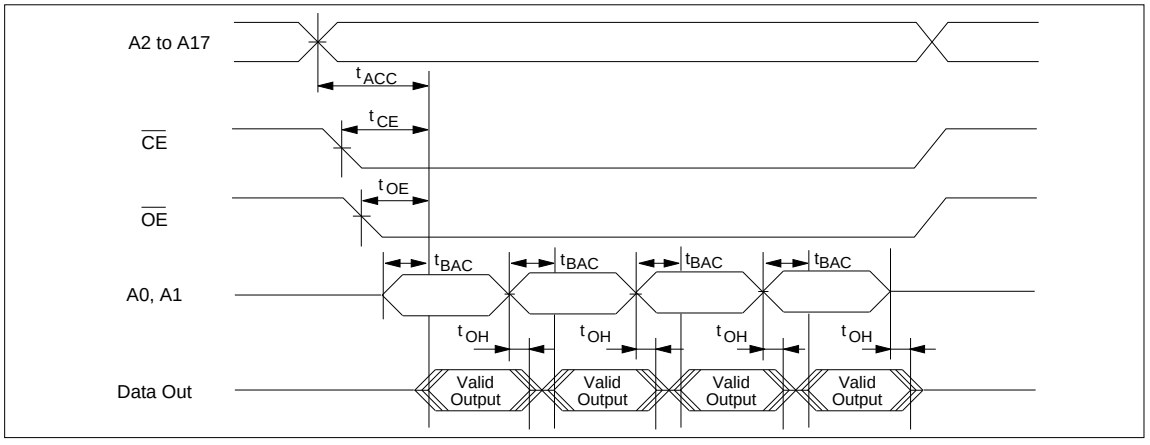
Note: 1. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## Read Timing Waveform




## Read Timing Waveform (Burst access mode)

In Burst access mode, fast read-out of 4 word data is selected by address A0, A1.



## Fast High-Reliability Page Programming

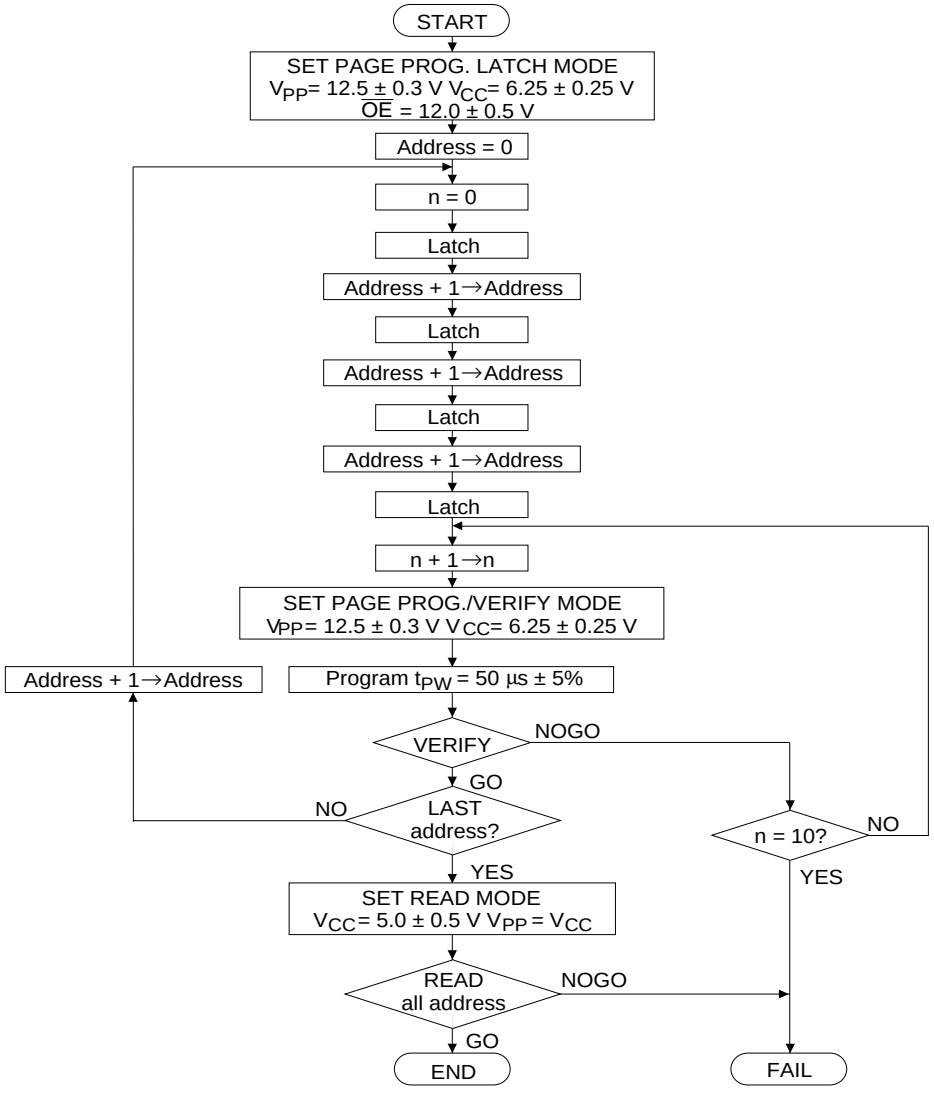
This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

### Page Program Set

Apply 12 V to $\overline{OE}$ pin after applying 12.5 V to $V_{PP}$ to set a page program mode.
The device operates in a page program mode until reset.

### Page Program Reset

Set $V_{PP}$ to $V_{CC}$ level or less to reset a page program mode.




Fast High-Reliability Page Programming Flowchart

**DC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | — | — | 2 | µA | Vin = 6.5 V/0.45 V |
| Output voltage during verify | $V_{OL}$ | — | — | 0.45 | V | $I_{OL}$ = 2.1 mA |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –400 µA |
| Operating $V_{CC}$ current | $I_{CC}$ | — | — | 50 | mA | |
| Input voltage | $V_{IL}$ | –0.1*5 | — | 0.8 | V | |
| | $V_{IH}$ | 2.2 | — | $V_{CC}$+0.5*6 | V | |
| | $V_H$ | 11.5 | 12.0 | 12.5 | V | |
| $V_{PP}$ supply current | $I_{PP}$ | — | — | 70 | mA | $\overline{CE}$=$V_{IL}$ |

Notes:
1. $V_{CC}$ must be applied before $V_{PP}$ and removed after $V_{PP}$.
2. $V_{PP}$ must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}$ = 12.5 V.
4. Do not alter $V_{PP}$ either $V_{IL}$ to 12.5 V or 12.5 V to $V_{IL}$ when $\overline{CE}$ = low.
5. $V_{IL}$ min = –0.6 V for pulse width $\leq$ 20 ns.
6. If $V_{IH}$ is over the specified maximum value, programming operation cannot be guaranteed.

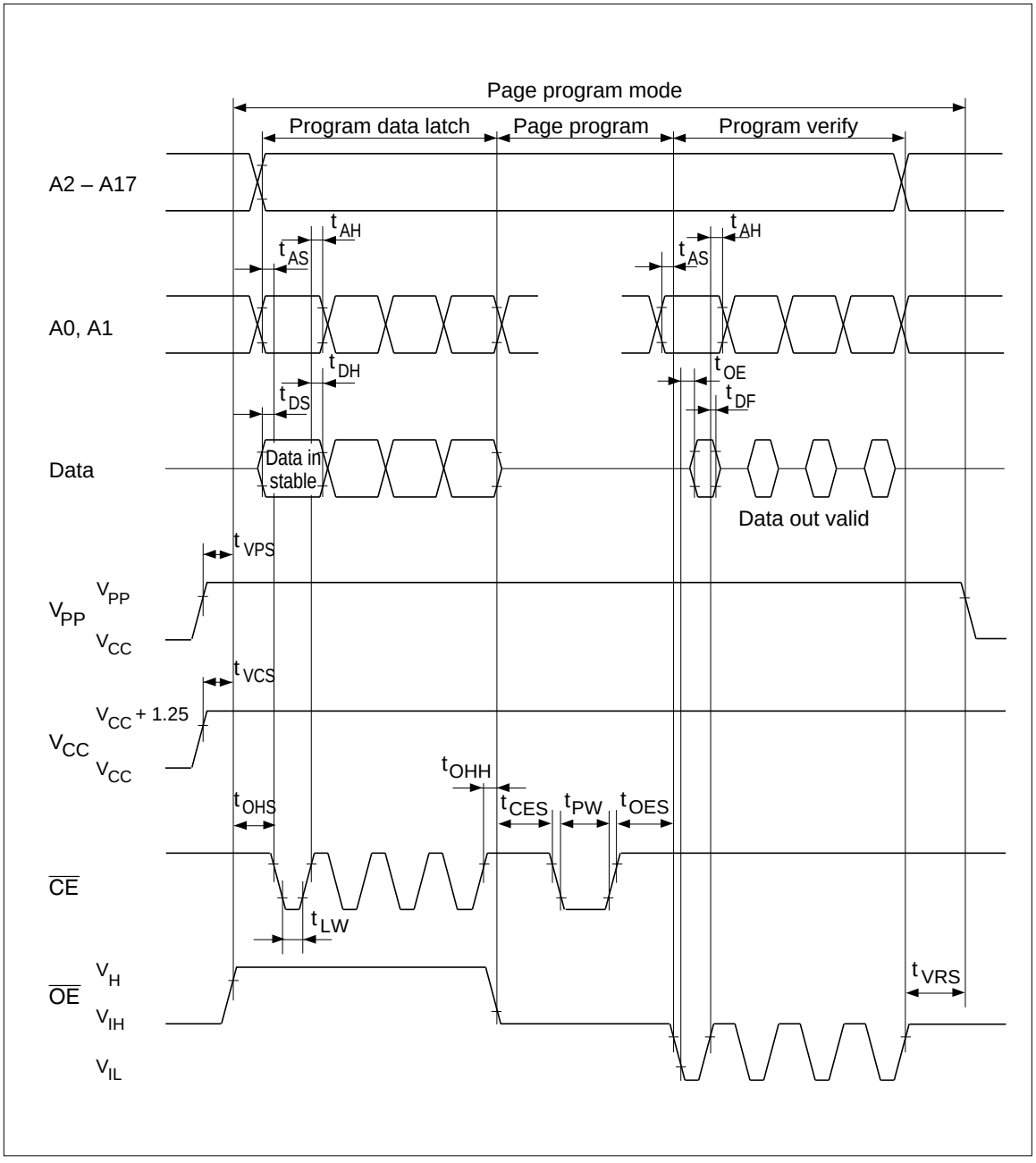
**AC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

**Test Conditions**
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing:
  Inputs; 0.8 V, 2.0 V,
  Outputs; 0.8 V, 2.0 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | — | — | µs | |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | — | — | µs | |
| Data setup time | $t_{DS}$ | 2 | — | — | µs | |
| Address hold time | $t_{AH}$ | 0 | — | — | µs | |
| Data hold time | $t_{DH}$ | 2 | — | — | µs | |
| $\overline{OE}$ high to output float delay | $t_{DF}$*1 | 0 | — | 130 | ns | |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | — | — | µs | |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | — | — | µs | |
| $\overline{CE}$ programming pulse width | $t_{PW}$ | 47.5 | 50.0 | 52.5 | µs | |
| $\overline{CE}$ setup time | $t_{CES}$ | 2 | — | — | µs | |
| Data valid from $\overline{OE}$ | $t_{OE}$ | 0 | — | 150 | ns | |
| $\overline{CE}$ pulse width during data latch | $t_{LW}$ | 1 | — | — | µs | |
| $\overline{OE}$ = $V_H$ setup time | $t_{OHS}$ | 2 | — | — | µs | |
| $\overline{OE}$ = $V_H$ hold time | $t_{OHH}$ | 2 | — | — | µs | |
| $\overline{OE}$ hold time | $t_{OEH}$ | 2 | — | — | µs | |
| $V_{PP}$ hold time*2 | $t_{VRS}$ | 1 | — | — | µs | |

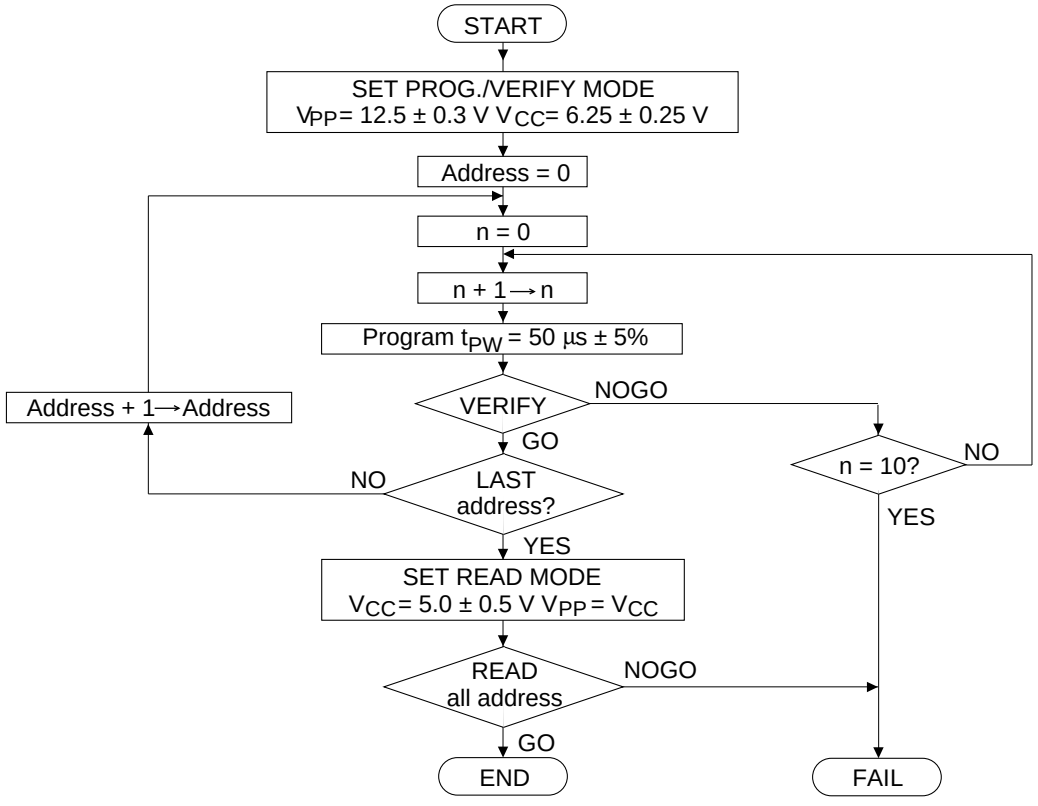
Notes: 1. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Page program mode will be reset when $V_{PP}$ is set to $V_{CC}$ or less.

**Fast High-Reliability Page Programming Timing Waveform**



## Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.




Fast High-Reliability Programming Flowchart

**DC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ =12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | — | — | 2 | µA | Vin = 6.5 V/0.45 V |
| $V_{PP}$ supply current | $I_{PP}$ | — | — | 40 | mA | $\overline{CE}$ = $V_{IL}$ |
| Operating $V_{CC}$ current | $I_{CC}$ | — | — | 50 | mA | |
| Input voltage | $V_{IL}$ | –0.1*5 | — | 0.8 | V | |
| | $V_{IH}$ | 2.2 | — | $V_{CC}$ +0.5*6 | V | |
| Output voltage | $V_{OL}$ | — | — | 0.45 | V | $I_{OL}$ = 2.1 mA |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –400 µA |

Notes: 1. $V_{CC}$ must be applied before $V_{PP}$ and removed after $V_{PP}$.
2. $V_{PP}$ must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}$ = 12.5 V.
4. Do not alter $V_{PP}$ either $V_{IL}$ to 12.5 V or 12.5 V to $V_{IL}$ when $\overline{CE}$ = low.
5. $V_{IL}$ min = –0.6 V for pulse width ≤ 20 ns.
6. If $V_{IH}$ is over the specified maximum value, programming operation cannot be guaranteed.

**AC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

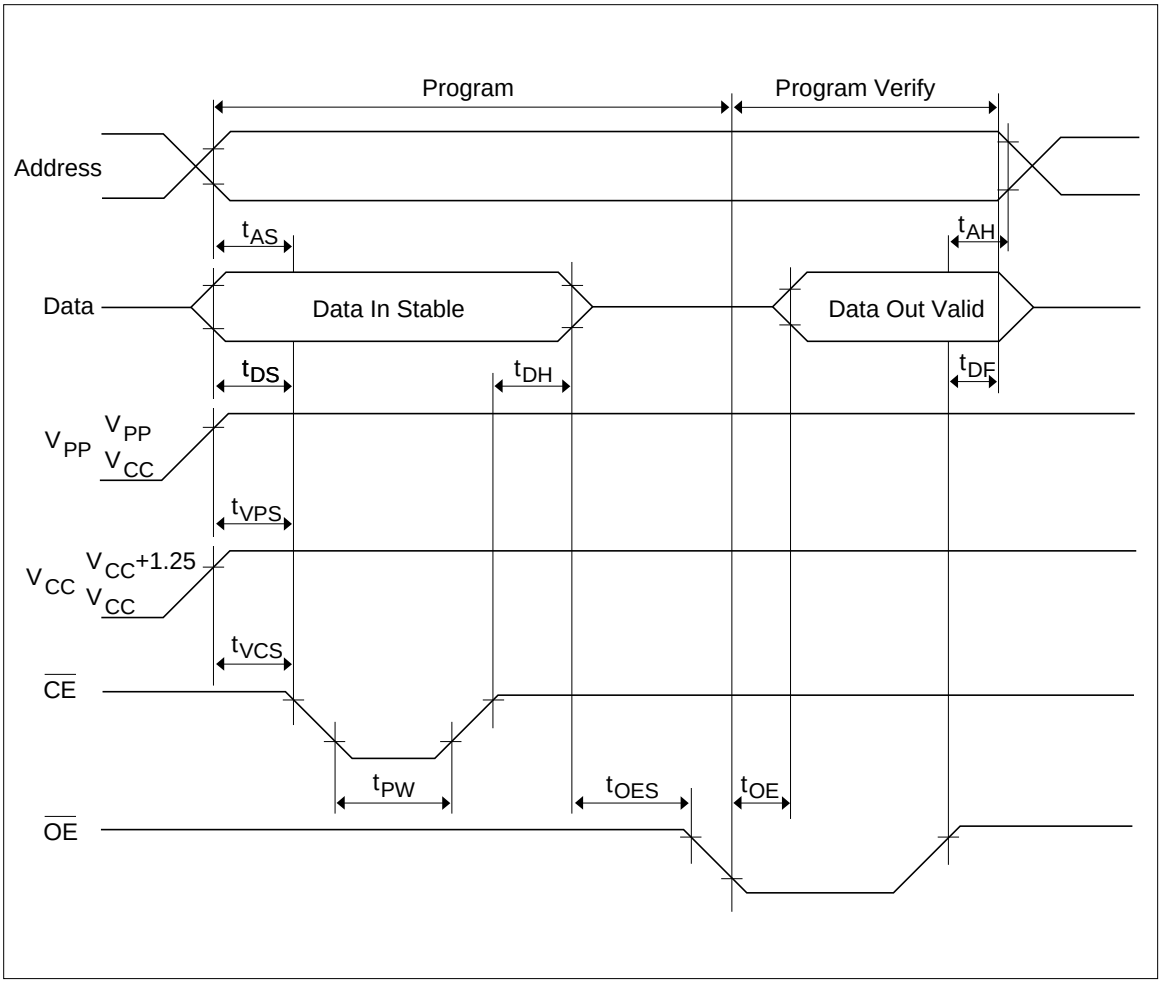
**Test Conditions**

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timings:
  Inputs: 0.8 V, 2.0 V
  Outputs: 0.8 V, 2.0 V

| Paramerter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | — | — | µs | |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | — | — | µs | |
| Data setup time | $t_{DS}$ | 2 | — | — | µs | |
| Address hold time | $t_{AH}$ | 0 | — | — | µs | |
| Data hold time | $t_{DH}$ | 2 | — | — | µs | |
| $\overline{OE}$ to output float delay | $t_{DF}$*1 | 0 | — | 130 | ns | |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | — | — | µs | |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | — | — | µs | |
| $\overline{CE}$ programming pulse width | $t_{PW}$ | 47.5 | 50.0 | 52.5 | µs | |
| Data valid from $\overline{OE}$ | $t_{OE}$ | 0 | — | 150 | ns | |

Note: 1. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

**Fast High-Reliability Programming Timing Waveform**

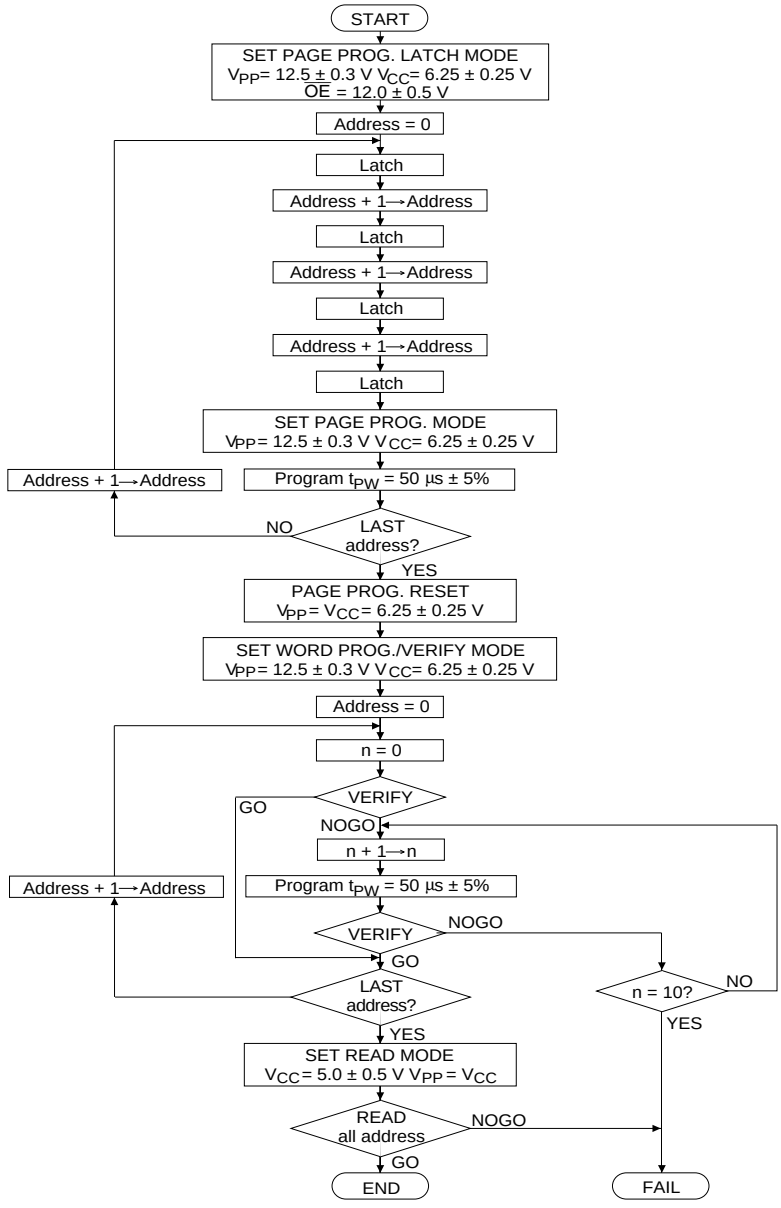


## Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.




Optional Page Programming Flowchart

**DC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ =12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | — | — | 2 | µA | Vin = 6.5 V/0.45 V |
| Output voltage during verify | $V_{OL}$ | — | — | 0.45 | V | $I_{OL}$ = 2.1 mA |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –400 µA |
| Operating $V_{CC}$ current | $I_{CC}$ | — | — | 50 | mA | |
| Input voltage | $V_{IL}$ | –0.1*5 | — | 0.8 | V | |
| | $V_{IH}$ | 2.2 | — | $V_{CC}$ +0.5*6 | V | |
| | $V_H$ | 11.5 | 12.0 | 12.5 | V | |
| $V_{PP}$ supply current | $I_{PP}$ | — | — | 70 | mA | $\overline{CE}$ = $V_{IL}$ |

Notes:
1. $V_{CC}$ must be applied before $V_{PP}$ and removed after $V_{PP}$.
2. $V_{PP}$ must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}$ = 12.5 V.
4. Do not alter $V_{PP}$ either $V_{IL}$ to 12.5 V or 12.5 V to $V_{IL}$ when $\overline{CE}$ = low.
5. $V_{IL}$ min = –0.6 V for pulse width $\leq$ 20 ns.
6. If $V_{IH}$ is over the specified maximum value, programming operation cannot be guaranteed.

**AC Characteristics** ($V_{CC}$ = 6.25 V ± 0.25 V, $V_{PP}$ = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

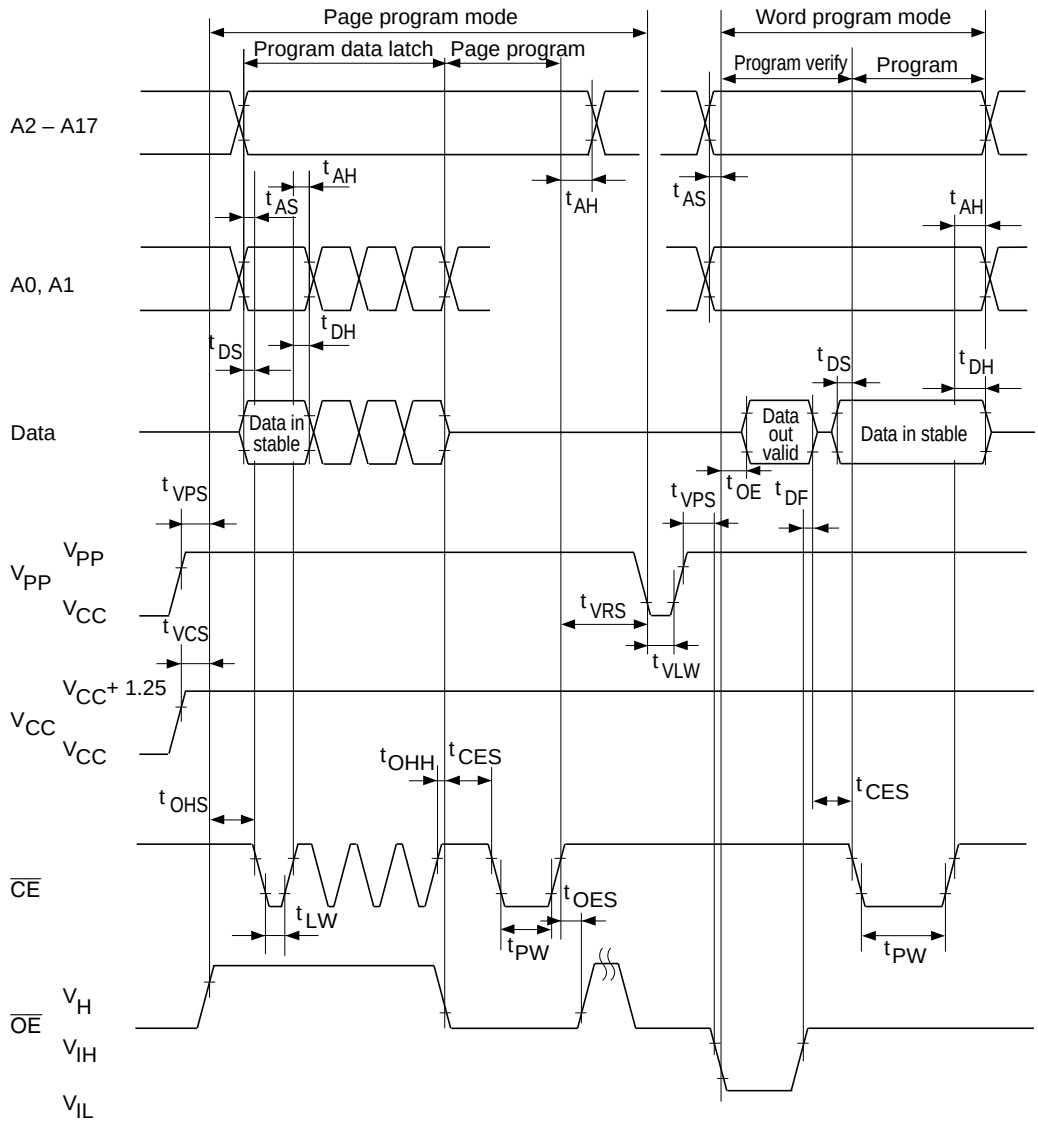
**Test Conditions**

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timings:
  Inputs; 0.8 V, 2.0 V
  Outputs; 0.8 V, 2.0 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | — | — | µs | |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | — | — | µs | |
| Data setup time | $t_{DS}$ | 2 | — | — | µs | |
| Address hold time | $t_{AH}$ | 0 | — | — | µs | |
| Data hold time | $t_{DH}$ | 2 | — | — | µs | |
| $\overline{OE}$ high to output float delay | $t_{DF}$*1 | 0 | — | 130 | ns | |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | — | — | µs | |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | — | — | µs | |
| $\overline{CE}$ initial programming pulse width | $t_{PW}$ | 47.5 | 50.0 | 52.5 | µs | |
| $\overline{CE}$ setup time | $t_{CES}$ | 2 | — | — | µs | |
| Data valid from $\overline{OE}$ | $t_{OE}$ | 0 | — | 150 | ns | |
| $\overline{CE}$ pulse width during data latch | $t_{LW}$ | 1 | — | — | µs | |
| $\overline{OE}$ = $V_H$ setup time | $t_{OHS}$ | 2 | — | — | µs | |
| $\overline{OE}$ = $V_H$ hold time | $t_{OHH}$ | 2 | — | — | µs | |
| Page programming reset time *2 | $t_{VLW}$ | 1 | — | — | µs | |
| $V_{PP}$ hold time *2 | $t_{VRS}$ | 1 | — | — | µs | |

Notes: 1. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Page program mode will be reset when $V_{PP}$ is set to $V_{CC}$ or less.

**Option Page Programming Timing Waveform**



## Erase

Erasure of the HN27C4096AHG/AHCC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity X exposure time) for erasure is 15 W•sec/cm$^2$.

## Mode Description

### Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

**HN27C4096AHG/AHCC Identifier Code**

| | A0 | I/O8-I/O15 | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CC-44 | (24) | (11-4) | (14) | (15) | (16) | (17) | (18) | (19) | (20) | (21) | |
| Identifier | DG-40A | (21) | (10-3) | (12) | (13) | (14) | (15) | (16) | (17) | (18) | (19) | Hex Data |
| Manufacturer code | | $V_{IL}$ | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| Device code | | $V_{IH}$ | X | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2 |

Notes: 1. $V_{CC}$ = 5.0 V ± 10%
2. A9 = 12.0 V ± 0.5 V
3. $\overline{CE}$, $\overline{OE}$ = $V_{IL}$
4. A1 – A8, A10 – A17: Don't care.
5. X: Don't care.