

## 27C256/87C256 256K (32K × 8) CMOS UV Erasable PROM

### Preliminary Specification

#### Application Specific Products

#### FEATURES

- CMOS/NMOS microcontroller and microprocessor compatible
  - 87C256-Integrated address latch
  - Universal 28-Pin memory site, 2-line control
- Low power consumption
  - 10mA maximum CMOS active current
  - 100µA maximum CMOS standby current
- High-performance speeds
  - 170ns maximum access time
- Noise immunity features
  - ±10% V<sub>CC</sub> tolerance
  - Maximum latch-up immunity through epitaxial processing
- Fast, reliable intelligent programming
  - 12.5V V<sub>PP</sub>

#### DESCRIPTION

Signetics' 27C256 and 87C256 CMOS EPROMs are 256K-bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 87C256 has been optimized

for multiplexed bus microcontroller and microprocessor compatibility while the 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

The 27C256 and 87C256 achieve both high-performance (170ns access time for 27C256) and low power consumption (10mA active current maximum, CMOS inputs) making them, ideal for high-performance, portable equipment.

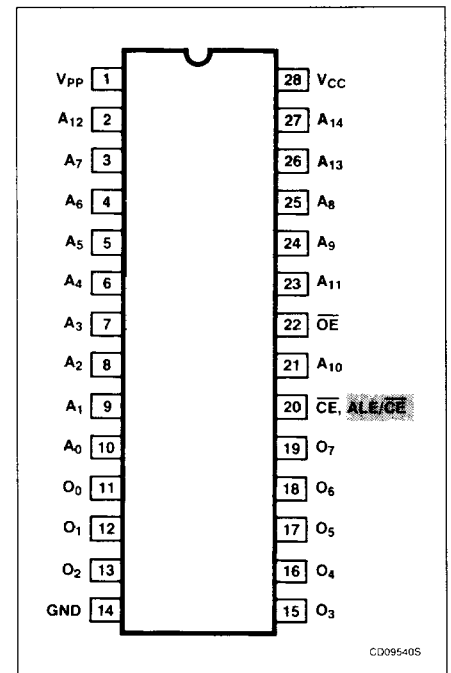
The highest degree of protection against latch-up is achieved through epitaxial processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins from -1V to V<sub>CC</sub> + 1V.

The 87C256 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can tie combined (multiplexed) address-data processor busses directly into both the A<sub>0</sub>-A<sub>14</sub> and O<sub>0</sub>-O<sub>7</sub> pins of the 87C256. During ALE high (ALE/ $\overline{CE}$ ) the address information is allowed to flow into the EPROM and begin accessing the stored code. On the

falling edge of the ALE input (ALE/ $\overline{CE}$ ), address information at the address inputs is latched internally. The A<sub>0</sub>-A<sub>7</sub> inputs are then ignored as data information is passed on the same bus from the EPROM O<sub>0</sub>-O<sub>7</sub> Pins (ALE/ $\overline{CE}$  remains low).

The 27C256 and 87C256 are offered in ceramic DIP Packages. Both devices can be programmed with standard EPROM Programmers and the intelligent programming algorithm may be utilized.

#### PIN CONFIGURATION



#### BLOCK DIAGRAM

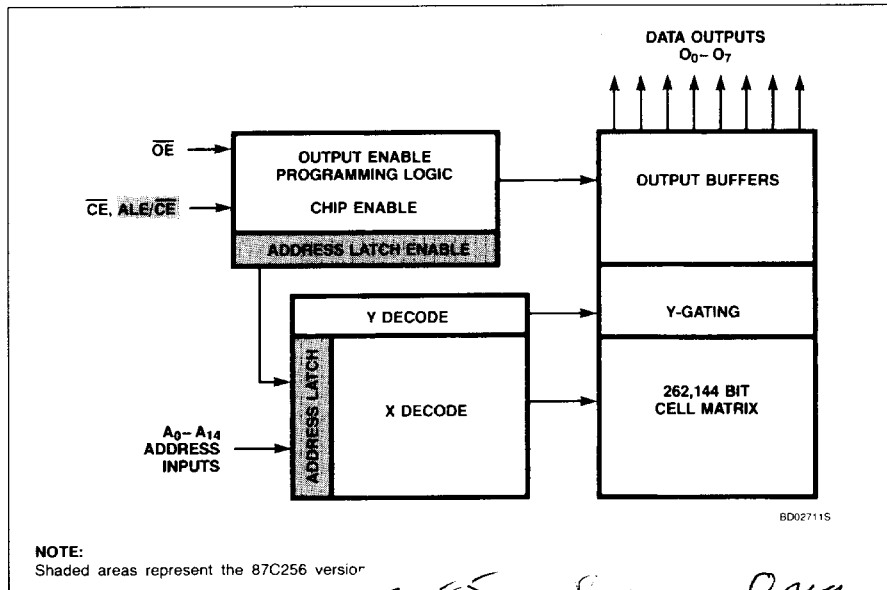


Table 1. Pin Names

A <sub>0</sub> - A <sub>14</sub>	Addresses
O <sub>0</sub> - O <sub>7</sub>	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
ALE/ $\overline{CE}$	Address latch enable/chip enable
GND	Ground
V <sub>PP</sub>	Program voltage
V <sub>CC</sub>	Power supply

