National Semiconductor

NMC27C32
32,768-Bit (4096 x 8) UV Erasable CMOS PROM

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

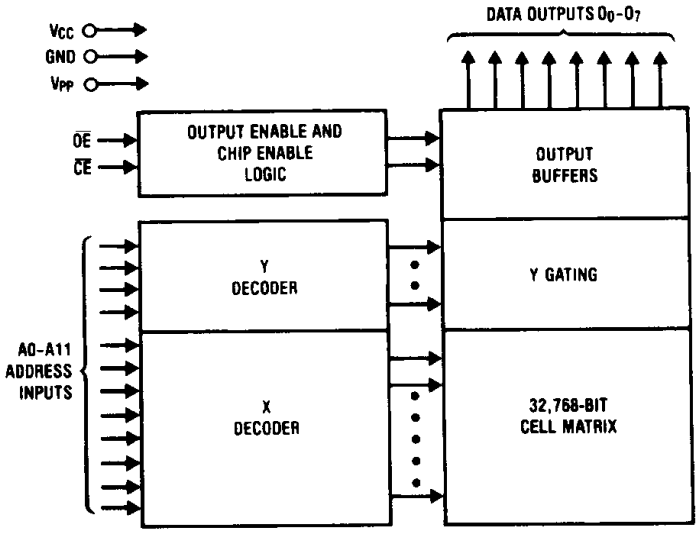
The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, p^{2}CMOS^{TM} silicon gate technology.

Features

- Access time down to 300 ns
- Low CMOS power consumption
  - Active power: 26.25 mW max
  - Standby power: 0.53 mW max (98% savings)
- Extended temperature range available (NMC27C32E-45 and NMC27C32HE-45), −40°C to +85°C, 450 ns ±5% power supply
- 10 ms programming available (NMC27C32H), an 80% time savings
- Pin compatible to NMC2732 and higher density EPROMs
- Static-no clocks required
- TTL compatible inputs/ outputs
- Two-line control
- TRI-STATE® output

Block Diagram



TL/D/5274–1

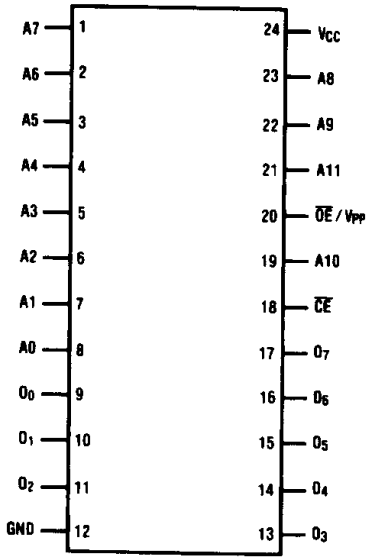
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32
Dual-In-Line Package



TL/D/5274–2

27C216 27216	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Top View

Order Number NMC27C32
See NS Package Number J24AQ

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32 pins.

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32-30, NMC27C32H-30	300
NMC27C32-35, NMC27C32H-35	350
NMC27C32-45, NMC27C32H-45	450
NMC27C32-55, NMC27C32H-55	550

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32E-45, NMC27C32EH-45	450

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground during Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C32-30, NMC27C32-35, NMC27C32-45, NMC27C32-55, NMC27C32H-30, NMC27C32H-35, NMC27C32H-45, NMC27C32H-55	0°C to +70°C
NMC27C32HE-45, NMC27C32E-45	−40°C to +85°C
V_{CC} Power Supply	5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{CC} or GND, f = 1 MHz I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32								Units
			-30, H-30		-35, H-35		-45, H-45 E-45; HE-45		-55, H-55		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300		350		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300		350		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		150		150		150		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	130	0	130	0	130	0	130	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

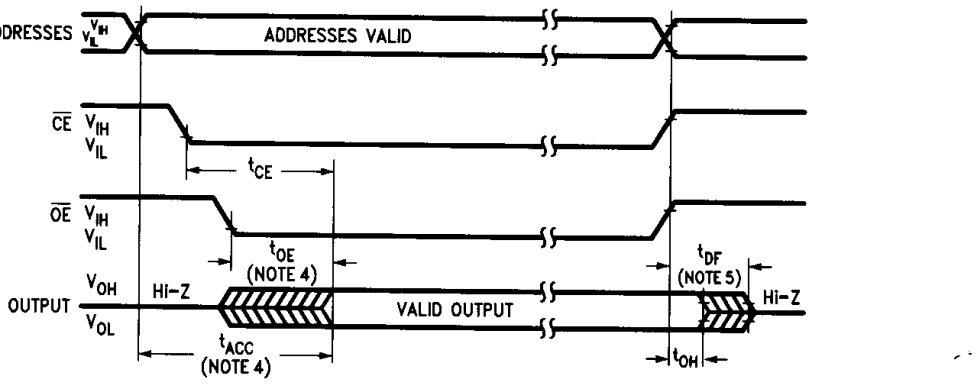
Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	V_{IN} = 0V	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF	Timing Measurement Reference Level	
		Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6 & 8)



TL/D/5274–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING (Note 1)

DC Programming Characteristics

T_A = +25°C ±5°C, V_{CC} = 5V ± 5%, V_{PP} = 25V ±1V (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{CC}$ or GND			10	μA
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 μA	2.4			V
I_{CC}	V_{CC} Supply Current			2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level (All Inputs except $\overline{OE}/V_{PP}$)		2.0		V_{CC} + 1	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA

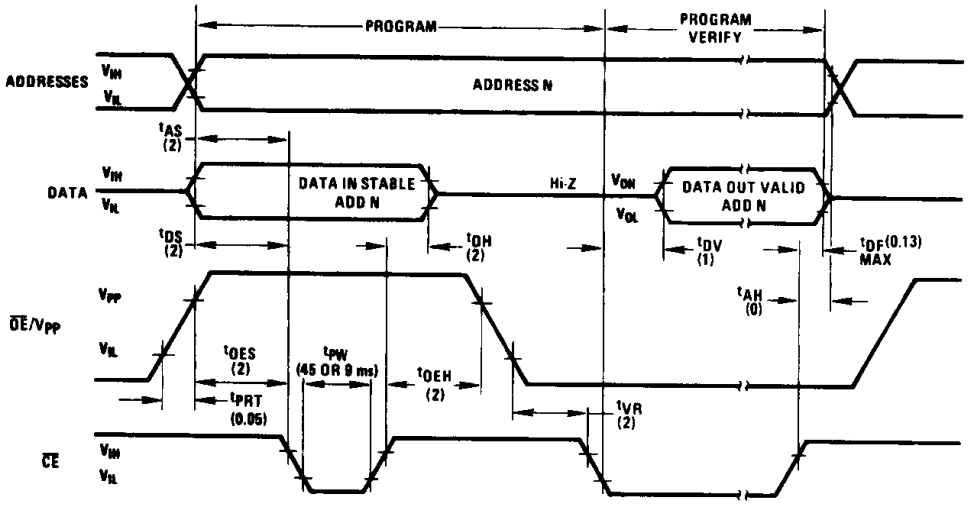
AC Programming Characteristics T_A = +25°C ±5°C, V_{CC} = 5V ± 5%, V_{PP} = 25V ±1V

Symbol	Parameter	Conditions	NMC27C32			NMC27C32H			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Setup Time		2			2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			2			μs
t_{DS}	Data Setup Time		2			2			μs
t_{AH}	Address Hold Time		0			0			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	0		130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1			1	μs
t_{PW}	$\overline{CE}$ Pulse Width during Programming		45	50	55	9	10	11	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			50			ns
t_{VR}	V_{PP} Recovery Time		2			2			μs

AC Test Conditions

V_{CC}	5V ± 5%	Timing Measurement Reference Level	
V_{PP}	25V ± 1V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



TL/D/5274–4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified..
The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must not be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description (Continued)

DEVICE OPERATION

The 6 modes of operation of the NMC27C32 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The NMC27C32 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC27C32 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C32 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the NMC27C32.

Initially, and after each erasure, all bits of the NMC27C32 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

Functional Description (Continued)

The NMC27C32 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC}, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C32H devices) active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C32H devices). The NMC27C32 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple NMC27C32s in parallel with the same data can easily be accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32s.

Program Inhibit

Programming multiple NMC27C32s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C32s may be common. A TTL level program pulse applied to an NMC27C32's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that NMC27C32. A high level $\overline{CE}$ input inhibits the other NMC27C32s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32 is exprosure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C32 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The NMC27C32-55 and NMC27C32H-55 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Output Disable	Don't Care	V_{IH}	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z