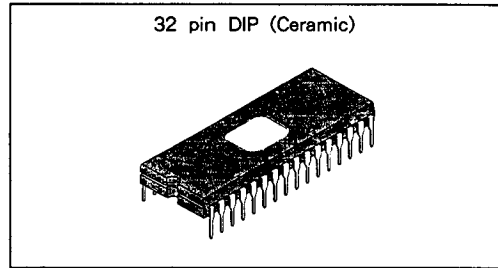


131072-word × 8-bit Ultraviolet Erasable CMOS PROM

Description

The CXK27C1000DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit micro-processor systems requiring large program memories, this IC is organized as 131072-word by 8-bit in a 32 pin Frit-Seal package.

This IC has features of pin compatibility with 1M bit mask ROM.



Features

- Fast access time: (Access time)
 CXK27C1000DQ-15 150ns (Max.)
 CXK27C1000DQ-20 200ns (Max.)
- Low current consumption
 at operation current 50mA (Max.)
 at standby 1mA (Max.)
- At read out 5V single supply operation: 5V ± 10 %
- Directory TTL compatible: All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 32 pin ceramic DIP package

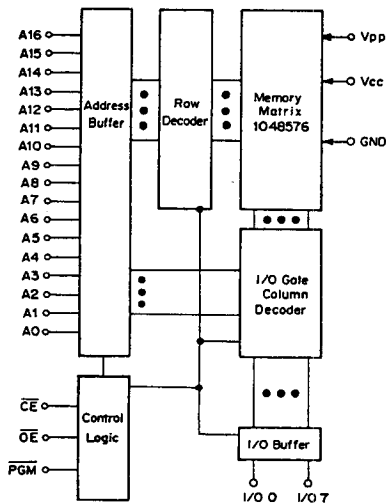
Function

131072-word × 8-bit EPROM

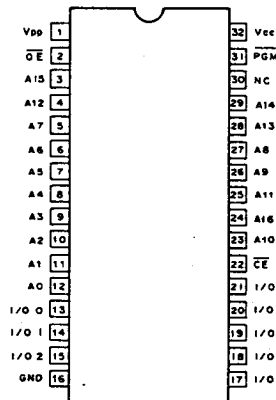
Structure

Silicon Stacked-gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O0 to I/O7	Data I/O
CE	Chip enable input
OE	Output enable input
PGM	Program enable input
Vpp	Program power supply
Vcc	+ 5V power supply
GND	GND
NC	No connection

Absolute Maximum Ratings (Ta = 25 °C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.6 to + 7.0	V
	V _{PP}	- 0.6 to + 14	V
Input voltage	A ₉	- 0.6 to + 13.5	V
	V _{IN}	- 0.6 to + 6.5	V
Output voltage	V _{I/O}	- 0.6 to + 6.5	V
Operating temperature	T _{opr}	- 10 to + 80	°C
Storage temperature	T _{stg}	- 65 to + 125	°C

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

\overline{CE}	\overline{OE}	A ₉	PGM	V _{pp}	Mode	I/O pin
L	L	X	X	V _{CC}	Read	Data output
L	H	X	X	V _{CC}	Output disable	High impedance
H	X	X	X	V _{CC}	Standby	High impedance
L	X	X	L	V _{PP}	Program	Data input
L	L	X	H	V _{PP}	Program verify	Data output
H	X	X	X	V _{PP}	Program inhibit	High impedance
L	L	V _H	H	V _{CC}	Electronic signature	Device code output

Set X to either "H" or "L", V_H = 12V ± 0.5V

Read Mode**Recommended Operating Conditions**

(Ta = 0 to + 70 °C, GND = 0V, V_{pp} = V_{CC}*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	V _{CC} + 0.5	V
Input low voltage	V _{IL}	- 0.1	—	0.8	V

* V_{pp} must be applied simultaneously or after V_{CC} and removed simultaneously or before V_{CC}.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V ± 10%, V_{pp} = V_{CC}, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 5.5V	-10	—	10	μA
Output leakage current	I _{LO}	V _{I/O} = 5.5V	-10	—	10	μA
V _{CC} average operating supply current	I _{CC1}	Cycle time 125ns Duty = 100 % I _{OUT} = 0mA $\overline{CE} = \overline{OE} = V_{IL}$	—	—	50	mA
V _{CC} standby supply current	I _{SB}	$\overline{CE} = V_{IH}$	—	—	1	mA
V _{pp} supply current	I _{pp1}		—	—	0.1	mA
Output high voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	12	pF

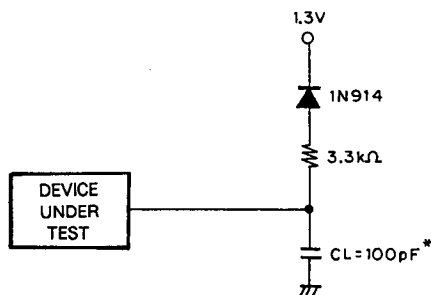
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10%, V_{pp} = V_{CC}, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	t _r ≤ 20ns
Input fall time	t _f ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load condition	Right figure

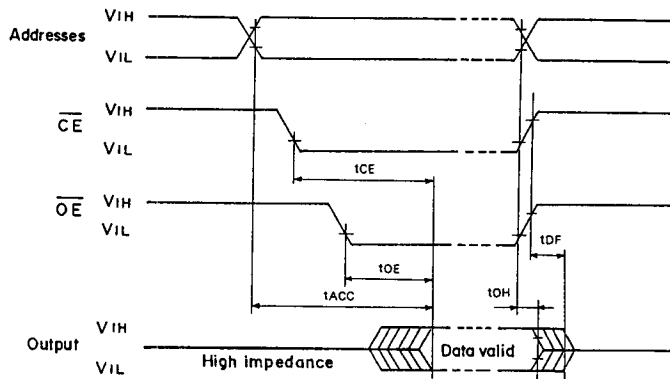


* CL includes scope and jig capacitances.

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t _{ACC}	—	150	—	200	ns
Chip enable access time	t _{CE}	—	150	—	200	ns
Output enable access time	t _{OE}	—	65	—	70	ns
Output data hold time	t _{OH}	0	—	0	—	ns
Output disable time	t _{DF} *	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation**Recommended Operating Conditions**

(Ta = 25 ± 5 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	Vcc*1	6.00	6.25	6.50	V
Vpp program supply voltage	Vpp*2	12.50	12.75	13.00	V
Input high voltage	V _{IH}	2.0		Vcc + 0.5V	V
Input low voltage	V _{IL}	- 0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.

*2 Keep Vpp below 14V including overshoot.

Extraction of the device while 12.75V is applied to Vpp may impair reliability.

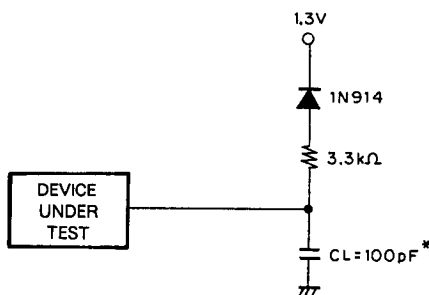
Electrical Characteristics**• DC characteristics**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = V _{IL} or V _{IH}	- 10	—	10	μA
Vcc supply current	I _{CC2}		—	—	50	mA
Vpp supply current	I _{PP2}	$\overline{CE} = V_{IL}$	—	—	50	mA
Output high voltage (at verify)	V _{OH}	I _{OH} = - 400 μA	2.4	—	—	V
Output low voltage (at verify)	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V
A9 electronic signature	V _{ID}		11.5	12.0	12.5	V

AC Characteristics**• AC test conditions**

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to + 30 °C)

Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load conditions	Right figure

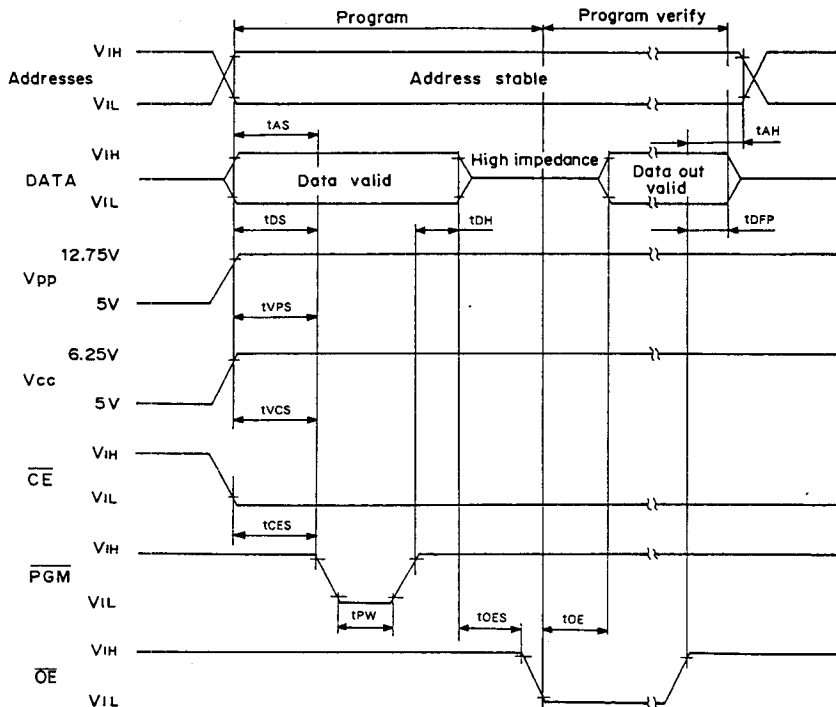


* CL includes scope and jig capacitances.

Item	Symbol	Min.	Max.	Unit
Address setup time	t _{AS}	2		μs
\overline{OE} setup time	t _{oES}	2		μs
Data setup time	t _{DS}	2		μs
Address hold time	t _{AH}	0		μs
Data hold time	t _{DH}	2		μs
\overline{OE} high to output float delay	t _{DFP} *	0	130	ns
V _{pp} setup time	t _{VPS}	2		μs
V _{cc} setup time	t _{VCS}	2		μs
\overline{CE} setup time	t _{CES}	2		μs
Program pulse width	t _{PW}	95	105	μs
Data valid from \overline{OE}	t _{OE}		100	ns

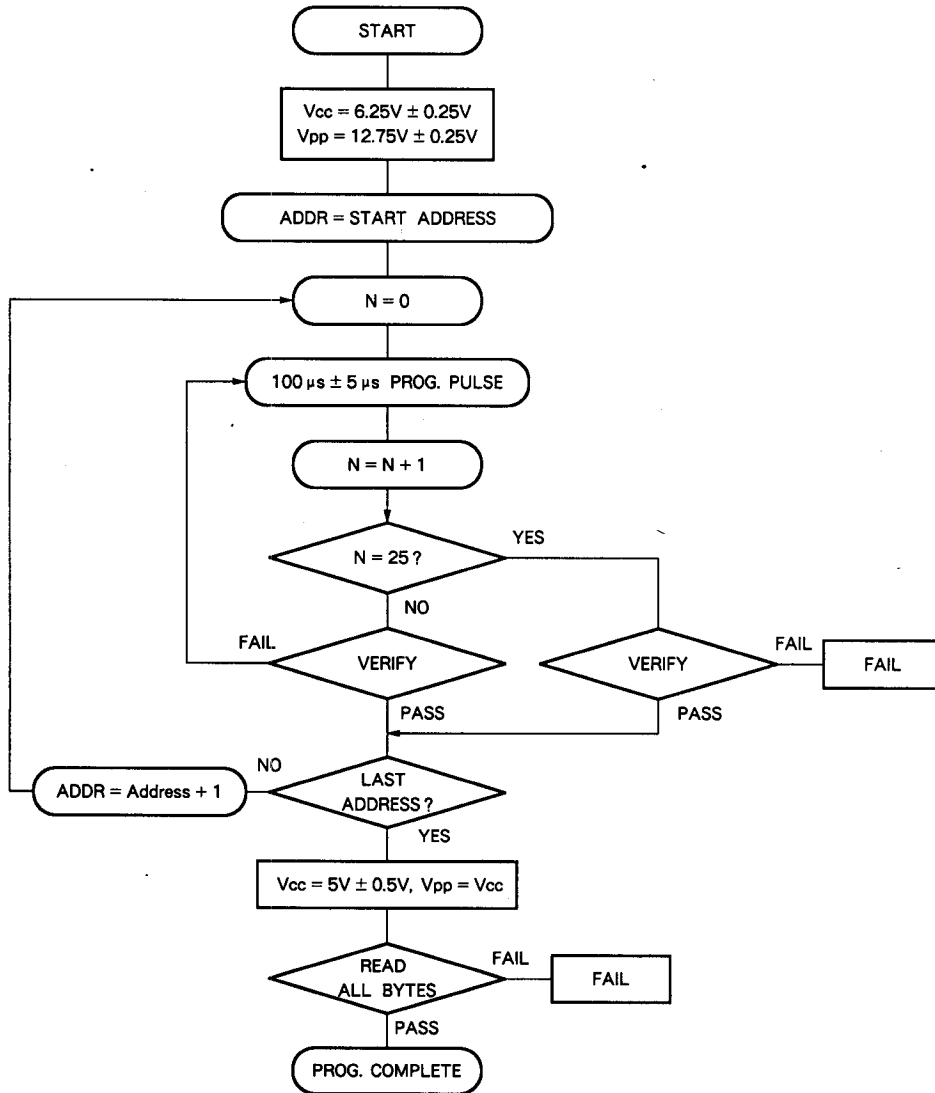
* t_{DFP} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Program)



Note) When programming the CXK27C1000DQ a 0.1 μF capacitor is required access V_{pp} and GND to suppress switching noise caused by V_{pp} transient current.

High Speed Programming Method Flow Chart
Flowchart



Erasure Operation

The recommended erasure procedure for the CXK27C1000DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity X exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 μW/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Operation Modes**Read Mode**

This IC features a chip enable (\overline{CE}) and an output enable (\overline{OE}). \overline{CE} selects the device and at the same time controls the power down function. \overline{OE} controls the output buffer, independently from \overline{CE} . By setting the address while $\overline{CE} = \overline{OE} = V_{IL}$, data becomes stable after t_{acc} .

After address has become stable, respective data become stable when after t_{ce} , \overline{CE} is lowered to V_{IL} from V_{IH} in $\overline{OE} = V_{IL}$ condition, or \overline{OE} is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{oe} .

Output Disable Mode

By turning \overline{OE} to V_{IH} , the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning \overline{CE} to V_{IH} automatically brings in power down condition. Then consumption current I_{cc} is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of \overline{CE} .

Notes on Operation

Supply current I_{cc} features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 μF ceramic capacitor between V_{cc} and GND on every device, and as close to the device as possible.

In addition, a 4.7 μF electrolytic capacitor is recommended for every 8 devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C1000DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C1000DQ is set to programming mode when 12.75V is applied to Vpp pin and "L" level to CE and PGM.

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 13 seconds.

Program Inhibit Mode

By turning Vpp to 12.75V and \overline{CE} to V_{IH} , programming is inhibited. Using this method allows for programming of multiple devices in parallel with different data. With the exception of \overline{CE} wiring is common. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = \overline{OE} = V_{IL}$, and $\overline{PGM} = V_{IH}$ at Vpp = 12.75V.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

A1 to A8, A10 to A16 = $\overline{OE} = \overline{CE} = V_{IL}$ and $\overline{PGM} = V_{IH}$ is obtained.

With A0 = V_{IL} the manufacturer code is output and with A0 = V_{IH} the device code is output.

The chart below shows the Electronic Signature.

Signature \ Pins	A0	07	06	05	04	03	02	01	00	Hex
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	1	0	0	0	0	1	1	0	86

Package Outline Unit : mm

32 pin DIP (Ceramic)

