March 1993
Edition 1.0

FUJITSU

DATA SHEET

MBM27C4096-12-X/-15-X
CMOS 4M-BIT UV EPROM

CMOS 4,194,304-BIT UV ERASABLE READ ONLY MEMORY

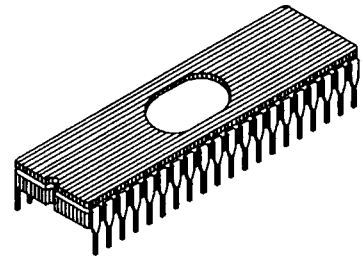
The Fujitsu MBM27C4096 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable bits organized in a 262,144-word/16-bit format. The MBM27C4096 is housed in a 40-pin DIP with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15 to 20 minutes. A new bit pattern can then be written into memory.

The MBM27C4096 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C4096 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

- 262,144-byte/16-bit organization with on-chip decoding
- One-word or Two-word programming capability with high-speed algorithms
- Static operation (no clocks required)
- Fast access time:

  MBM27C4096-12-X = 120ns (max)
  MBM27C4096-15-X = 150ns (max)
- Easy and simple memory expansion via @ pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (±10%) power supply with low current drain:

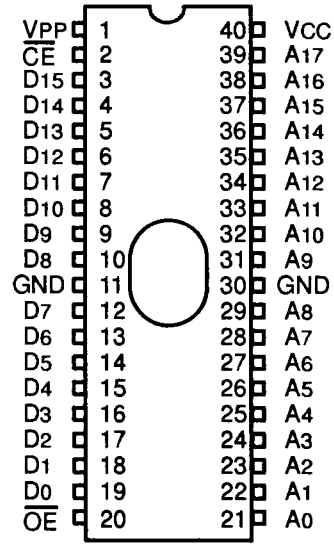
  Active operation = 50mA (max)
  Standby operation = 1.0mA (max)-TTL Level
  Standby operation = 100µA (max)-CMOS Level
- Fast Programming: 0.1ms pulse
- Programming voltage: +12.5V
- JEDEC approved 40-pin Ceramic DIP(Suffix: Z)



CERAMIC PACKAGE
DIP-40C-C04

PIN ASSIGNMENT

(TOP VIEW)



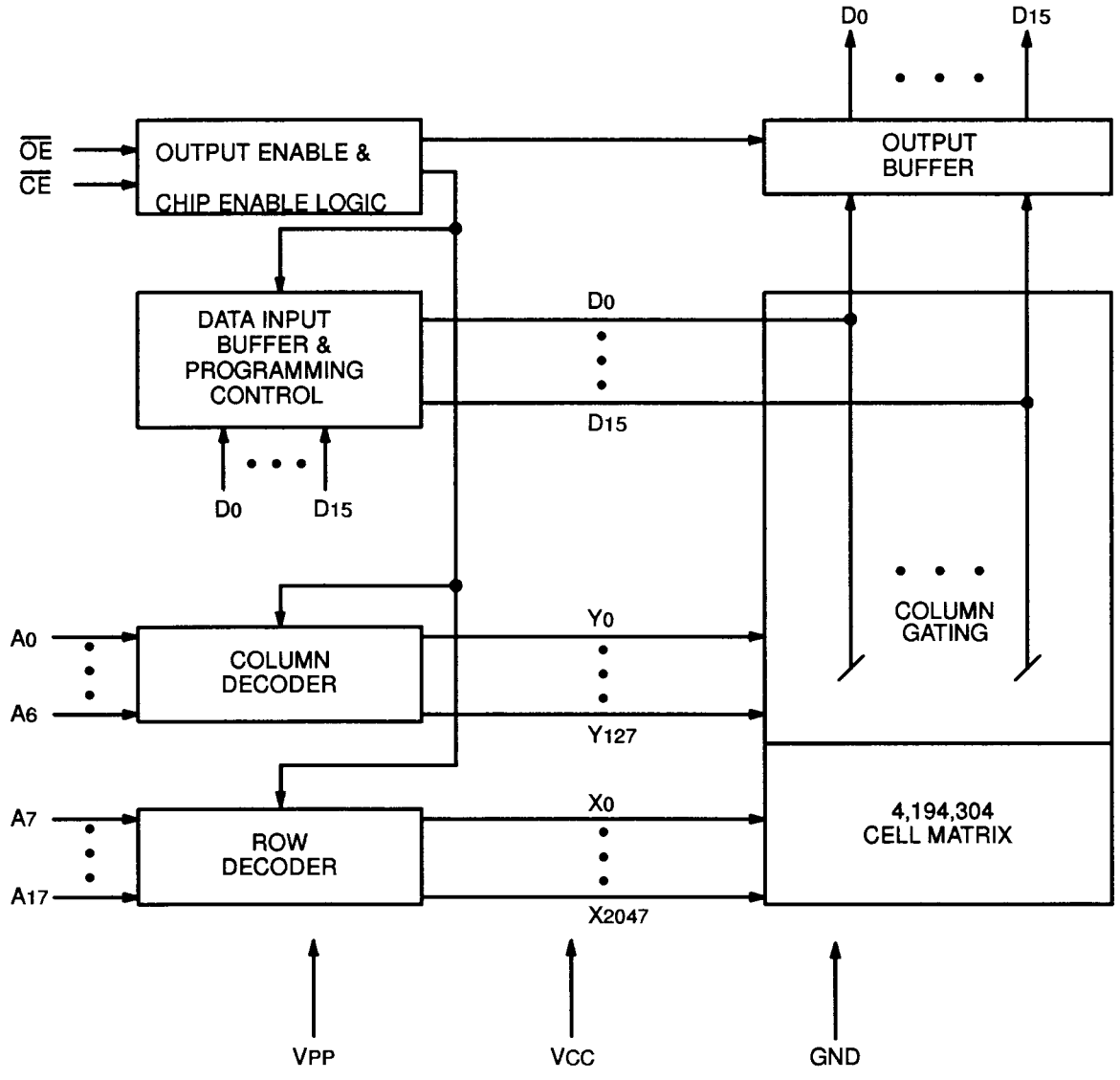
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	-0.6 to +7.0	V
Programming Voltage with respect to ground	V_{PP}	-0.6 to +14.0	V
Input/Output Voltage (except for A9 with respect to ground)	V_{IN1}, V_{OUT}	-0.6 to V_{CC} +0.6	V
Programming Voltage with respect to ground	V_{IN2}	-0.6 to +13.5	V
Temperature under Bias	T_{BIAS}	-50 to +95	°C
Storage Temperature Range	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 — BLOCK DIAGRAM



CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN}=0V)	C_{IN}		10	13	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}		6	9	pF

PIN DESCRIPTION

Symbol	Pin No.	Function
V_{PP}	1	+5V power supply. When +12.5V is applied, the device is enabled for programming operation.
$\overline{CE}$	2	Chip enable. When active Low, the device is enabled for data read and programming operations.
D_0 to D_{15}	3 to 10, 12 to 19	Three-state output data lines
GND	11, 30	Circuit ground
$\overline{OE}$	20	Output enable. When active Low, all output lines are enabled.
A_0 to A_{17}	21 to 29, 31 to 39	Address lines
V_{CC}	40	+5V power supply

FUNCTIONS AND PIN CONNECTIONS

1. Read Mode

Mode \ Symbol	A_0 to A_{17}	D_0 to D_7	$\overline{OE}$	$\overline{CE}$	V_{CC}	V_{PP}	GND
Standby	X	Hi-Z	X	V_{IH}	+5V	+5V	GND
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	+5V	GND
Output Disable	A_{IN}	Hi-Z	V_{IH}	V_{IL}	+5V	+5V	GND
Electronic Signature	A_0	CODE	V_{IL}	V_{IL}	+5V	+5V	GND

Legend: X="H" or "L"

2. One-Word Programming Mode

Mode \ Symbol	A_0 to A_{17}	D_0 to D_7	$\overline{OE}$	$\overline{CE}$	V_{CC}	V_{PP}	GND
Data Latch	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program	A_{IN}	Hi-Z	V_{IH}	V_{IL}	+6V	+12.5V	GND
Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+6V	+12.5V	GND
Program Inhibit	X	Hi-Z	V_{IH}	V_{IH}	+6V	+12.5V	GND

Legend: X='H" or "L"

3. Two-Word Programming Mode

Mode \ Symbol	A0	A1 to A17	D0 to D15	$\overline{OE}$	$\overline{CE}$	VCC	VPP	GND
Data Latch	AIN	AIN	DIN	VIL	VIH	+6V	+12.5V	GND
Program	X	AIN	Hi-Z	VIH	VIL	+6V	+12.5V	GND
Verify	AIN	AIN	DOUT	VIL	VIL	+6V	+12.5V	GND
Program Inhibit	X	X	Hi-Z	VIH	VIH	+6V	+12.5V	GND

Legend: X="H" or "L"

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage *1	VPP	VCC −0.6	VCC	VCC +0.6	V
Input High Level	VIH	2.0		VCC +0.3	V
Input Low Level	VIL	−0.3		0.8	V
Operating Temperature	TA	−40		85	°C

*1 : VPP supply voltage is applied posterior to or coincident with VCC supply voltage and cut off prior to or coincident with VCC supply voltage.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	VIN = VCC = 5.5V			10	µA
Output Leakage Current	$\|I_{LO}\|$	VOUT = VCC = 5.5V			10	µA
VCC Standby Current	ISB1	$\overline{CE}$ = VIH			1.0	mA
VCC Standby Current	ISB2	$\overline{CE}$ = VCC ±0.3V			100	µA
VCC Operation Current	ICC	Cycle = min., IOUT = 0mA			50	mA
VPP Supply Current	IPP	VPP = VCC ±0.6V			100	µA
Output High Level	VOH1	IOH = −400µA	2.4			V
Output High Level	VOH2	IOH = −100µA	VCC −0.7			V
Output Low Level	VOL	IOL = 2.1mA			0.45	V

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

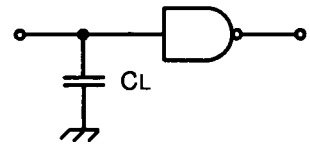
Parameter	Symbol	MBM27C4096-12-X Values		MBM27C4096-15-X Values		Unit
		Min	Max	Min	Max	
Address Access Time	tACC		120		150	ns
$\overline{CE}$ to Output Delay Time	tCE		120		150	ns
$\overline{OE}$ to Output Delay Time	tOE		70		70	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	tDF		60		60	ns
Address to Output Hold Time	tOH	0		0		ns
$\overline{CE}$ or $\overline{OE}$ to Output Active	tDV	0		0		ns

NOTE: Output Float is defined as the point where data is no longer driven.

AC TEST CONDITIONS

Fig. 2 —AC TEST CONDITIONS(INCLUDING PROGRAMMING)

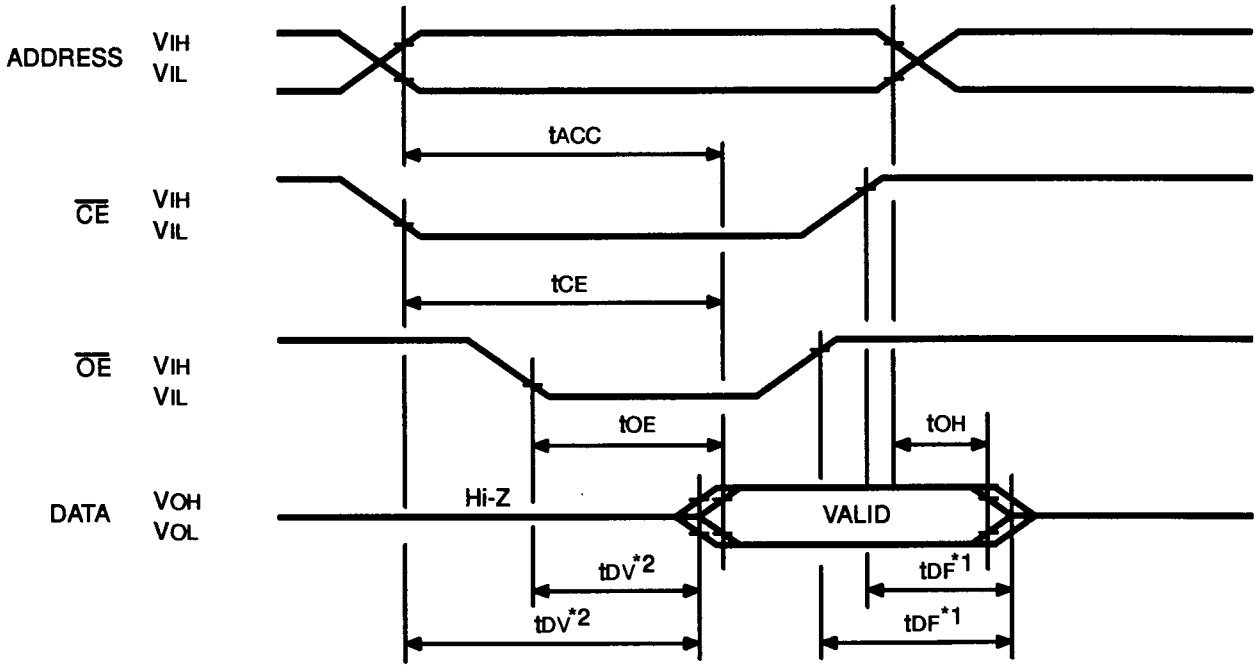
Input Pulse Levels:	0.45V to 2.4V
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L = 100pF



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ WAVEFORM



NOTE: *1: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to high earlier.
*2: t_{DV} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to low later.

PROGRAMMING / ERASING INFORMATION

PROGRAMMING

One-word Programming. When +12.5V(±0.3) volts are applied to Vpp, +6(±0.25) volts are to VCC and $\overline{CE}$, $\overline{OE}$ =VIH (TTL) , theprogramming mode is initiated. Address is selected for programmingby address pins A0 to A17 and input data is applied to output pins D0 to D15. When both address and data are stable, a 0.1-millisecond negative pulse is applied to the $\overline{OE}$ pin. Upon verification of written data should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Two-word Programming. Compared to the One-word programming , the Two-word programming method reduces programming time by about 75%. Voltages applied to VPP and VCC are the same as in the One-word programming; however some logic levels differ (refer to "Two-word Programming" in the truth table). In conjunction with $\overline{OE}$ pin, address pins A0 is used to latch Two-word of data. When both address and data are stable, a 0.1-millisecond negative pulse is applied to the $\overline{OE}$ pin. Upon verification of written data should be applied to complete the programming of Two-word.

Caution

In program mode (VPP=12.5V(±0.3)), a continue us TTL low-level Voltage should not be applied to the $\overline{CE}$. Also a 0.1-microfarad capacitor must be connected between VPP and ground to prevent excessive voltage transient. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When MBM27C4096 is shipped from the factory, all memory cells (4,194,304 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

Manufacturer and device codes are electronically stored in each device. The Electronic Signature Code List is shown in the table preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C4096 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 10Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C4096 with a non-abrasive cleaner. Hold the MBM27C4096 approximately one inch from the light source for 15 to 20 minutes. (Note. The MBM27C4096 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	A0	A1 to A8	A9	A10 to A17	$\overline{OE}$	$\overline{CE}$	D0	D1	D2	D3	D4	D5	D6	D7	D8 to D15	HEX
Manufacture	VIL	VIL	12(±0.5)V	VIL	VIL	VIL	0	0	1	0	0	0	0	0	0	#04
Device	VIH	VIL	12(±0.5)V	VIL	VIL	VIL	1	0	1	0	1	1	1	0	0	#75

PROGRAMMING / ERASING INFORMATION (Cont'd)

DC CHARACTERISTICS

(T_A= 25 °C ± 5°C, V_{CC} *1 = 6V ± 0.25V, V_{PP} *2 = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 6.25V/0V			10	µA
V_{PP} Supply Current (One-word)	I_{PP1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			30	mA
V_{PP} Supply Current (Two-word)	I_{PP2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			50	mA
V_{PP} Supply Current (Inhibit)	I_{PP3}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}			5	mA
V_{PP} Supply Current (Verify)	I_{PP4}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}			5	mA
V_{CC} Supply Current	I_{CC}				50	mA
Input Low Level	V_{IL}		-0.1		0.8	V
Input High Level	V_{IH}		2.0		V_{CC} +0.3	V
Output Low Level	V_{OL}	I_{OL} = 2.1mA			0.45	V
Output High Level	V_{OH}	I_{OH} = -400µA	2.4			V

NOTE : *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
*2 V_{PP} must not be 13.5volts or more including overshoot. Permanent device damage may occuer if the device is taken out or put into socket remaining V_{PP}=12.5 volts. Also, during $\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC CHARACTERISTICS

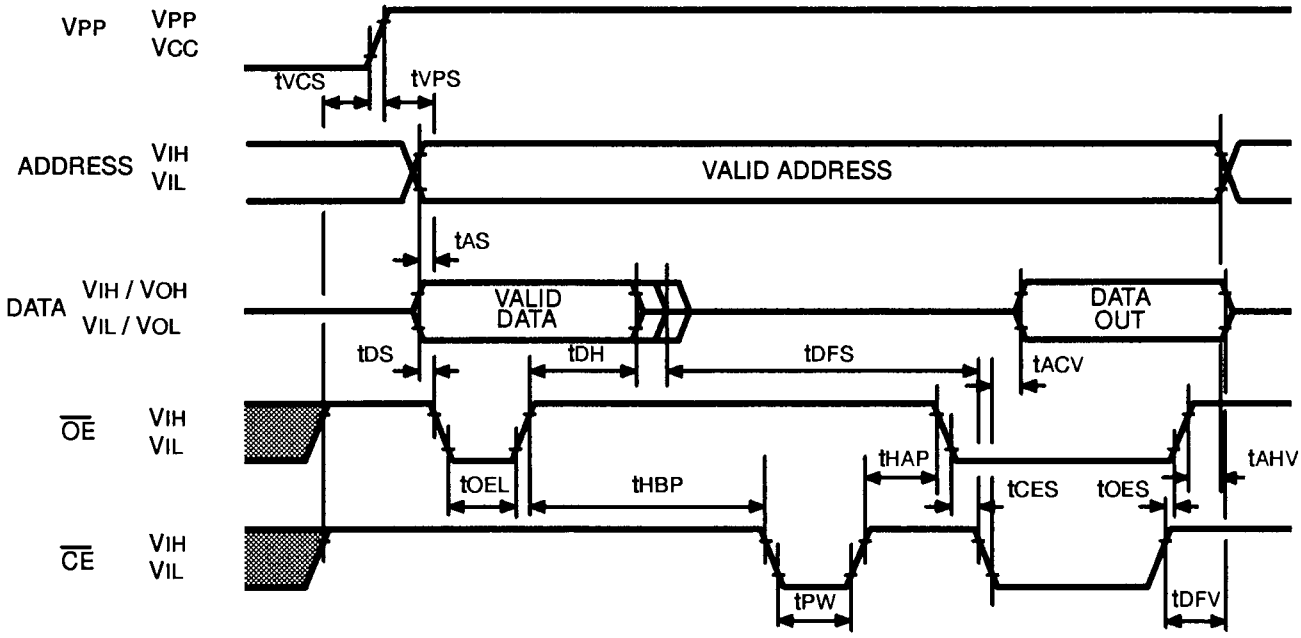
(T_A= 25 °C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	0.5			µs
Address Hold Time	t_{AH}	0.5			µs
Data Setup Time	t_{DS}	0.5			µs
Data Hold Time	t_{DH}	0.5			µs
$\overline{OE}$ Hold Time("L")	t_{OEL}	0.5			µs
$\overline{OE}$ Hold Time("H")	t_{OEH}	0.5			µs
Hold Time Before Programming	t_{HBP}	2			µs
Programming Pulse Width	t_{PW}	95	100	105	µs
Over Programming Pulse Number	N	1		50	times

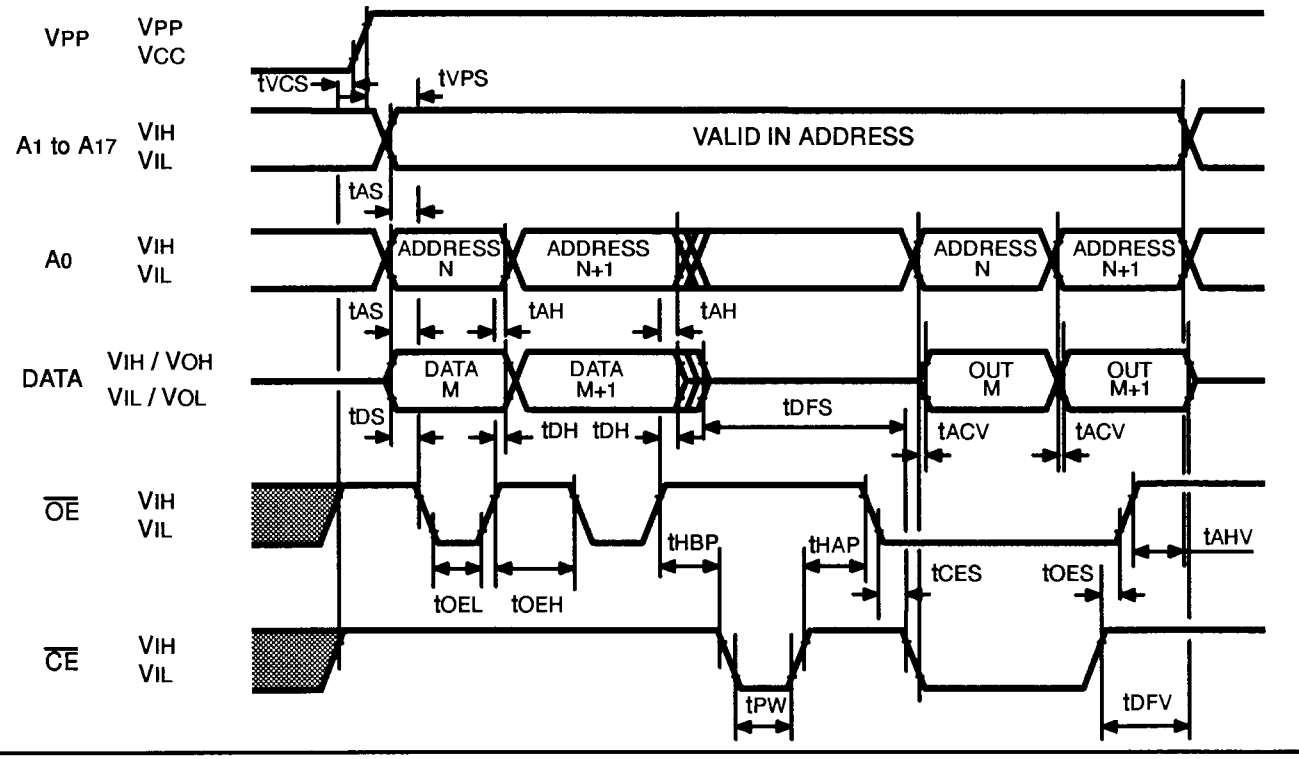
AC CHARACTERISTICS(Cont'd)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Hold Time After Programming	tHAP	2			µs
$\overline{CE}$ Setup Time	tCES	2			µs
$\overline{OE}$ Setup Time	tOES	2			µs
Input Data Floating Setup Time	tDFS	1			µs
Address Access Time at Verify	tACV			500	ns
$\overline{OE}$ to Output Float	tDFV			150	ns
Hold Time After Verify	tAHV	0			µs
V_{PP} Setup Time	tVPS	20			µs
V_{PP} Hold Time	tVCS	20			µs

PROGRAMMING WAVEFORM (ONE-WORD) Note 1



PROGRAMMING WAVEFORM (TWO-WORD) Note 1

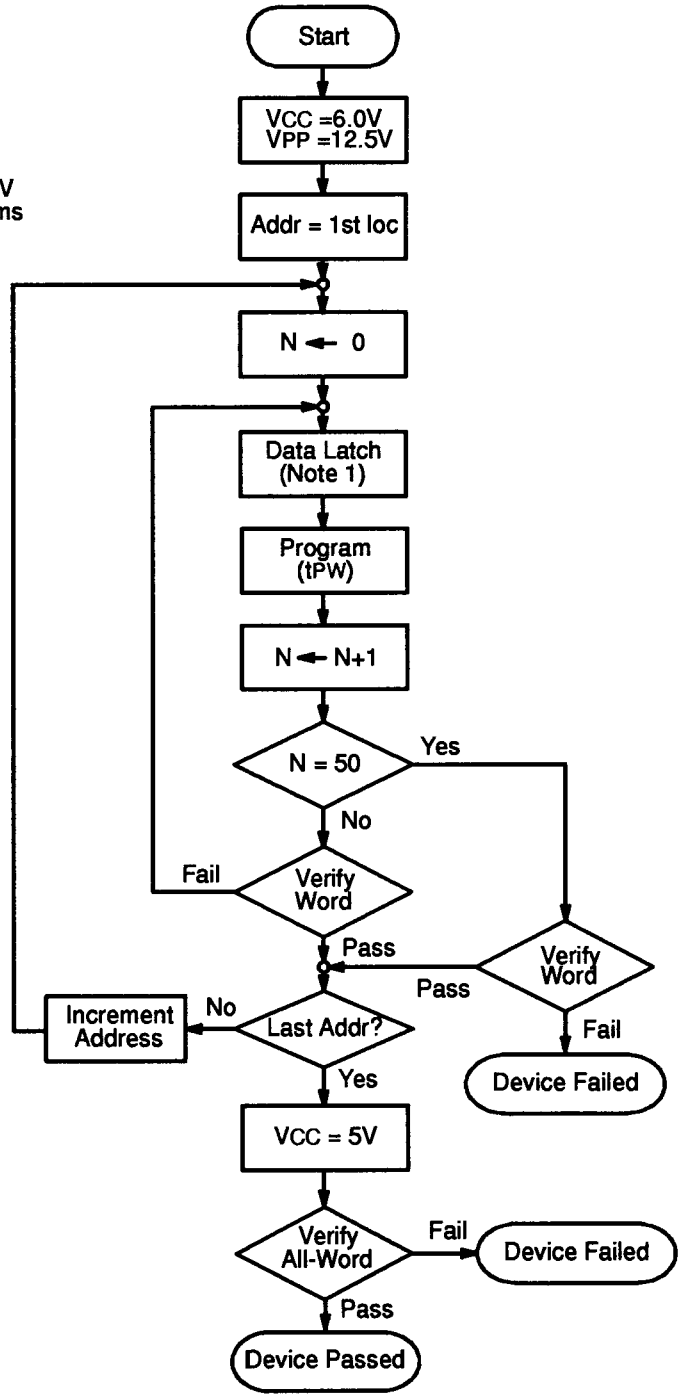


Note 1: When verify fails, return to data latch.

PROGRAMMING / ERASING INFORMATION

PROGRAMMING FLOWCHART

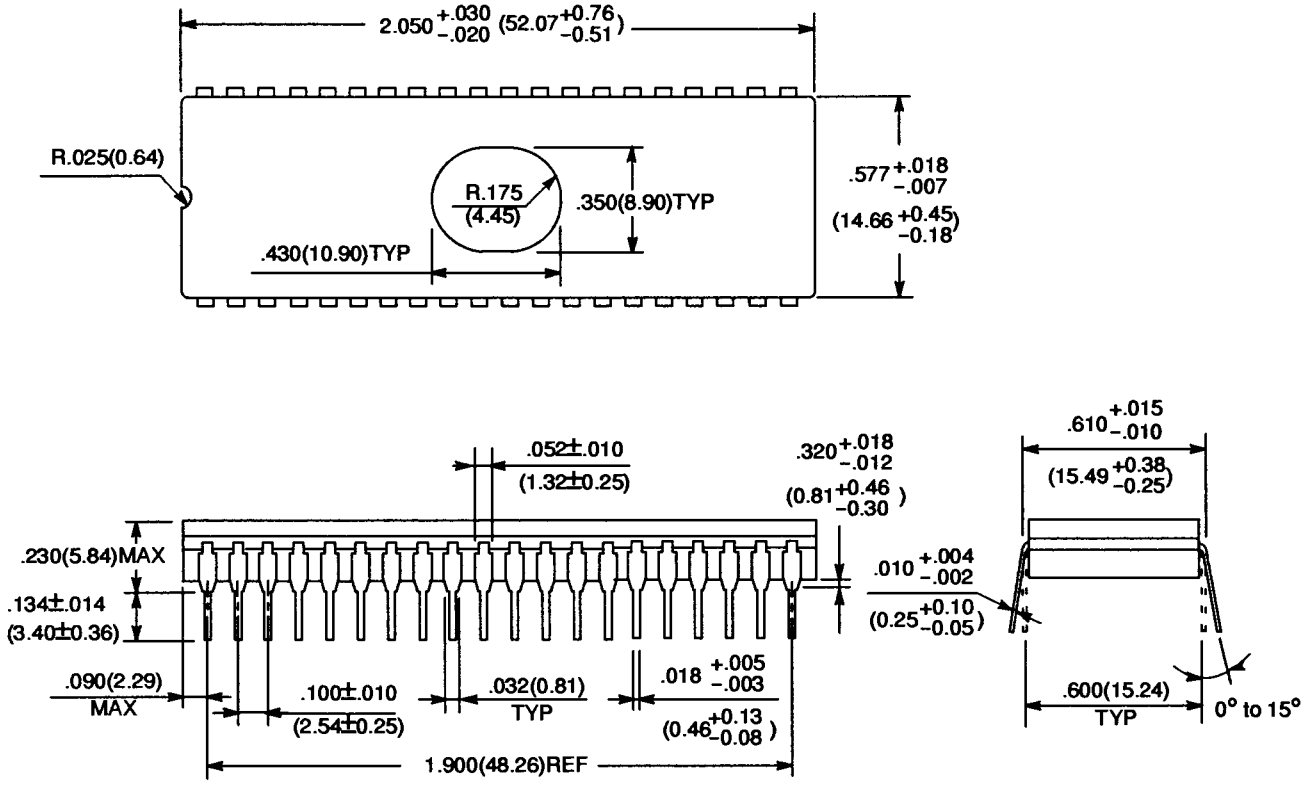
Note 1 :
1. 1-word or 2-word
2. Conditions:
   VCC = 6(±0.25)V
   VPP = 12.5(±0.3)V
   tPW = 0.1±0.005ms



PACKAGE DIMENSIONS

(Suffix: Z)

40-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40C-C04)



Dimensions in inches (millimeters)