HN27C512 Series

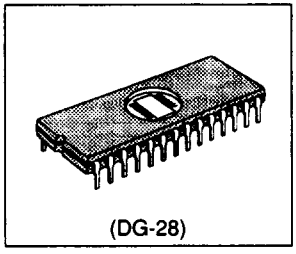
512K (64K x 8-bit) UV EPROM

■ DESCRIPTION

The Hitachi HN27C512 is a 512-Kilobit Ultraviolet Erasable and Electrically Programmable Read Only Memory organized as 65,536 x 8-bits.

The HN27C512 features fast address access times and low power dissipation. This combination makes the HN27C512 suitable for high speed microcomputer systems. The HN27C512 also offers high speed programming.

Hitachi's HN27C512 is offered with the JEDEC-Standard Byte-Wide EPROM pinout in a 28-pin Ceramic package.



(DG-28)

■ FEATURES

- Fast Access Times:
  170 ns/200 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mA (typ)
  Standby Mode: 250 µA (max)
- High Speed Programming
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
- Package:
  28-pin Ceramic DIP

■ ORDERING INFORMATION

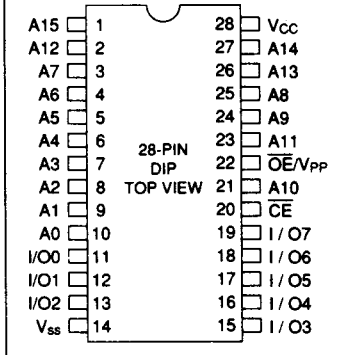
Type No.	Access Time	Package
HN27C512G-17	170 ns	28-pin Ceramic DIP
HN27C512G-20	200 ns	(DG-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{15}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

■ PIN ARRANGEMENT

HN27C512G Series



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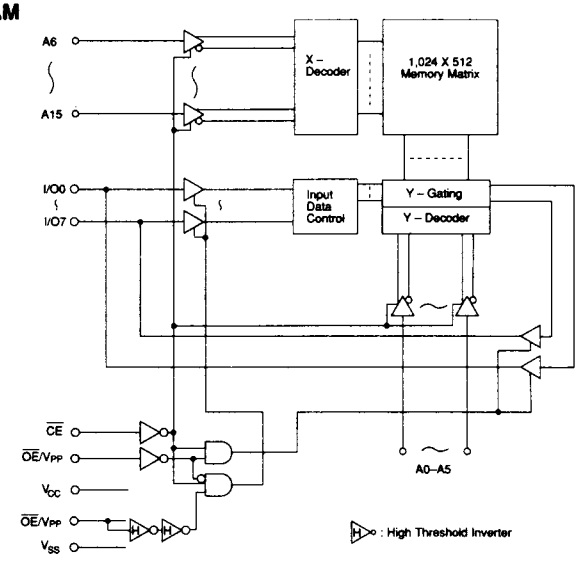
■ BLOCK DIAGRAM



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■ MODE SELECTION

Mode	V_{CC}	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	I/O
Read	V_{CC}	V_{IL}	V_{IL}	X [1]	D_{OUT}
Output Disable	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{IH}	X	X	High-Z
Program	V_{CC}	V_{IL}	V_{PP}	X	D_{IN}
Program Verify	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{CC}	V_{IH}	V_{PP}	X	High-Z
Identifier	V_{CC}	V_{IL}	V_{IL}	V_H [2]	ID

Notes: 1. X = Don't Care.
2. $11.5\ V \leq V_H \leq 12.5\ V$

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 Input Voltage	V_{ID}	-0.6 to +13.5	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	6	10	pF	V_{IN} = 0V, all pins except $\overline{OE}/V_{PP}$
Output Capacitance	C_{OUT}	8	14	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	35	50	mA	f = 6 MHz, $\overline{CE}$ = $\overline{OE}$ = V_{IL}
Standby V_{CC} Current	I_{SB}	-	-	500	mA	$\overline{CE}$ = V_{IH}
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.1 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 1.0 mA
	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

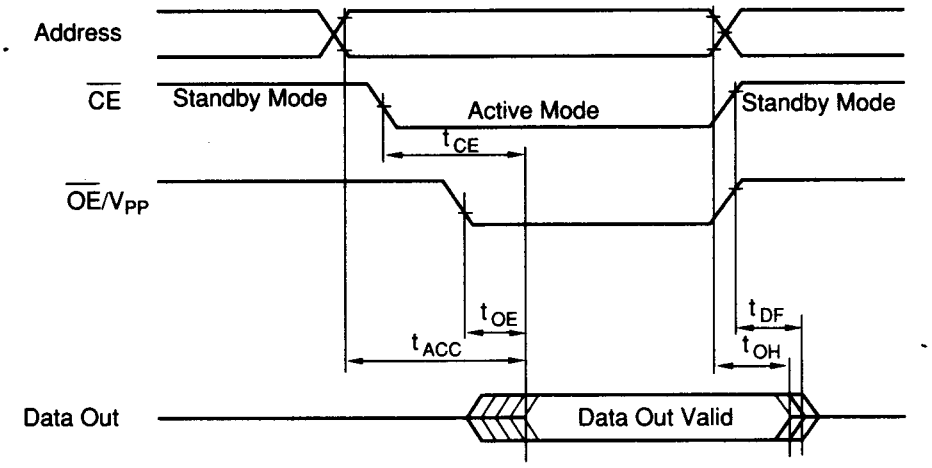
(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.4 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0 V

Item	Symbol	-17		-20		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	170	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	170	-	200	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	75	-	75	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	60	0	60	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address	t_{OH}	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

■ READ TIMING WAVEFORM



(TD.R.HN27C512)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	35	50	mA	$\overline{CE}$ = V_{IL}
Input Voltage [1]	V_{IH}	2.2	-	V_{CC} +.5 [2]	V	
	V_{IL}	- 0.1[1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.4	V	I_{OH} = 2.1 mA

Notes: 1. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
2. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

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■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

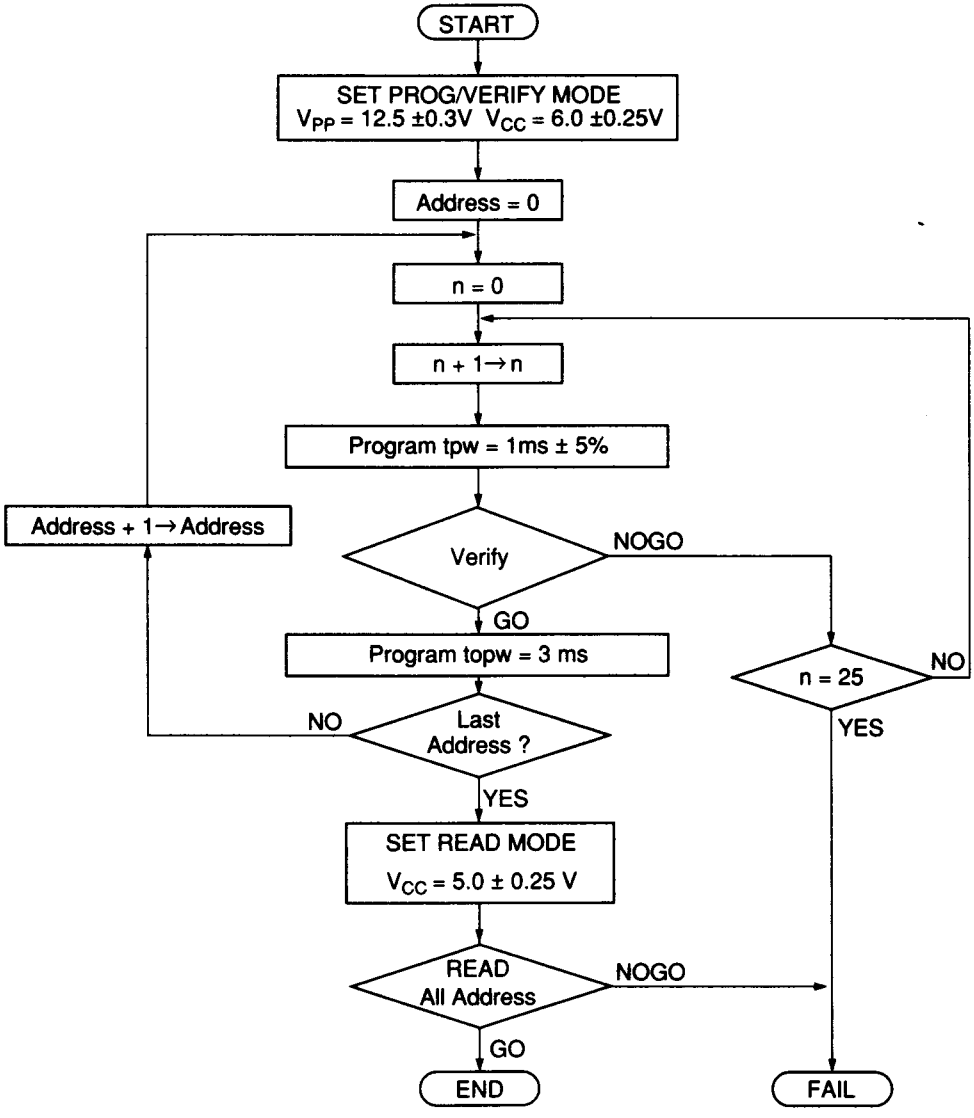
- Input pulse levels: 0.4 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}	2.85	-	78.75	ms	
Data Hold Time	t_{DH}	2	-	-	µs	
V_{PP} Rise Time	t_R	50	-	-	ns	
V_{PP} Recovery Time	t_{VR}	2	-	-	µs	
Data Valid from Chip Enable	t_{DV}	-	-	1	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ HIGH PERFORMANCE PROGRAMMING FLOWCHART

The Hitachi HN27C512 can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



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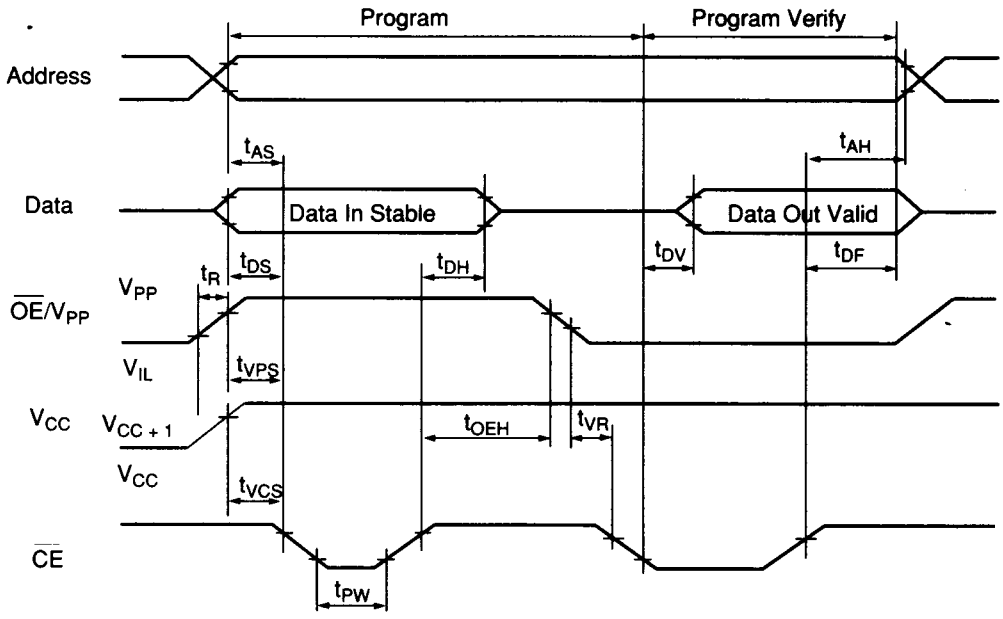
■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM



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■ ERASING THE HN27C512

The Hitachi HN27C512 Ceramic DIP package allows the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm².

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN27C512 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{15}, $\overline{CE}$, $\overline{OE} = V_{IL}$