



27256

256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
 - 4 Second Programming
 - intelligent Programming™ Algorithm Compatible
- **Fast Access Time**
 - 170 ns D27256-1
 - 200 ns P27256-2
- **intelligent Identifier™ Mode**
- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package**
(See Packaging Spec, Order # 231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the intelligent Identifier and rapidly program it using a superior programming method. The intelligent Programming Algorithm may be utilized in the absence of such equipment.

The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.

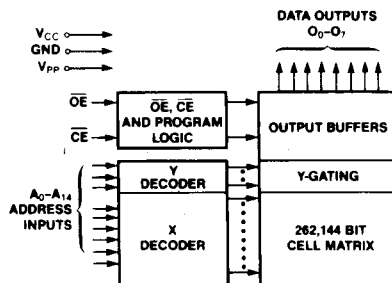
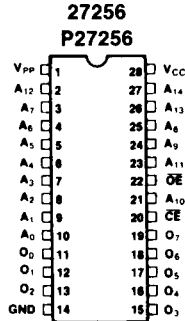


Figure 1. Block Diagram

Pin Names

| | |
|---------------------------------|---------------|
| A ₀ -A ₁₄ | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| O ₀ -O ₇ | Outputs |
| N.C. | No Connect |

| 27512 27C512 | 27128A 27C128 | 2764A 27C64 87C64 | 2732A | 2716 |
|-----------------|------------------|-------------------------|------------------|----------------|
| A ₁₅ | V _{PP} | V _{PP} | | |
| A ₁₂ | A ₁₂ | A ₁₂ | | |
| A ₇ | A ₇ | A ₇ | A ₇ | A ₇ |
| A ₆ | A ₆ | A ₆ | A ₆ | A ₆ |
| A ₅ | A ₅ | A ₅ | A ₅ | A ₅ |
| A ₄ | A ₄ | A ₄ | A ₄ | A ₄ |
| A ₃ | A ₃ | A ₃ | A ₃ | A ₃ |
| A ₂ | A ₂ | A ₂ | A ₂ | A ₂ |
| A ₁ | A ₁ | A ₁ | A ₁ ' | A ₁ |
| A ₀ | A ₀ | A ₀ | A ₀ | A ₀ |
| O ₀ | O ₀ | O ₀ | O ₀ | O ₀ |
| O ₁ | O ₁ | O ₁ | O ₁ | O ₁ |
| O ₂ | O ₂ | O ₂ | O ₂ | O ₂ |
| GND | GND | GND | GND | GND |



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| 2716 | 2732A | 2764A 27C64 87C64 | 27182A 27C128 | 27512 27C512 |
|-----------------|------------------------|-------------------------|------------------------|------------------------------------|
| | | V _{CC} PGM | V _{CC} PGM | V _{CC} A ₁₄ |
| V _{CC} | V _{CC} | N.C. | A ₁₃ | A ₁₃ |
| A ₈ | A ₈ | A ₈ | A ₈ | A ₈ |
| A ₉ | A ₉ | A ₉ | A ₉ | A ₉ |
| V _{PP} | A ₁₁ | A ₁₁ | A ₁₁ | A ₁₁ |
| \overline{OE} | \overline{OE}/V_{PP} | \overline{OE} | \overline{OE} | \overline{OE}/V_{PP} |
| A ₁₀ | A ₁₀ | A ₁₀ | A ₁₀ | A ₁₀ |
| \overline{CE} | \overline{CE} | \overline{CE} | \overline{CE} | \overline{CE} |
| O ₇ | O ₇ | O ₇ | O ₇ | O ₇ |
| O ₆ | O ₆ | O ₆ | O ₆ | O ₆ |
| O ₅ | O ₅ | O ₅ | O ₅ | O ₅ |
| O ₄ | O ₄ | O ₄ | O ₄ | O ₄ |
| O ₃ | O ₃ | O ₃ | O ₃ | O ₃ |

NOTE:

Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are

available with 168 ± 8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (-40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

| Type | Operating Temperature | Burn-In 125°C (hr) |
|------|-----------------------|--------------------|
| Q | 0°C to +70°C | 168 ± 8 |
| T | -40°C to +85°C | None |
| L | -40°C to +85°C | 168 ± 8 |

EXPRESS OPTIONS

27256 VERSIONS

| Packaging Options | |
|-------------------|---------|
| Speed Versions | Cerdip |
| -20 | Q, T, L |

READ OPERATION

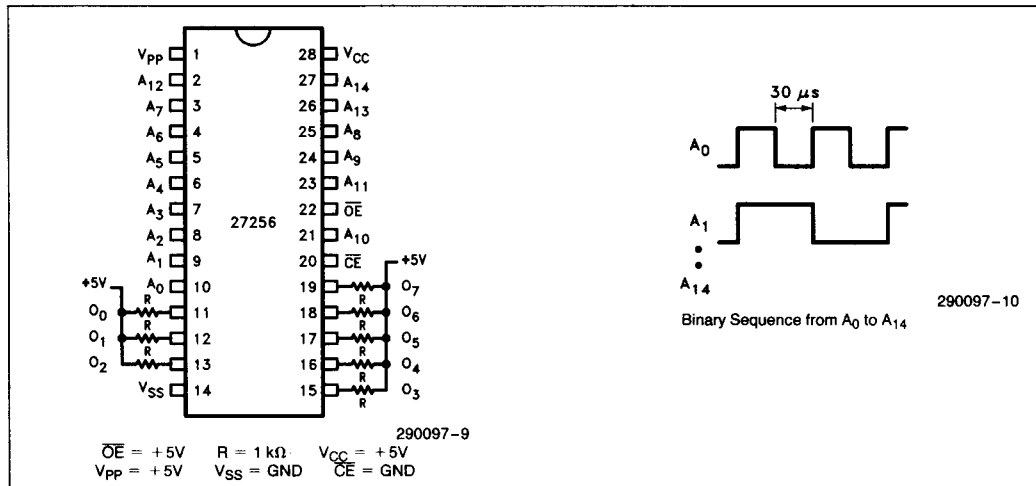
D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

| Symbol | Parameter | TD27256 LD27256 | | Test Conditions |
|-------------|-------------------------------|--------------------|-----|--|
| | | Min | Max | |
| I_{SB} | V_{CC} Standby Current (mA) | | 50 | $\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$ |
| $I_{CC(1)}$ | V_{CC} Active Current (mA) | | 125 | $\overline{OE} = \overline{CE} = V_{IL}$ |

NOTE:

1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|-----------------|
| Operating Temperature | |
| During Read | 0°C to +70°C |
| Temperature Under Bias | -10°C to +80°C |
| Storage Temperature | -65°C to +125°C |
| All Input or Output Voltages with Respect to Ground | -0.6V to +6.25V |
| Voltage on Pin 24 with Respect to Ground | -0.6V to +13.5V |
| V _{PP} Supply Voltage with Respect to Ground | -0.6V to +14.0V |
| V _{CC} Supply Voltage with Respect to Ground | -0.6V to +7.0V |

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION
D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

| Symbol | Parameter | 27256-1, 27256-2, 27256-20, P27256-2 Limits | | | 27256-25, 27256, P27256-25, P27256 Limits | | | Unit | Test Conditions |
|----------------------|--------------------------------------|---|---------|---------------------|---|---------|---------------------|------|---|
| | | Min | Typ (3) | Max | Min | Typ (3) | Max | | |
| I _{LI} | Input Load Current | | | 10 | | | 10 | μA | V _{IN} = 0V to V _{CC} |
| I _{LO} | Output Leakage Current | | | 10 | | | 10 | μA | V _{OUT} = 0V to V _{CC} |
| I _{PP1} (2) | V _{PP} Current Read/Standby | | | 5 | | | 5 | mA | V _{PP} = 5.5V |
| I _{SB} (2) | V _{CC} Current Standby | | 25 | 50 | | 20 | 40 | mA | $\overline{CE} = V_{IH}$ |
| I _{CC1} (2) | V _{CC} Current Active | | 55 | 125 | | 45 | 100 | mA | $\overline{CE} = \overline{OE} = V_{IL}$ V _{PP} = V _{CC} |
| V _{IL} | Input Low Voltage | -0.1 | | +0.8 | -0.1 | | +0.8 | V | |
| V _{IH} | Input High Voltage | 2.0 | | V _{CC} + 1 | 2.0 | | V _{CC} + 1 | V | |
| V _{OL} | Output Low Voltage | | | 0.45 | | | 0.45 | V | I _{OL} = 2.1 mA |
| V _{OH} | Output High Voltage | 2.4 | | | 2.4 | | | V | I _{OH} = -400 μA |
| V _{PP} (2) | V _{PP} Read Voltage | 3.8 | | V _{CC} | 3.8 | | V _{CC} | V | V _{CC} = 5.0V ± 0.25V |

READ OPERATION

A.C. CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

| Versions ⁽⁵⁾ | Parameter | $V_{CC} \pm 5\%$ | | 27256-1 | | 27256-2 P27256-2 | | 27256 P27256 | | Unit | Test Conditions |
|-------------------------|---|-------------------|-----|----------|-----|-----------------------|-----|-----------------|-----|------|--|
| | | $V_{CC} \pm 10\%$ | | 27256-20 | | 27256-25 P27256-25 | | | | | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Min | Max | | |
| t_{ACC} | Address to Output Delay | | 170 | | 200 | | 250 | | | ns | $\overline{CE} = \overline{OE} = V_{IL}$ |
| t_{CE} | \overline{CE} to Output Delay | | 170 | | 200 | | 250 | | | ns | $\overline{OE} = V_{IL}$ |
| t_{OE} | \overline{OE} to Output Delay | | 70 | | 75 | | 100 | | | ns | $\overline{CE} = V_{IL}$ |
| $t_{DF}^{(4)}$ | \overline{OE} High to Output Float | 0 | 35 | 0 | 55 | 0 | 60 | | | ns | $\overline{CE} = V_{IL}$ |
| $t_{OH}^{(4)}$ | Output Hold from Address, \overline{CE} or \overline{OE} Whichever Occurred First | 0 | | 0 | | 0 | | | | ns | |

NOTES:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
- V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP} . The maximum current value is with outputs O_0 to O_7 unloaded.
- Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal supply voltages.
- This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram.
- Packaging Options: No prefix = Cerdip; P = Plastic DIP.

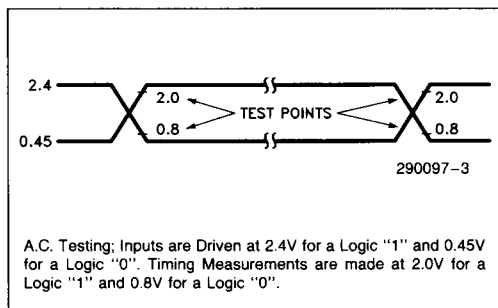
CAPACITANCE⁽²⁾ ($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

| Symbol | Parameter | Typ ⁽¹⁾ | Max | Unit | Conditions |
|-----------|--------------------|--------------------|-----|------|----------------|
| C_{IN} | Input Capacitance | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | Output Capacitance | 8 | 12 | pF | $V_{OUT} = 0V$ |

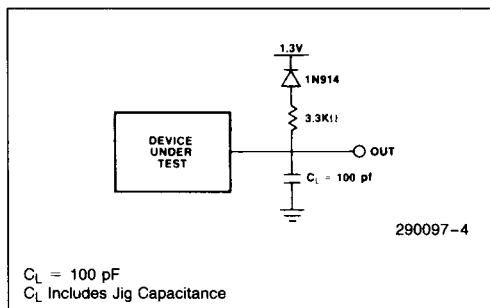
NOTES:

- $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0V$.
- This parameter is only sampled and is not 100% tested.

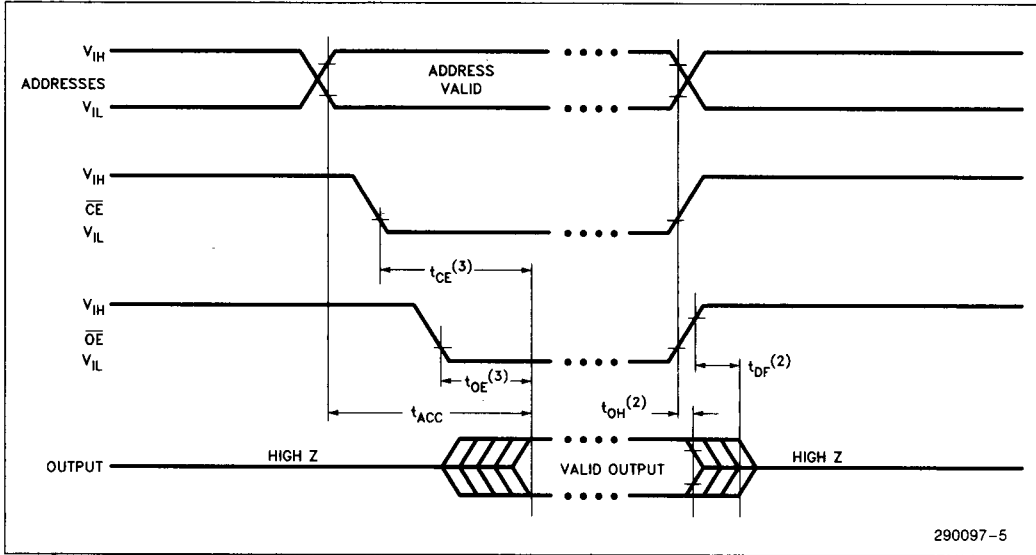
A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. WAVEFORMS



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NOTES:

1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .

Table 1. Operating Modes

| Mode | \overline{CE} | \overline{OE} | A_9 | A_0 | V_{PP} | V_{CC} | Outputs |
|---------------------------------------|-----------------|-----------------|------------------|----------|----------|----------|--------------------|
| Read | V_{IL} | V_{IL} | X ⁽¹⁾ | X | V_{CC} | 5.0V | D _{OUT} |
| Output Disable | V_{IL} | V_{IH} | X | X | V_{CC} | 5.0V | High Z |
| Standby | V_{IH} | X | X | X | V_{CC} | 5.0V | High Z |
| Programming | V_{IL} | V_{IH} | X | X | (4) | (4) | D _{IN} |
| Program Verify | V_{IH} | V_{IL} | X | X | (4) | (4) | D _{OUT} |
| Optional Program Verify | V_{IL} | V_{IL} | X | X | V_{CC} | (4) | D _{OUT} |
| Program Inhibit | V_{IH} | V_{IH} | X | X | (4) | (4) | High Z |
| intelligent Identifier ⁽³⁾ | | | | | | | 89H ⁽⁵⁾ |
| —manufacturer | V_{IL} | V_{IL} | $V_H^{(2)}$ | V_{IL} | 5.0V | 5.0V | 88H ⁽⁵⁾ |
| —device | V_{IL} | V_{IL} | $V_H^{(2)}$ | V_{IH} | 5.0V | 5.0V | 04H |

NOTES:

1. X can be V_{IH} or V_{IL} .
2. $V_H = 12.0V \pm 0.5V$.
3. $A_1 - A_8, A_{10} - A_{13} = V_{IL}, A_{14} = V_{IH}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturer's identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

DEVICE OPERATION

The modes of operation of the 27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for intelligent identifier mode.

Read Mode

The P27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

EPRoms can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

- a) the lowest possible memory power dissipation, and
- b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, \overline{CE} should be decoded and used as the primary device selecting function, while \overline{OE} should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and \overline{CE} is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level \overline{CE} input inhibits the other devices from being programmed.

Except for \overline{CE} , all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the \overline{CE} input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with \overline{OE} at V_{IL} , \overline{CE} at V_{IH} , and V_{PP} and V_{CC} at their programming voltages.

Optional Program Verify

The optional verify may be performed in place of the verify mode. It is performed with \overline{OE} at V_{IL} , \overline{CE} at V_{IL} (as opposed to the standard verify which has \overline{CE} at V_{IH}), and V_{PP} at its programming voltage. The outputs will tri-state according to the signal presented to \overline{OE} . Therefore, all devices with $V_{PP} = 12.75\text{V}$ (12.5V intelligent programming) and $\overline{OE} = V_{IL}$ will present data on the bus independent of the \overline{CE} state. When parallel programming several devices which share a common bus, V_{PP} should be lowered to V_{CC} (= 6.25/6.0V—see Table 2) and the normal read mode used to execute a program verify.

intelligent Identifier™ Mode

The intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during intelligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 \AA range. Data shows that constant expo-

sure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu\text{W}/\text{cm}^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 $\mu\text{W}/\text{cm}^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

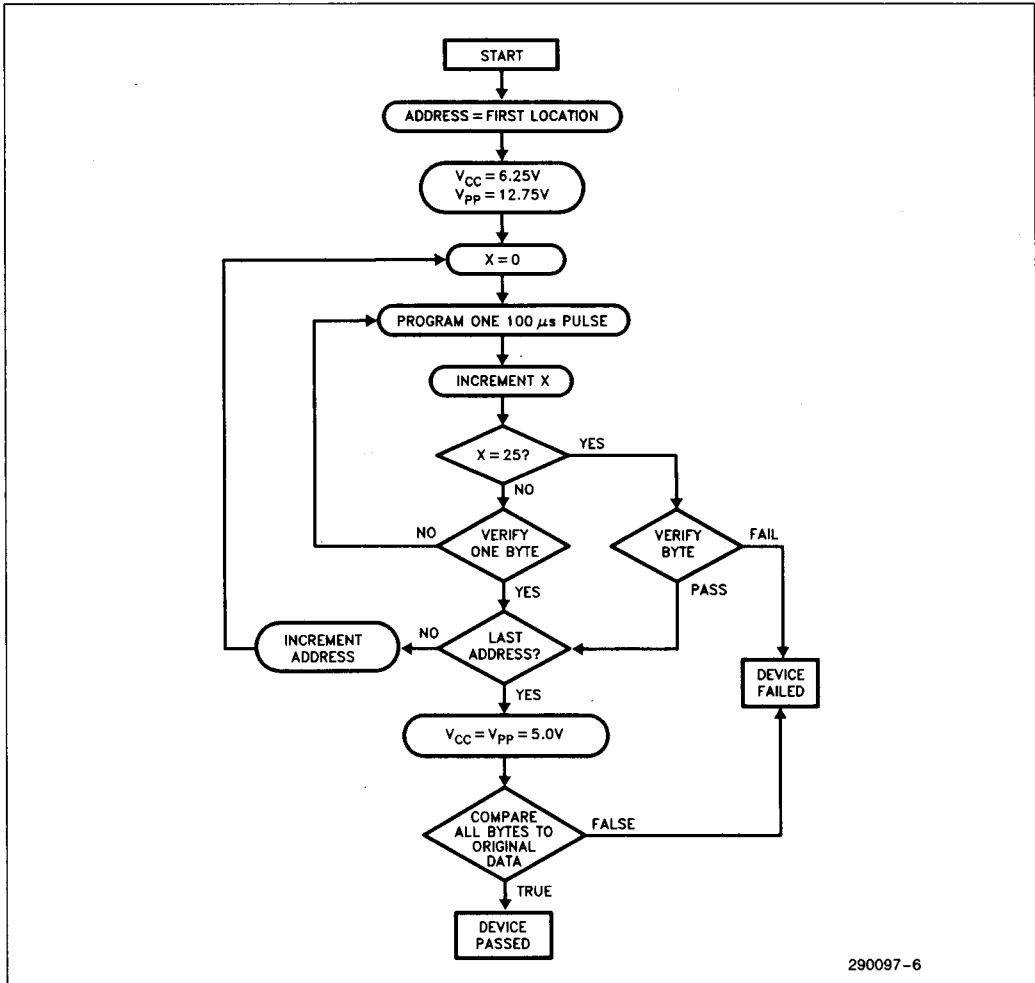


Figure 3. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic EPROMs)

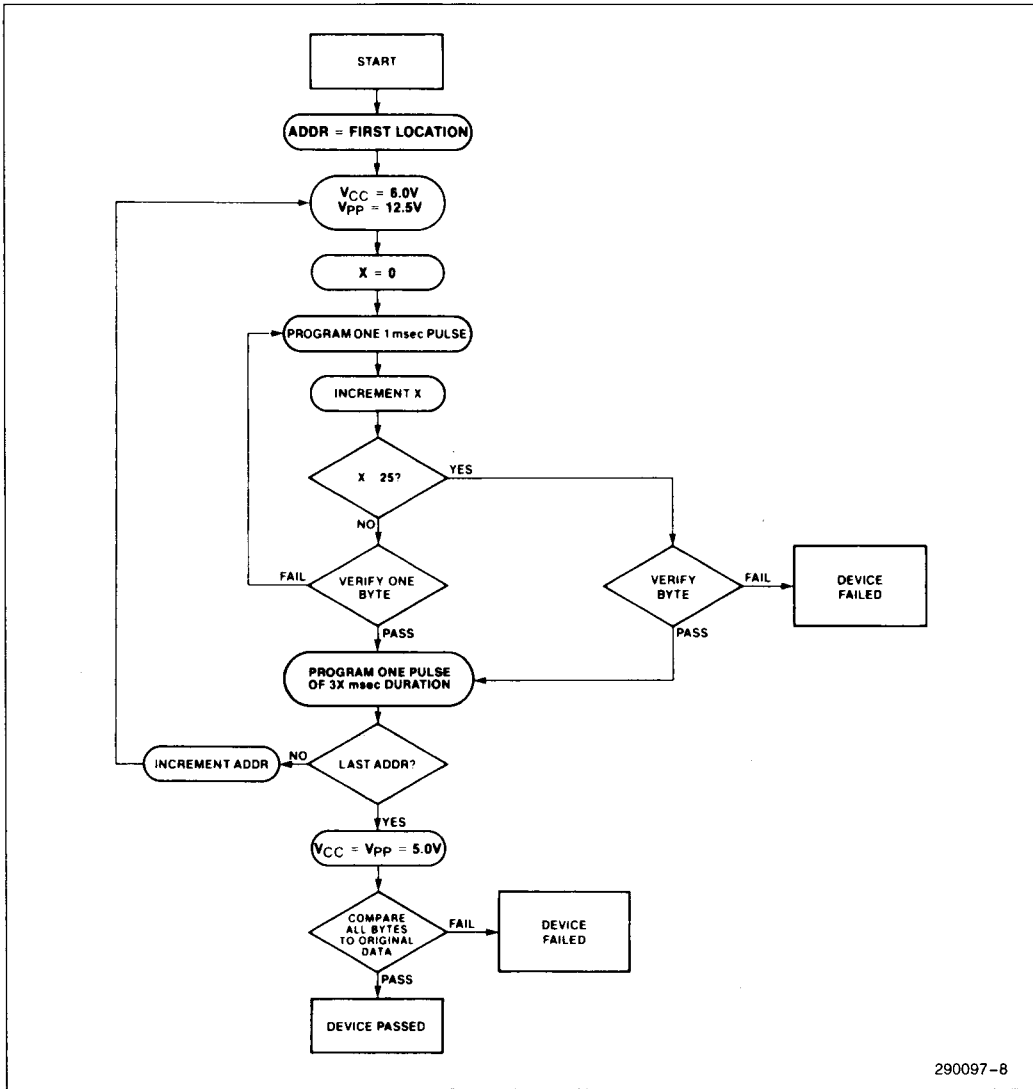
Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic devices to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has

been successfully programmed. Up to 25 100 μ s pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{CC} = 6.25V$ and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

In addition to the Quick-Pulse Programming Algorithm, Plastic EPROMs are also compatible with Intel's intelligent Programming Algorithm.



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Figure 4. intelligent Programming™ Flowchart

intelligent Programming™ Algorithm

The intelligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the intelligent Programming Algorithm is shown in Figure 4.

The intelligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial \overline{CE} pulse(s) is one millisecond, which will then be followed by a longer overprogram

pulse of length $3X$ msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $V_{pp} = 12.5V$. When the intelligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{pp} = 5.0V$.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5^\circ\text{C}$

| Symbol | Parameter | Limits | | | Test Conditions (see Note 1) |
|-----------------|--|--------|----------|---------------|---------------------------------|
| | | Min | Max | Unit | |
| I_{LI} | Input Current (All Inputs) | | 10 | μA | $V_{IN} = V_{IL}$ or V_{IH} |
| V_{IL} | Input Low Level (All Inputs) | -0.1 | 0.8 | V | |
| V_{IH} | Input High Level | 2.0 | V_{CC} | V | |
| V_{OL} | Output Low Voltage During Verify | | 0.45 | V | $I_{OL} = 2.1 \text{ mA}$ |
| V_{OH} | Output High Voltage During Verify | 2.4 | | V | $I_{OH} = -400 \mu\text{A}$ |
| $I_{CC2}^{(4)}$ | V_{CC} Supply Current (Program & Verify) | | 125 | mA | |
| $I_{PP2}^{(4)}$ | V_{PP} Supply Current (Program) | | 50 | mA | $\overline{CE} = V_{IL}$ |
| V_{ID} | A_9 intelligent Identifier Voltage | 11.5 | 12.5 | V | |
| V_{PP} | intelligent Programming Algorithm | 12.0 | 13.0 | V | $\overline{CE} = V_{IL}$ |
| | Quick-Pulse Programming Algorithm | 12.5 | 13.0 | V | $\overline{CE} = V_{IL}$ |
| V_{CC} | intelligent Programming Algorithm | 5.75 | 6.25 | V | |
| | Quick-Pulse Programming Algorithm | 6.0 | 6.5 | V | |

A.C. PROGRAMMING CHARACTERISTICS
 $T_A = 25 \pm 5^\circ\text{C}$ (see table 2 for V_{CC} and V_{PP} voltages)

| Symbol | Parameter | Limits | | | | Test Conditions* (Note 1) |
|-----------|---|--------|-----|-------|---------------|------------------------------|
| | | Min | Typ | Max | Unit | |
| t_{AS} | Address Setup Time | 2 | | | μs | |
| t_{OES} | \overline{OE} Setup Time | 2 | | | μs | |
| t_{DS} | Data Setup Time | 2 | | | μs | |
| t_{AH} | Address Hold Time | 0 | | | μs | |
| t_{DH} | Data Hold Time | 2 | | | μs | |
| t_{DFP} | \overline{OE} High to Output Data Float Delay | 0 | | 130 | μs | (Note 3) |
| t_{VPS} | V_{PP} Setup Time | 2 | | | μs | |
| t_{VCS} | V_{CC} Setup Time | 2 | | | μs | |
| t_{PW} | \overline{CE} Initial Program Pulse Width | 0.95 | 1.0 | 1.05 | ms | intelligent Programming |
| | | 95 | 100 | 105 | μs | Quick-Pulse Programming |
| t_{OPW} | \overline{CE} Overprogram Pulse Width | 2.85 | | 78.75 | ms | (Note 2) |
| t_{OE} | Data Valid from \overline{OE} | | | 150 | ns | |

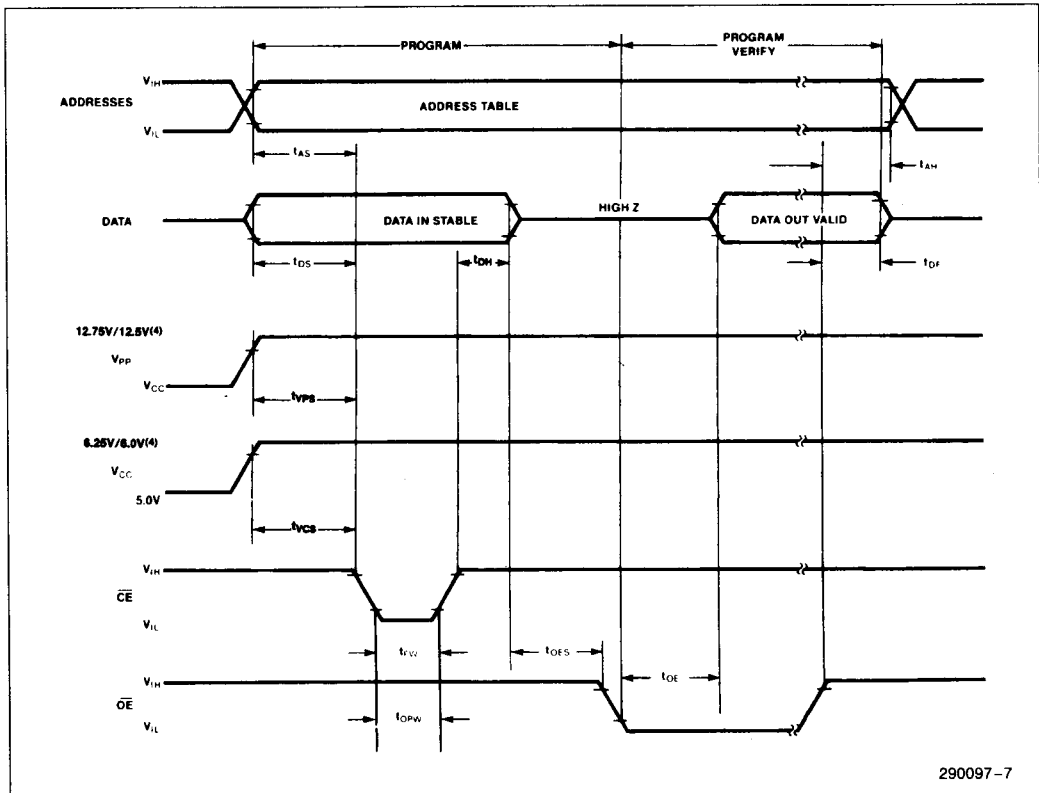
***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times
 (10% to 90%) 20 ns
 Input Pulse Levels 0.45V to 2.4V
 Input Timing Reference Level 0.8V and 2.0V
 Output Timing Reference Level 0.8V and 2.0V

NOTES:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
- The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (intelligent Programming Algorithm only).
- This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
- The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



290097-7

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NOTES:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH} .
2. t_{OE} and t_{DQ} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27256 a 0.1 μ F capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm. 12.5V V_{PP} & 6.0V V_{CC} for intelligent Programming Algorithm.

REVISION HISTORY

| Number | Description |
|--------|--|
| 04 | Revised Pin Configuration. Revised Express options. Deleted -3, -30, -5, L-2, L-20 and L-1 speed bins. D.C. Characteristics — I_{LI} Conditions are $V_{IN} = 0V$ to V_{CC} . D.C. Characteristics — I_{LO} Conditions are $V_{OUT} = 0V$ to V_{CC} . |