27C256
256K (32K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

Automotive

- **Extended Automotive Temperature Range −40°C to +125°C**
- **CHMOS/NMOS Microcontroller and Microprocessor Compatible**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current**
- **High Performance Speeds**
  - **200 ns Maximum Access Time**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **New Quick-Pulse Programming™ Algorithm**
  - **4 Second Programming**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec., Order #231369)

Intel's 27C256 CHMOS EPROM is a 256K bit 5V only memory organized as 32,768 words of 8 bits. It employs advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 27256 (HMOS II-E).

A new Quick-Pulse Programming Algorithm is employed on these devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse Compatible programming equipment, the int$_e$ligent Programming™ Algorithm may be utilized.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} + 1V.

In order to meet the rigorous environmental requirements of automotive applications, Intel offers the 27C256 in extended Automotive temperature range. Operational characteristics are guaranteed over the range of −40°C to +125°C ambient.

*HMOS and CHMOS are patented processes of Intel Corporation.

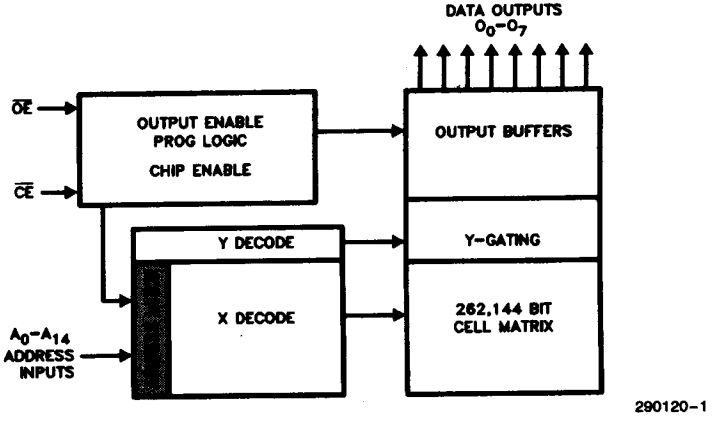


Figure 1. Block Diagram

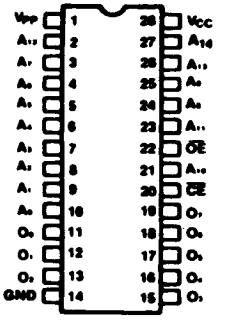
December 1987
Order Number: 290120-002

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
N.C.	NO CONNECT
D.U.	DON'T USE

27128	2764A	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

27C256



290120-2

2716	2732A	2764A	27128
		V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$
V_{CC}	V_{CC}	N.C.	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Figure 2. Pin Configuration

NOTE:
Intel "Universal Site" -Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products.

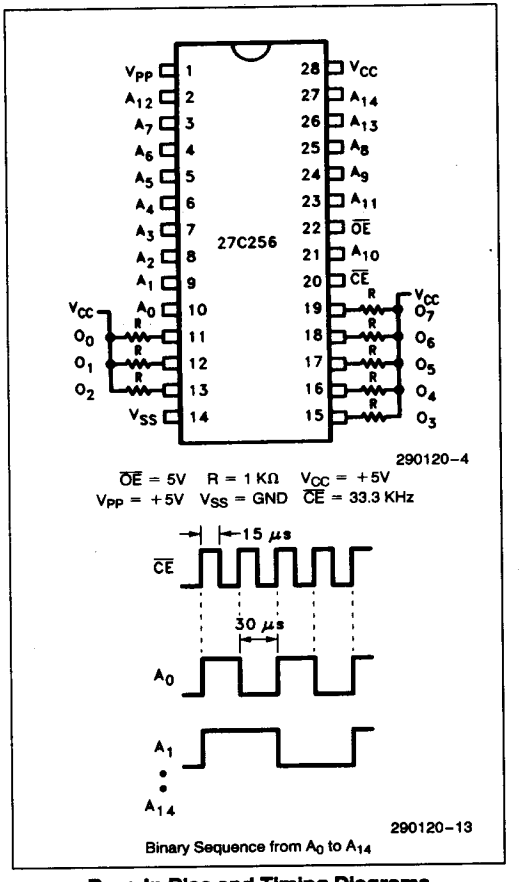
AUTOMOTIVE AND EXPRESS OPTIONS

Speed Versions	Packaging Options
	Cerdip
−2	T, L, Q, A
−20	T, L, Q, A
STD	T, L, Q, A
−25	T, L, Q, A
−3	T, L, Q, A
−30	T, L, Q, A

AUTOMOTIVE AND EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A	−40°C to +125°C	NONE
B	−40°C to +125°C	168 ±8



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... −40°C to +125°C
Temperature Under Bias ..... −40°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +13.5V(1)
V_{PP} supply Voltage with Respect to Ground during programming ..... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)
Maximum Junction Temperature (T_J) ..... 140°C

Maximum Thermal Resistance
Junction to Ambient (θ_{JA}):
Cerdip ..... 36°C/W
PLCC ..... 55°C/W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS: 27C256 $-40°C \le T_A \le +125°C$

Symbol	Parameter		Notes	Min	Typ(2)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	±1.0	µA	V_{IN} = 0V, 5.5V
I_{LO}	Output Leakage Current				0.01	±10	µA	V_{OUT} = 0V, 5.5V
I_{PP_1}	V_{PP} Read Current		4			200	µA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby	CMOS	3			200	µA	$\overline{CE} = V_{CC}$
I_{CC_1}	V_{CC} Active Current (mA)	TTL				30		$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)	TTL				30		$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = +125°C$
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		V_{CC} + 0.5	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			V_{CC} − 0.2		V_{CC} + 0.2		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		5			100	mA	
V_{PP}	V_{PP} Read Voltage		6	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C.
3. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
4. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with outputs O_0 to O_7 unloaded.
5. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
6. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
7. V_{IL}, V_{IH} levels at TTL inputs.

READ OPERATION

A.C. CHARACTERISTICS 27C256(1) $-40°C \le T_A \le +125°C$

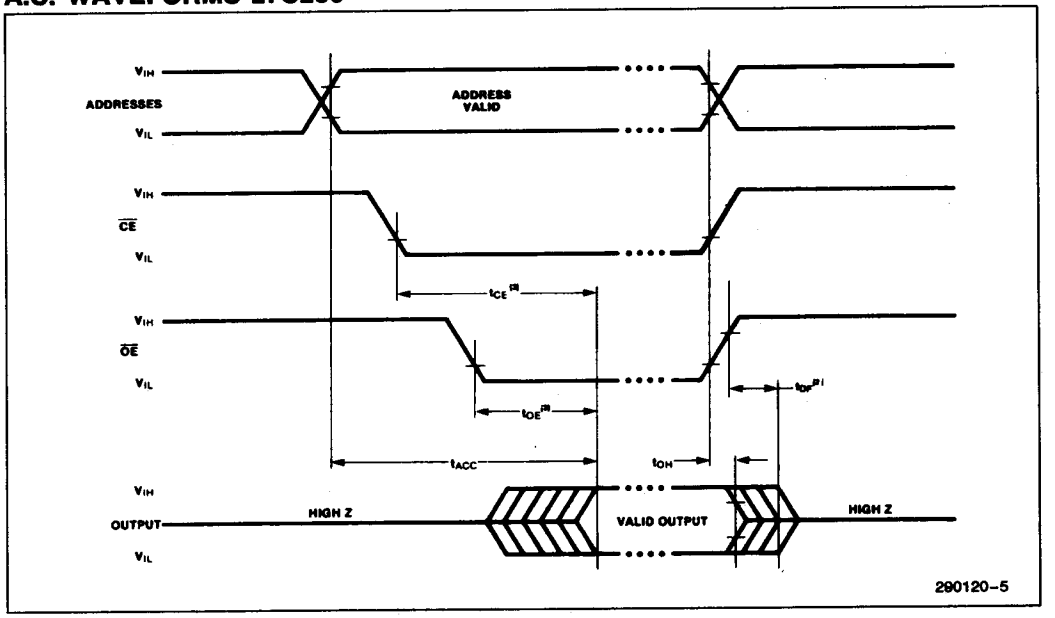
Versions(3)		$V_{CC} \pm 5\%$	27C256-2		27C256		27C256-3		Unit
		$V_{CC} \pm 10\%$	27C256-20		27C256-25		27C256-30		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay			200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay			75		100		120	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			55		60		75	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V.
Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Part Number Prefixes: No Prefix = CERDIP

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) .....10 ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V and 2.0V
Output Timing Reference Level .....0.8V and 2.4V

A.C. WAVEFORMS 27C256



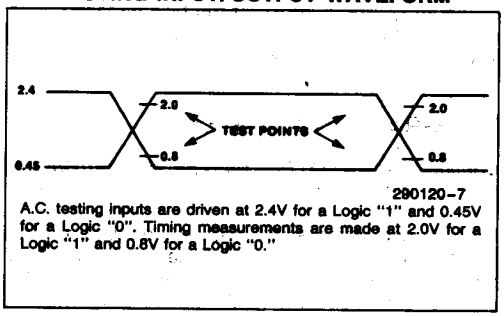
NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/control capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

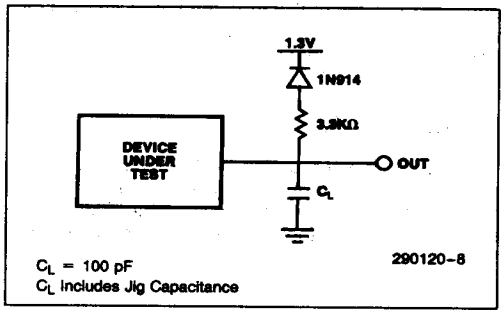
NOTE:
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier™ mode.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	HIGH Z
int$_e$ligent Identifier (3) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier (3) -27C256	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	8C H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. A_1–A_8, A_{10-12} = V_{IL}.
4. See Table 2 for V_{CC} and V_{PP} voltages during programming.

Read Mode

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The 27C256 has a Standby mode which reduces the maximum V_{CC} current to 100 μA. Both are placed in the Standby mode when $\overline{CE}$ is in the CMOS-high state. When the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus, This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ is pulsed to TTL low and $\overline{OE} = V_{IH}$. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$ and $\overline{OE}$ all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH}, and V_{PP} and V_{CC} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

Optional Program Verify

All 27C256s with V_{PP} = 12.75V (12.5V int$_e$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. The optional verify may be used in place of the verify mode to allow parallel programming where several devices share a common bus. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ = V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} = V_{CC} = 6.25V (6.0V int$_e$ligent programming). The outputs will then tri-state according to the signals presented to $\overline{OE}$ and $\overline{CE}$. With V_{PP} lowered to V_{CC} (= 6.25V/6.0V—See Table 2), the normal read mode may be used to execute a program verify.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code and byte 1 (A_0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new suport as it becomes available, with very low cost add-ons. For example, even the earliest users of the a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development Systems, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system

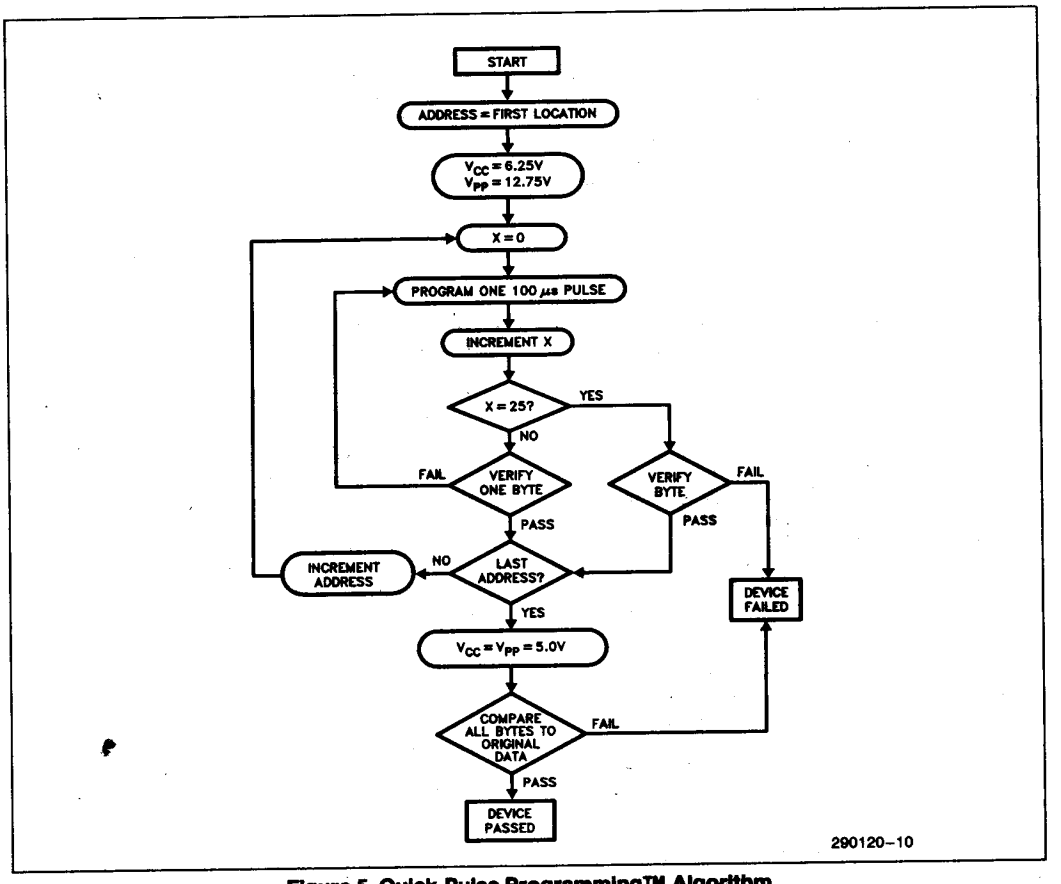


Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27C256 EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows 27C256s to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, the 27C256 is also compatible with Intel's Int$_e$ligent Programming Algorithm.

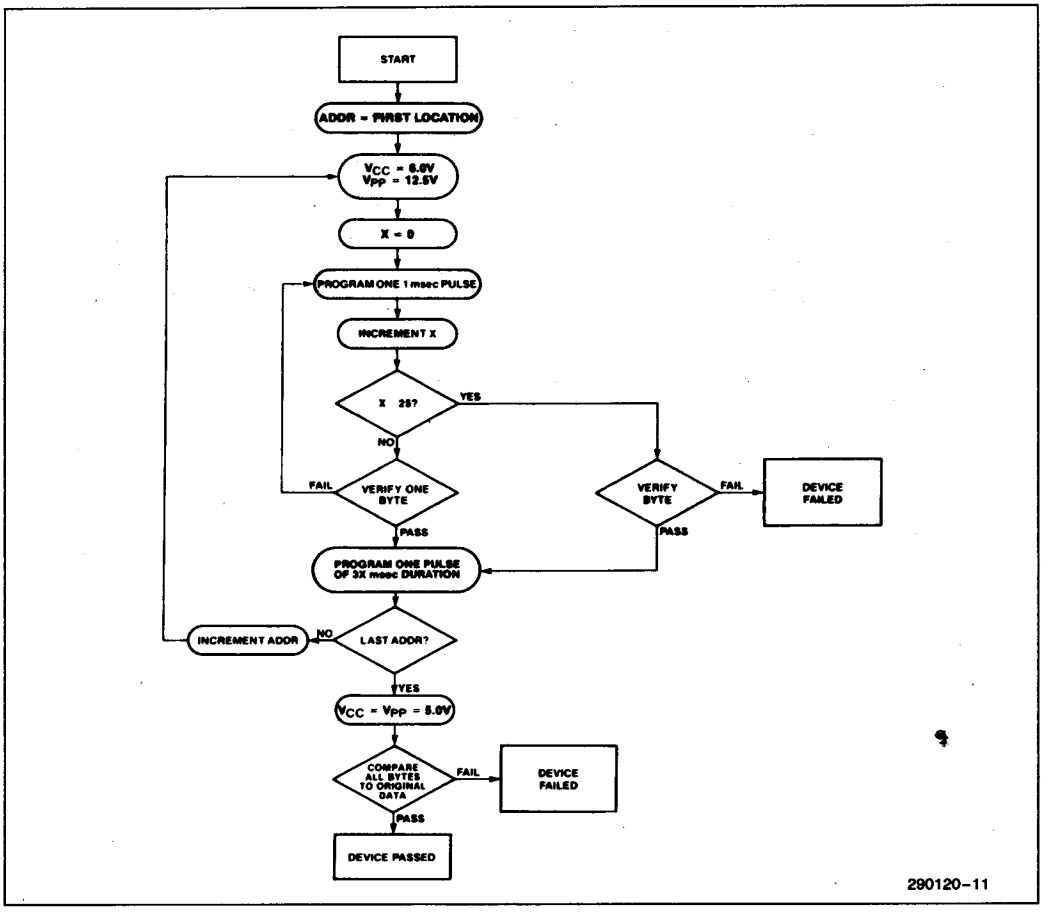


Figure 6. Int$_e$ligent Programming™ Flowchart

Int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 6.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS 27C256

$T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 Int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

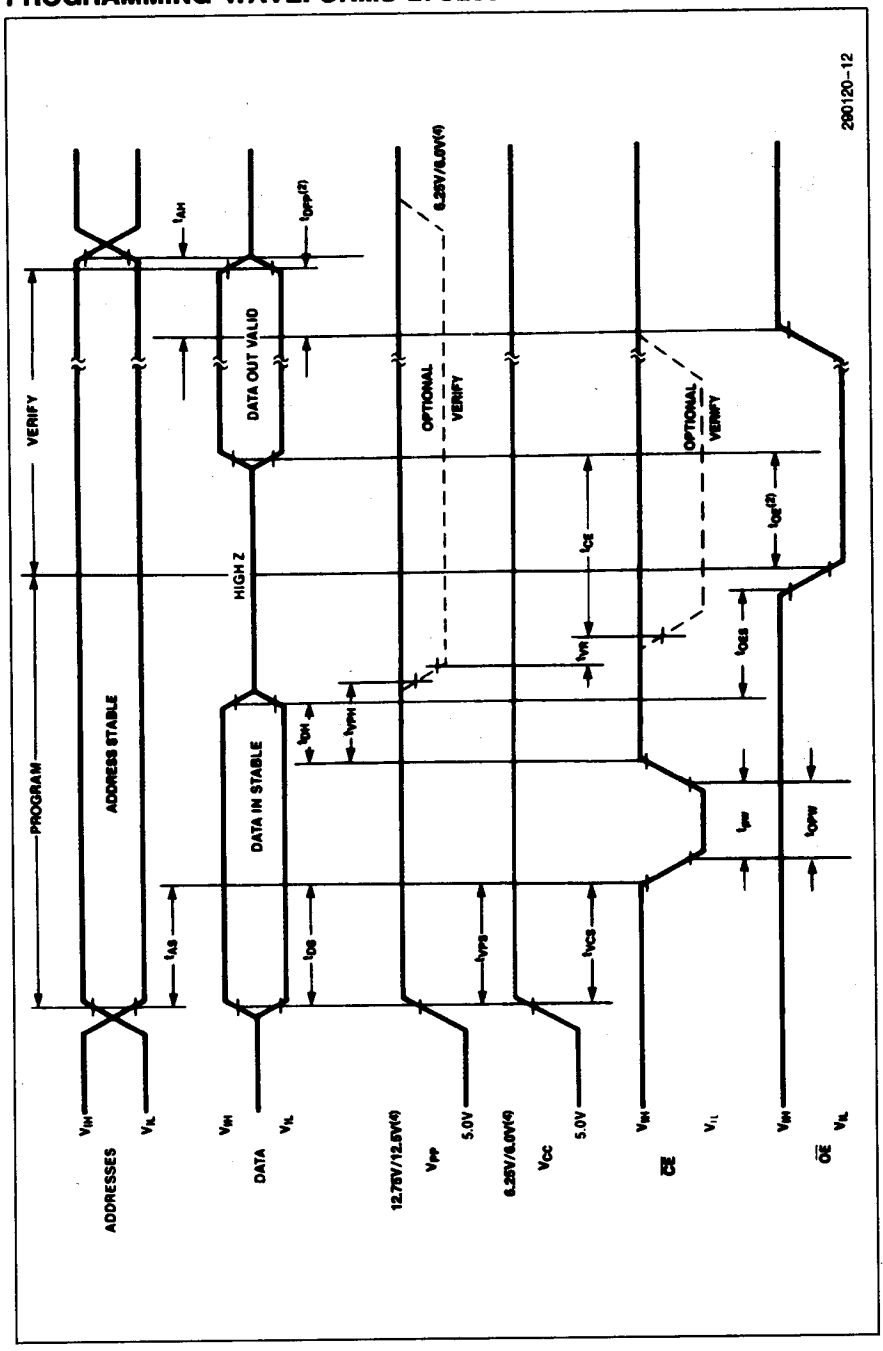
A.C. PROGRAMMING CHARACTERISTICS 27C256

T_A = 25°C ±5°C; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	µs	Quick-Pulse
		0.95	1.0	1.05	ms	int$_e$ligent
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(See Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	
t_{CE}	$\overline{CE}$ to Output Delay			500	ns	Optional Verify
t_{VR}	V_{PP} Recovery Time	2			µs	Optional Verify
t_{VPH}	V_{PP} Hold Time	2			µs	Optional Verify

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (Intelligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS 27C256



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C256, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{pp} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{pp} & 6.0V V_{CC} for intelligent Programming Algorithm.