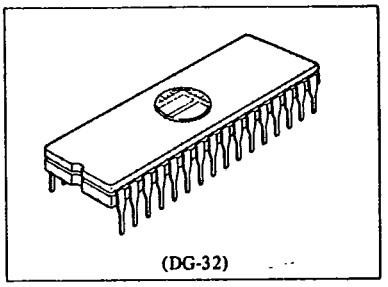
HN27C101G Series

T-46-13-29

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode . . . . . Program Voltage: +12.5V DC . . . . . High Performance Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode) 5μW typ. (Standby Mode)
- Pin Arrangement . . . . . 32 Pin JEDEC Standard

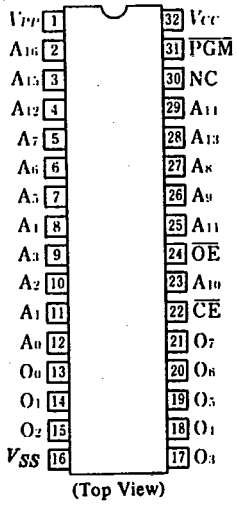


(DG-32)

■ ORDERING INFORMATION

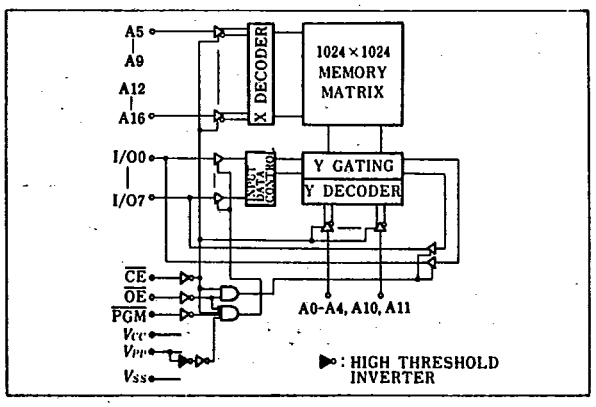
Type No.	Access Time	Package
HN27C101G-17	170ns	600 mil 32 pin Cerdip
HN27C101G-20	200ns	
HN27C101G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Notes) 1. X: Don't care
2. 30 pin should be connected to 32 pin.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

• DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	HN27C101G-17		HN27C101G-20		HN27C101G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	70	10	70	10	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

• **Test Condition**

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

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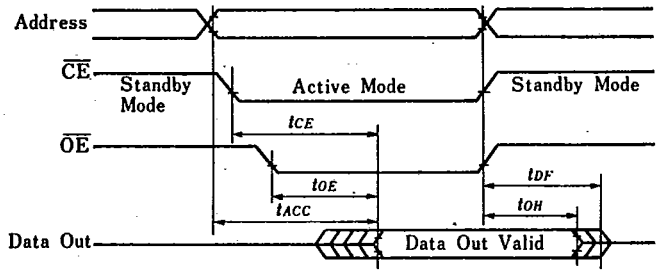
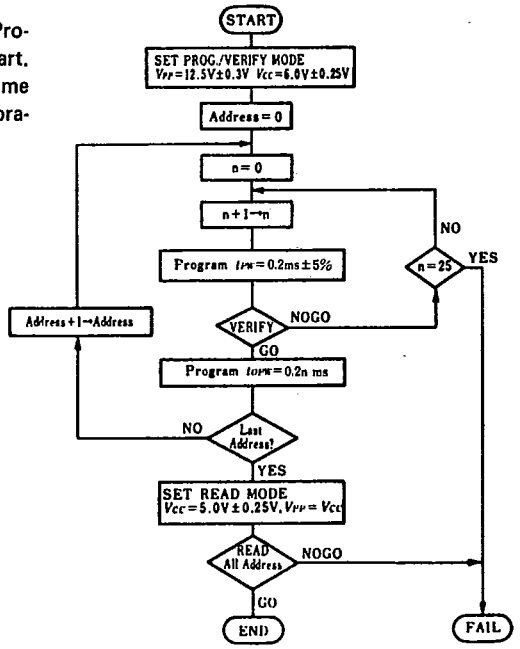


- **CAPACITANCE** (T_a=25°C, f=1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	µA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	µs
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	µs
V_{CC} Setup Time	t_{VCS}		2	–	–	µs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	µs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

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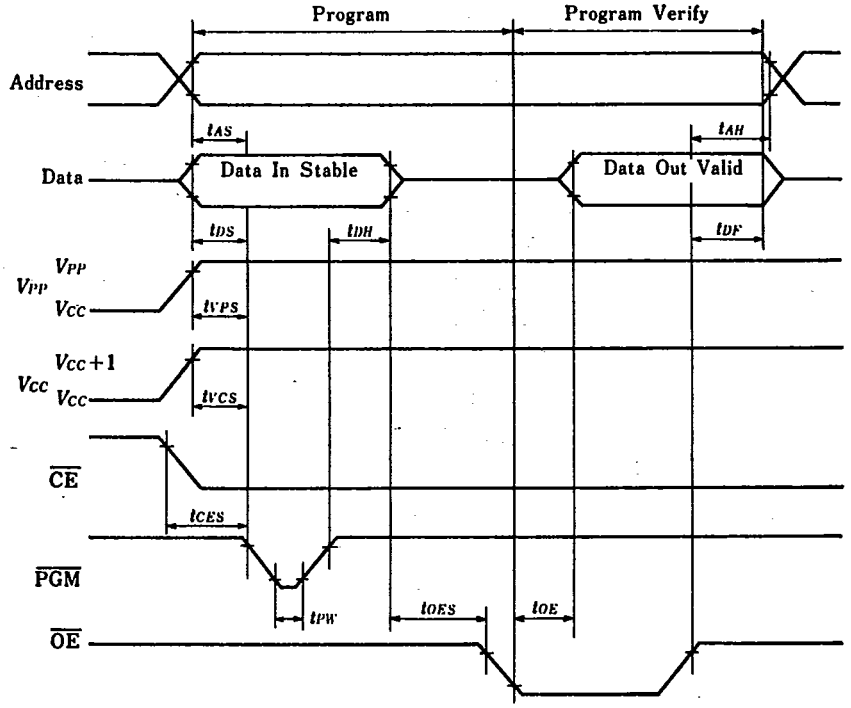
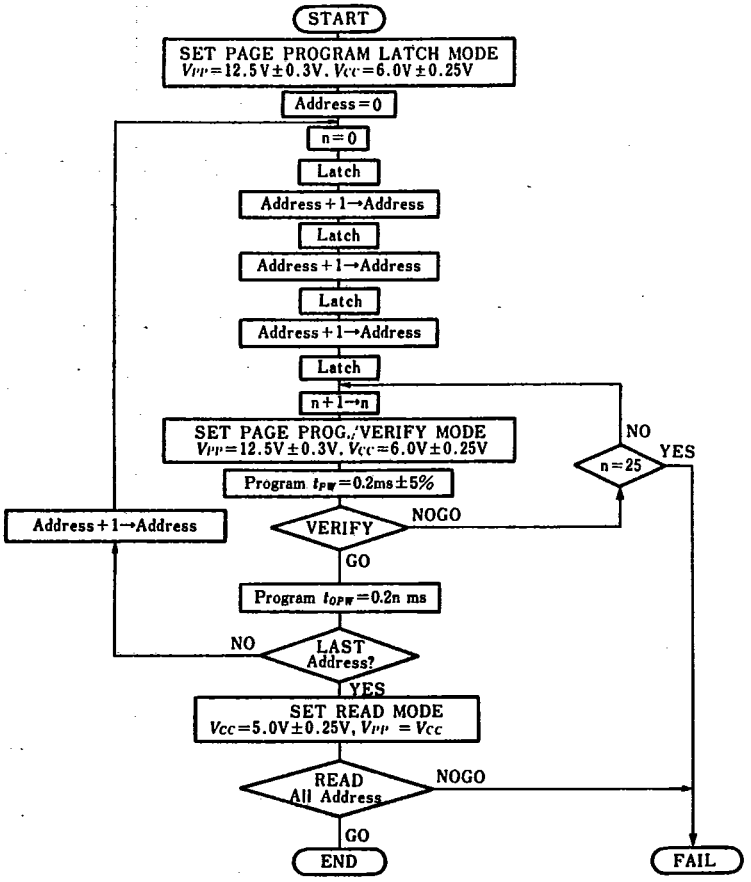
• SWITCHING CHARACTERISTICS

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



■ HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1 *5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5 *6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

T-46-13-29

• AC PROGRAMMING CHARACTERISTICS

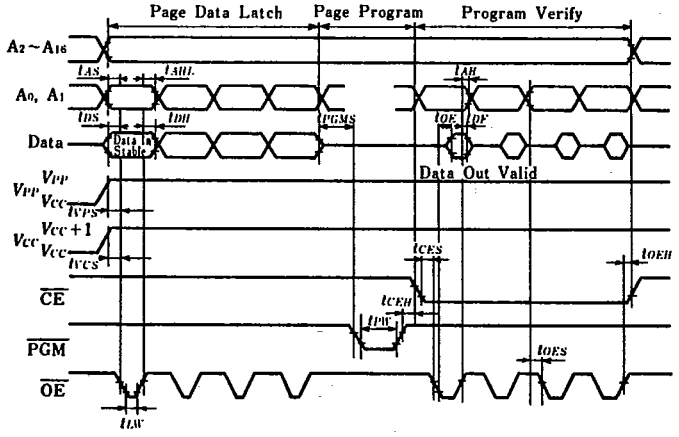
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	µs
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
	t_{AHL}		2	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	µs
V_{CC} Setup Time	t_{VCS}		2	–	–	µs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	µs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	µs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	µs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	µs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	µs

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

• SWITCHING CHARACTERISTICS

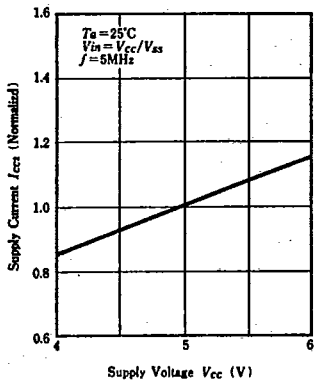
• **Test Condition** Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



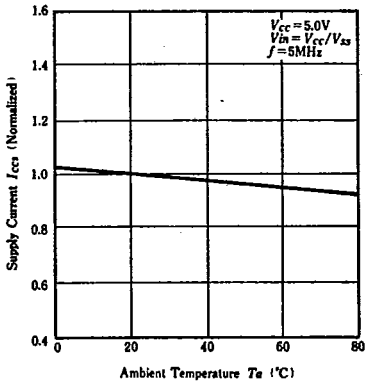
■ ERASE

Erasure of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W•sec/cm²

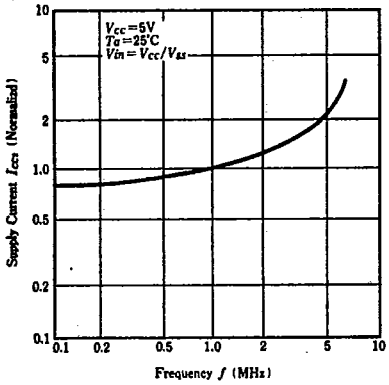
SUPPLY CURRENT vs. SUPPLY VOLTAGE



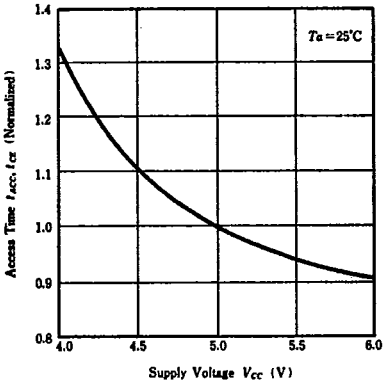
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE