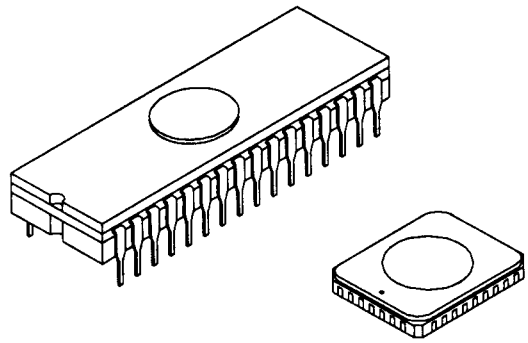
DPV27C101

128K X 8 UVPROM MONOLITHIC



DESCRIPTION:

The DPV27C101 is a high-speed 128K X 8 UV erasable, electrically programmable read only memory (EPROM). It is especially well suited for applications where low-power consumption is important.

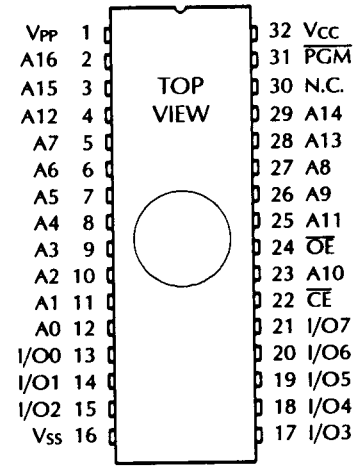
32-pin dual in-line packages (DIPs) and standard 32-pad leadless chip carriers (LCCs) are used to package the DPV27C101. A transparent lid allows the device to be erased by ultraviolet light.

The DPV27C101 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. Organization of 128K by 8-bit and a single +5V power supply facilitate its use in microprocessor systems.

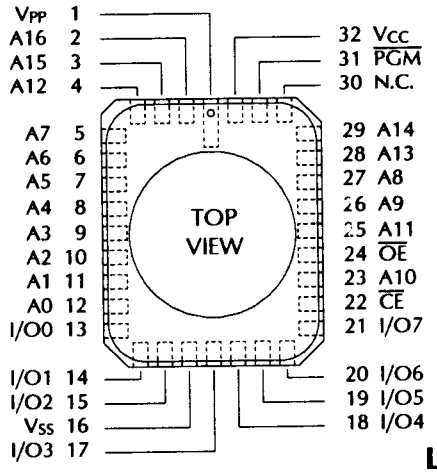
FEATURES:

- 131,072 by 8-Bits Organization, Fully Decoded
- Fast Access Times: 200, 250ns (max.)
- CMOS Power Consumption:
  - 110µW (Standby)
  - 165mW (Active)
- Single Location and Page Programming
- TTL Compatible Inputs and Outputs
- Common Data Input and Output
- Single +5V Power Supply, ± 10% Tolerance
- Three-State Output
- Simple Programming Requirements
- Fully Static Operation - No Clock Required
- High Speed Programming Algorithm (0.2ms Pulses Typ.)
- Programming Voltage: 12.5V
- Output Enable Pin for Simplified Memory Expansion
- Standard 32-Pin DIP or 32-pad LCC Packages

PIN-OUT DIAGRAMS

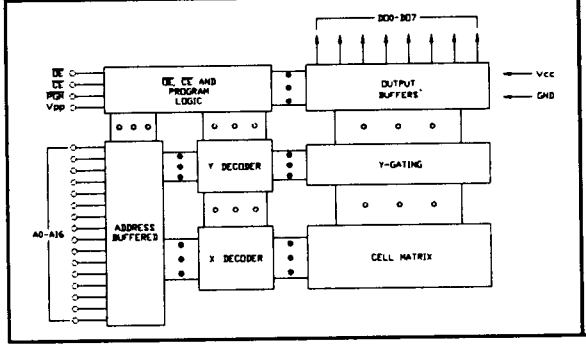


DIP



LCC

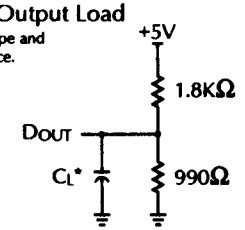
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES			
A0-A16	Address Inputs	$\overline{PGM}$	Program
I/O0-I/O7	Data In/Out	V_{PP}	Programming Voltage
$\overline{CE}$	Chip Enable	V_{CC}	Power Supply (+5V)
$\overline{OE}$	Output Enable	V_{SS}	Ground

Figure 1. Output Load

* Including Scope and Jig Capacitance.



ABSOLUTE MAXIMUM RATINGS[1]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{CC}	Supply Voltage [2]	-0.6 to +7.0	V
$V_{I/O}$	Input/Output Voltage [2]	-0.6 to +7.0	V
V_{PP}	Programming Voltage [2]	-0.6 to +13.0	V
V_{A9}	Voltage on A9 [2]	-0.6 to +13.0	V

AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{DF} and t_{DFP}
2	5 pF	t_{DF} and t_{DFP}

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	10	pF	V_{IN} = 0V
C_{ADR}	Address Input	10		
C_{OE}	Output Enable	10		
$C_{I/O}$	Data Input/Output	15		
C_{PGM}	Program	20		

RECOMMENDED OPERATING RANGE[2]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage[4]	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{CC}+1.0	V
V_{IL}	Input LOW Voltage	-0.3		0.8	V
V_{PP}	V_{PP} Supply Voltage[5]		12.5		V

DC OPERATING CHARACTERISTICS[6]: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = V_{CC}	-2	2	-2	2	-2	2	µA
I_{OUT}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{CC} or V_{SS}	-2	2	-2	2	-2	2	µA
I_{CC1}	V_{CC} Active Current, Read	V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA		25		25		25	mA
I_{CC2}	V_{CC} Operation Current, Read	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA Cycle = min. Duty = 100%		30		30		30	mA
I_{SB1}	V_{CC} Standby Current I_{OUT} = 0mA (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}		1		1		1	mA
I_{SB2}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		20		20		20	µA
I_{PP1}	V_{PP} Supply Current Byte Write	$\overline{CE}$, $\overline{PGM}$ = V_{IL}, $\overline{OE}$ = V_{IH}		40		40		40	mA
I_{PP2}	V_{PP} Supply Current Page Write	$\overline{CE}$, $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, V_{PP} = V_{CC}		50		50		50	mA
I_{PP3}	V_{PP} Supply Current Read	$\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}, I_{OUT} > 0mA		20		20		20	µA
V_{OL}	Output LOW Voltage	I_{OUT} = 2.1mA		0.45		0.45		0.45	V
V_{OH1}	Output HIGH Voltage	I_{OUT} = -400µA	2.4		2.4		2.4		V
V_{IL}	Input LOW Level		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}	Input HIGH Level		2.2	V_{CC}+1	2.2	V_{CC}+1	2.2	V_{CC}+1	V

FUNCTIONS AND PIN CONNECTIONS

Mode	Function	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	I/O0 - I/O7	Power
Read Operations	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	X	X	H			High Impedance	
	Standby	X	H	X			High Impedance	
Program Operations	Program	L	L	H	12.5V	6V	Data In	Standby
	Program Inhibit	H	H	X			High Impedance	
	Page Programming	L	H	H			High Impedance	
(T_A = +25 ± 5°C)	Program Verify	H	L	L			Data Out	

3

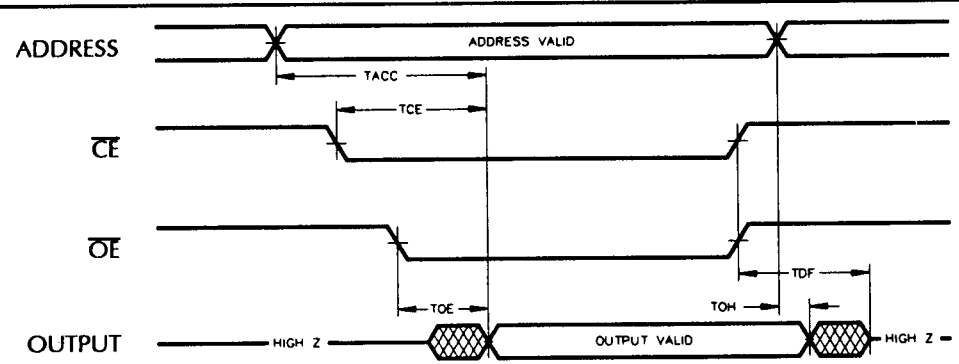
AC OPERATING CONDITIONS AND CHARACTERISTICS: Over operating ranges

No.	Symbol	Parameter	-200		-250		Unit
			Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time		200		250	ns
2	t_{CE}	Chip Enable to Output Valid [7]		200		250	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		70		100	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]	0	50	0	60	ns
5	t_{OH}	Output Hold from Address	0		0		ns

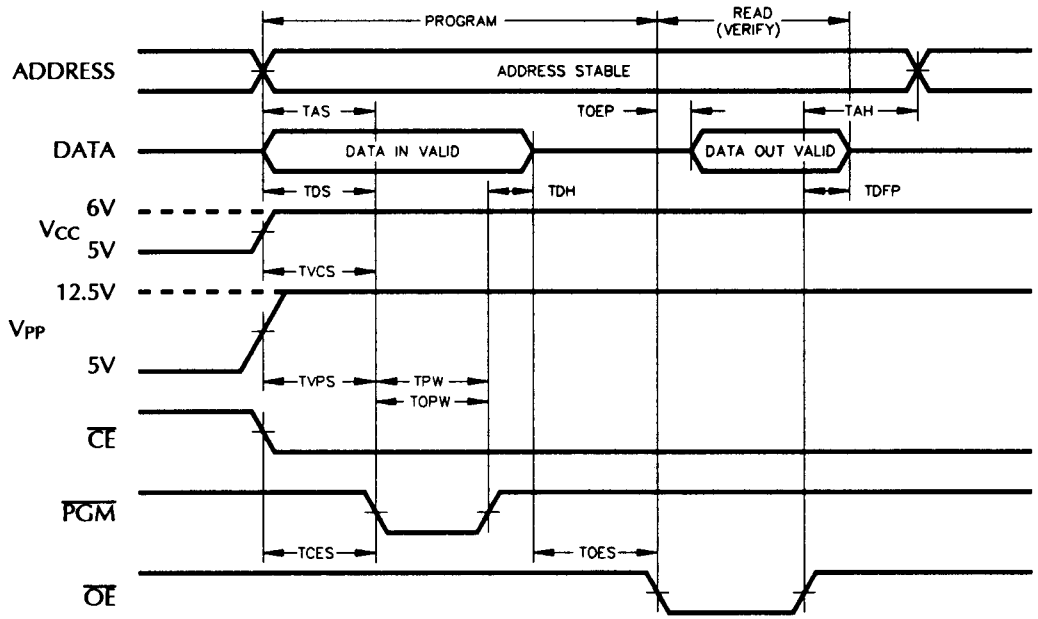
AC PROGRAMMING CONDITIONS AND CHARACTERISTICS[11]: Over operating ranges

No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Set-up Time	2		µs
7	t_{CES}	Chip Enable Set-up Time	2		µs
8	t_{OES}	Output Enable Set-up Time	2		µs
9	t_{DS}	Data Set-up Time	2		µs
10	t_{VCS}	V_{CC} Set-up Time [10]	2		µs
11	t_{VPS}	V_{PP} Set-up Time [10]	2		µs
12	t_{AH}	Address Hold Time	0		µs
13	t_{OEH}	Output Enable Hold Time	2		µs
14	t_{DH}	Data Hold Time	2		µs
15	t_{CEP}	Chip Enable to Data Valid		150	ns
16	t_{DFP}	Output Enable HIGH Output Float Delay [3]	0	130	ns
17	t_{PW}	Programming Pulse Width [10]	0.19	0.21	ms
18	t_{OPW}	Over Programming Pulse Width [11]	0.19	5.25	ms
19	t_{AHL}	Address Latch Hold Time	2		µs
20	t_{LW}	Output Enable Pulse Width During Data Latch	1		µs
21	t_{PGMS}	Page Programming Setup Time	2		µs
22	t_{CEH}	Chip Enable Hold Time	2		µs

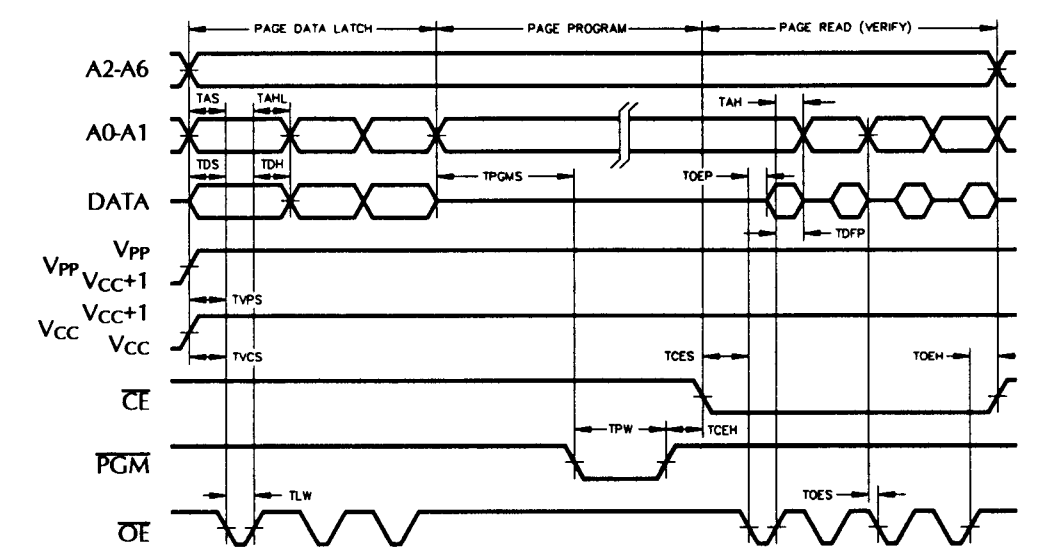
READ TIMING



BYTE PROGRAMMING TIMING [4]



PAGE PROGRAMMING TIMING [4]



PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure *(See Erasure section)*, the DPV27C101 contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV27C101 through the procedure of programming. A 0.1µF capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{CC} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the byte mode programming algorithm shown in Figure 2. In byte programming mode, $\overline{CE}$ is set at V_{IL} and $\overline{OE}$ is set at V_{IH}. After the applied address and input data signals are stable, programming is accomplished by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin *(refer to the Byte Mode Programming Timing Diagram)*.

The DPV27C101's fast page mode programming algorithm *(shown in Figure 3)* provides a great reduction in programming time by writing four bytes simultaneously. Each of these four bytes may contain different data. In page programming mode, $\overline{CE}$ and $\overline{PGM}$ are at V_{IH} while input data is strobed into internal holding registers by V_{IL} pulses on the $\overline{OE}$ pin. The EPROM is then programmed by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin while $\overline{CE}$ and $\overline{OE}$ are held at V_{IH} *(refer to the Page Programming Timing Diagram)*.

System design consideration must be taken to avoid inadvertent page mode programming which can occur when $\overline{CE}$ and $\overline{OE}$ are at V_{IH} and $\overline{PGM}$ is at V_{IL}.

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Erasure

Clear all locations of their programmed contents it is necessary to expose the DPV27C101 to an ultraviolet light source. A dosage of 15W- seconds/cm^2 is required to completely erase a DPV27C101. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with an intensity of 12,000µW/cm^2 for 21 minutes.

The DPV27C101 and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV27C101. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. V_{CC} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 13.0V. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. t_A = -55°C to +125°C, V_{CC} = 5.0V ± 0.5V, and V_{PP} = V_{CC} reading. t_A = +25°C ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.3V programming.
7. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the following edge of $\overline{CE}$ without impact on t_{CE}.
8. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the following Address is valid without impact on t_{ACC}.
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Initial Program Pulse Width Tolerance is 0.2ms ± 5%.
11. The length of the overprogram pulse may vary from 0.19ms to 5.25ms as a function of the iteration counter value X.

Figure 2. Programming Flow Chart

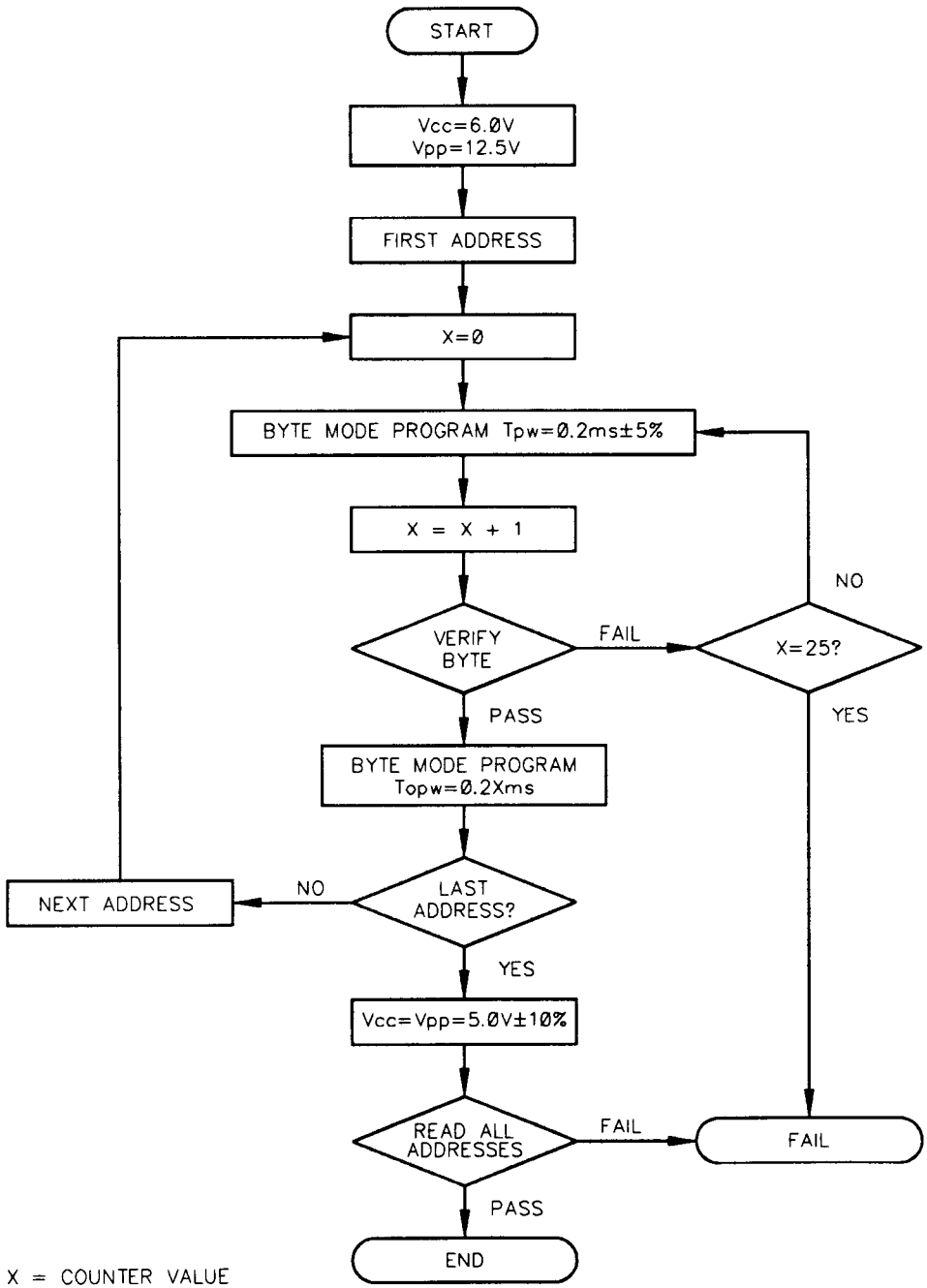

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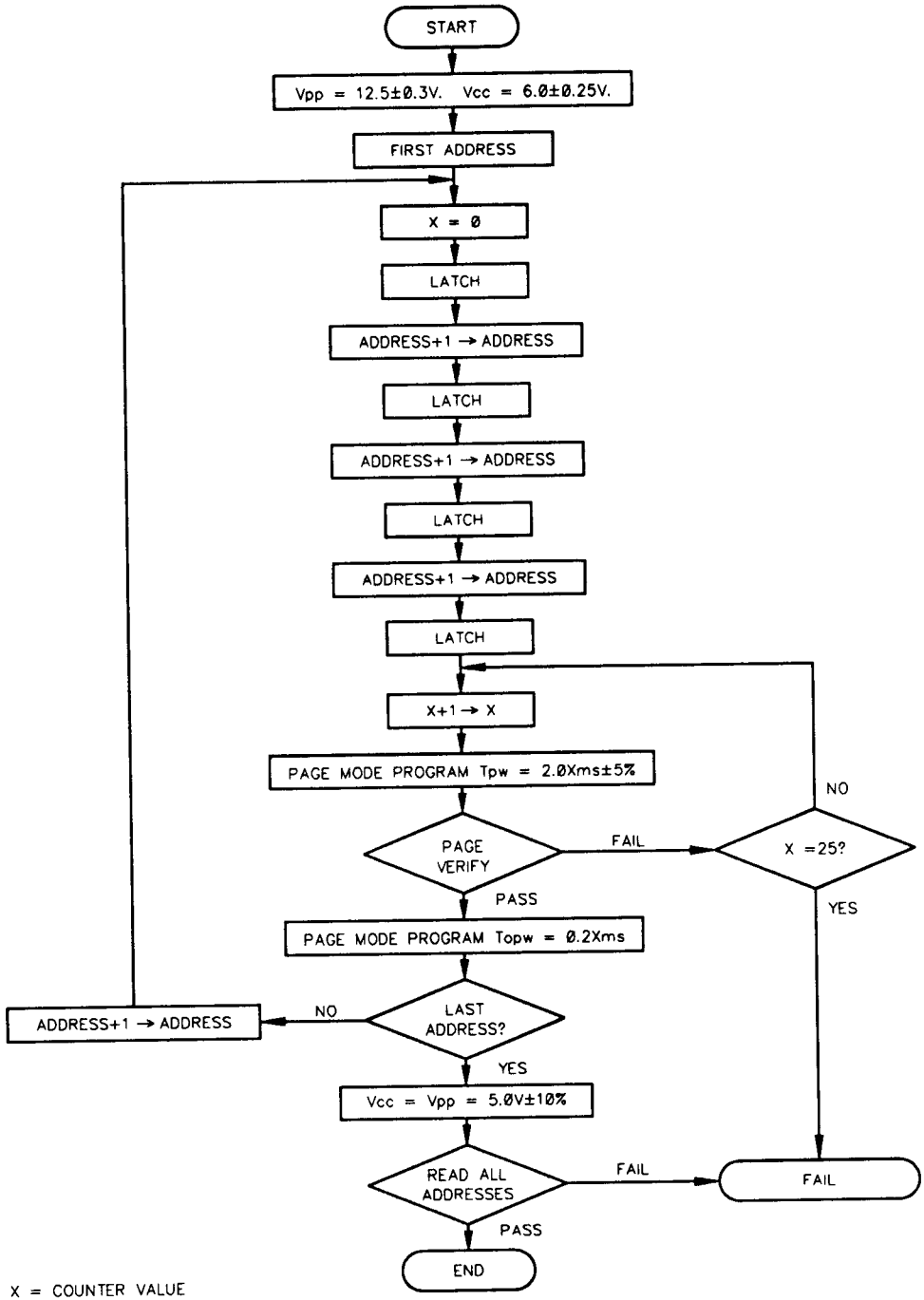
Figure 3. High Performance Page Programming Flow Chart



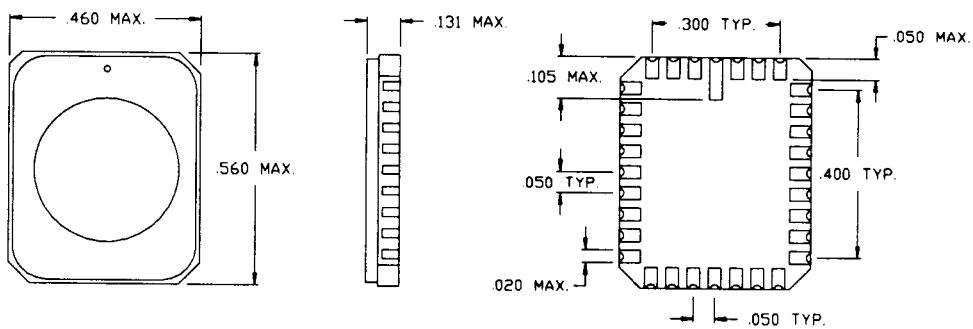
ORDERING INFORMATION

DP V27C1Ø1 G -XXX X

PREFIX | DEVICE TYPE | PACKAGE | SPEED | GRADE

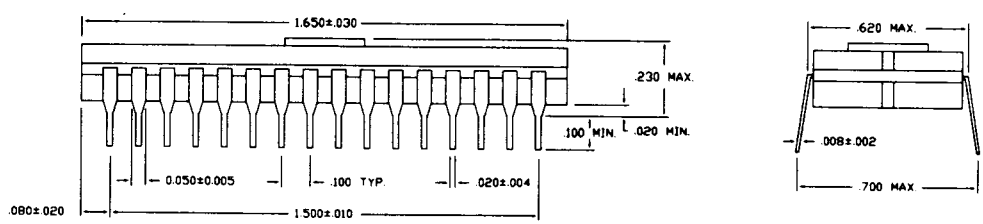
C	COMMERCIAL	Ø°C to +7Ø°C
I	INDUSTRIAL	-4Ø°C to +85°C
M	MILITARY	-55°C to +125°C
B	MIL-PROCESSED	-55°C to +125°C
2ØØ	2ØØns	
25Ø	25Øns	
G	32-PAD LCC	
NONE	32-PIN CERDIP	
128K X 8 UVPROM		

MECHANICAL DIAGRAMS



NOTE: Shape of Pin 1 subject to change without notice.

LCC



DIP

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