FAIRCHILD
SEMICONDUCTOR™

March 1997

NM27C512
524,288-Bit (64K x 8) High Performance CMOS EPROM

General Description

The NM27C512 is a high performance 512K UV Erasable Electrically Programmable Read Only Memory (EPROM). It is manufactured using Fairchild's proprietary CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

The NM27C512 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90 ns access time provides no wait-state operation with high-performance CPUs. The NM27C512 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

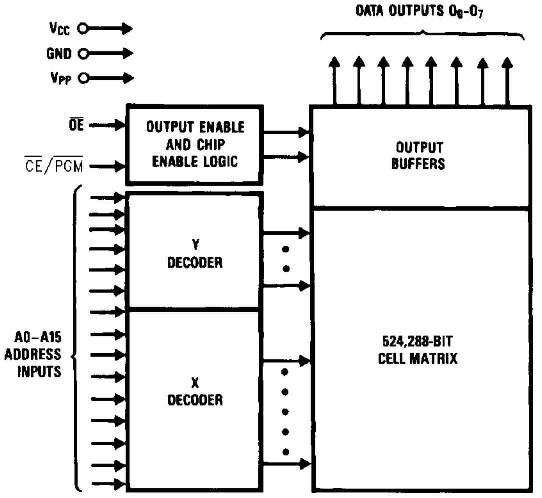
The NM27C512 is configured in the standard JEDEC EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C512 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - — 90 ns access time
- Fast turn-off for microprocessor compatibility
- Manufacturers identification code
- JEDEC standard pin configuration
  - — 28-pin DIP package
  - — 32-pin chip carrier

Block Diagram



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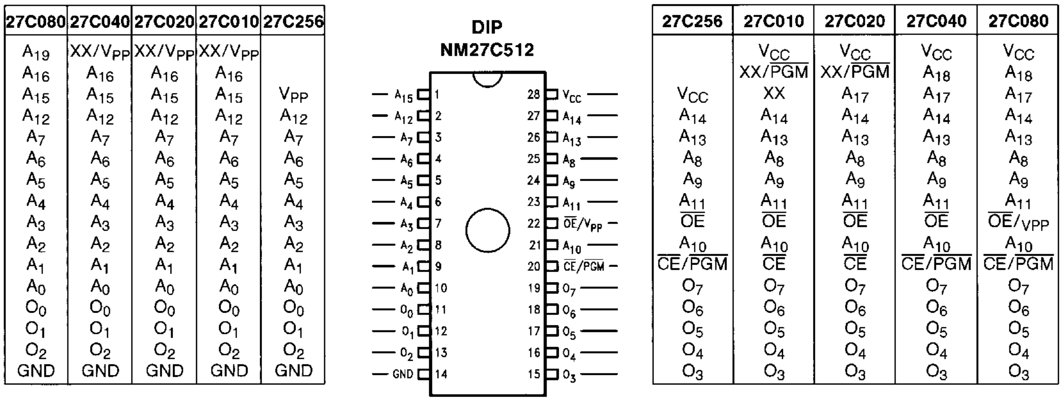
Connection Diagrams



27C080	27C040	27C020	27C010	27C256
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27C256	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{\text{PGM}}$	XX/$\overline{\text{PGM}}$	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{\text{CE}}/\overline{\text{PGM}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}/\overline{\text{PGM}}$	$\overline{\text{CE}}/\overline{\text{PGM}}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

DS010834-9

Compatible EPROM pin configurations are shown in the blocks adjacement to the NM27C512 pins.

Commercial Temp Range (0˚C to +70˚C)

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C512 Q, N, V 90	90
NM27C512 Q, N, V 120	120
NM27C512 Q, N, V 150	150

Industrial Temp Range (−40˚C to +85˚C)

Parameter/Order Number	Access Time (ns) (Note 1)
NM27C512 QE, NE, VE 90	90
NM27C512 QE, NE, VE 120	120
NM27C512 QE, NE, VE 150	150

Note 1: All versions are guaranteed to function for slower speeds.

Q = Quartz-Windowed Ceramic DIP Package

N = Plastic DIP Package

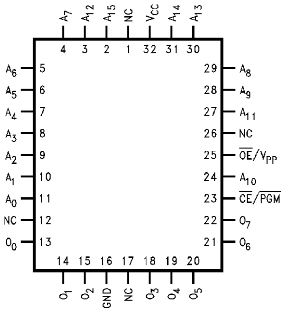
V = PLCC Package

- All packages conform to the JEDEC standard.

Pin Names

A0–A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
O0–O7	Outputs
$\overline{\text{PGM}}$	Program
XX	Don't Care (During Read)

PLCC



DS010834-3

Absolute Maximum Ratings (Note 2)

Storage Temperature	−65˚C to +150˚C
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0˚C to +70˚C	+5V	±10%
Extended	−40˚C to +85˚C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC1}	V_{CC}Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	f = 5 MHz		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C, E Temp Ranges			35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	µA

AC Electrical Characteristics

Symbol	Parameter	90		120		150		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		40		50		50	
t_{DF}	Output Disable to Output Float		35		25		45	
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance

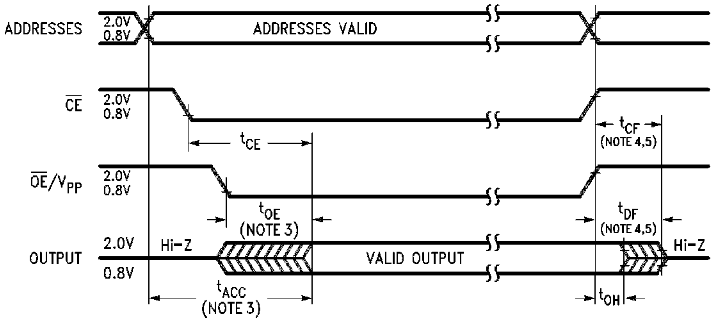
$T_A = +25^{\circ}C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}$ /V_{PP}	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}$ /V_{PP} Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 10)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7) (Note 8)



DS010834-4

Note 2: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC}- t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

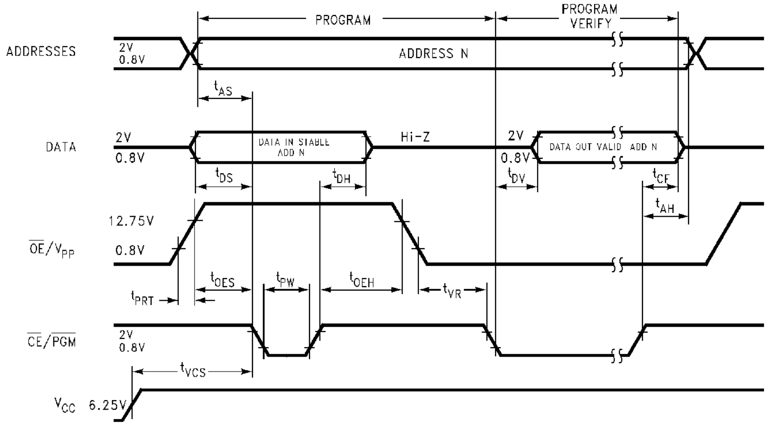
Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 µA.
C_L: 100 pF includes fixture capacitance.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Note 11) and (Note 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		45	50	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	˚C
V_{CC}	Power Supply Voltage		6.25	6.5	6.75	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



DS010834-5

Note 11: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Turbo Programming Algorithm Flow Chart

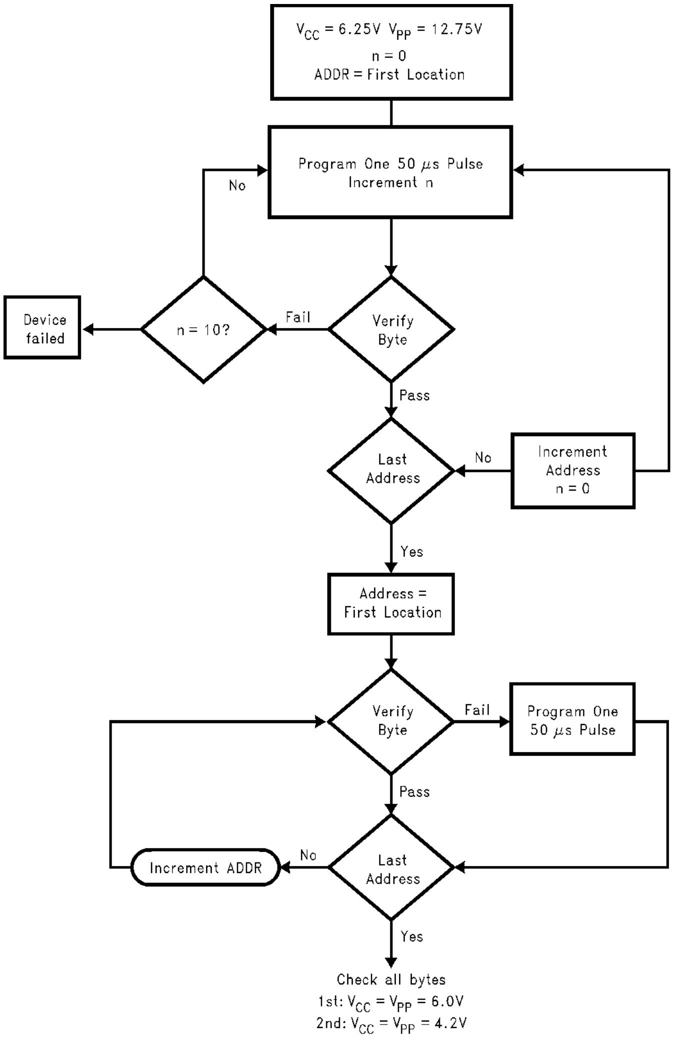


FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in *Table 1*. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE}after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the “1’s” state. Data is introduced by selectively programming “0’s” into the desired bit locations. Although only “0’s” will be programmed, both “1’s” and “0’s” can be presented in the data word. The only way to change a “0” to a “1” is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 µF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Turbo Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 50 µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 µs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.)

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE/V_{PP}) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM’s CE/PGM input with OE/V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with OE/V_{PP} and CE at V_{IL}. Data should be verified T_{DV} after the falling edge of CE.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER’S IDENTIFICATION CODE

The EPROM has a manufacturer’s identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer’s Identification code, shown in *Table 2*, specifically identifies the manufacturer and device type. The code for NM27C512 is “8F85”, where “8F” designates that it is made by Fairchild Semiconductor, and “85” designates a 512K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins

Functional Description (Continued)

are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25˚C ±5˚C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table 3 shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C512 are listed in *Table 1*. A single 5V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE 1. Mode Selection

Pins Mode	$\overline{CE}$ /$\overline{PGM}$	$\overline{OE}$ /V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X(Note 14)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 14: X can be V_{IL} or V_{IH}.

TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

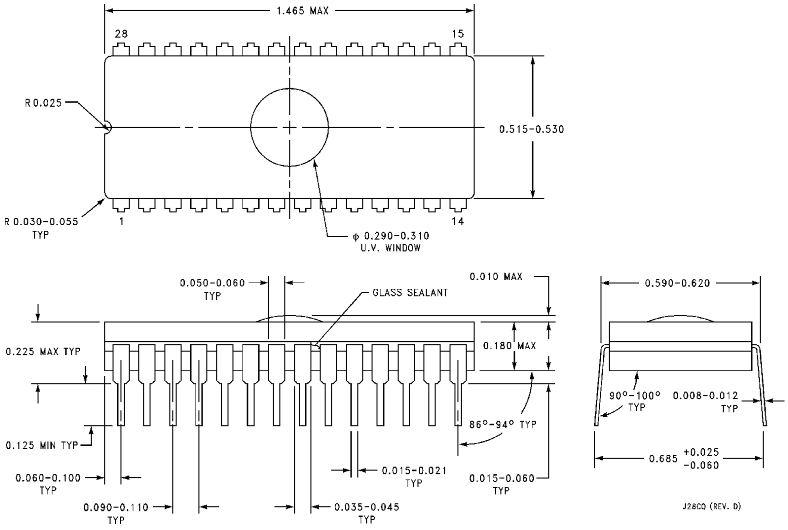
Mode Selection (Continued)

TABLE 3. Minimum NM27C512 Erasure Time

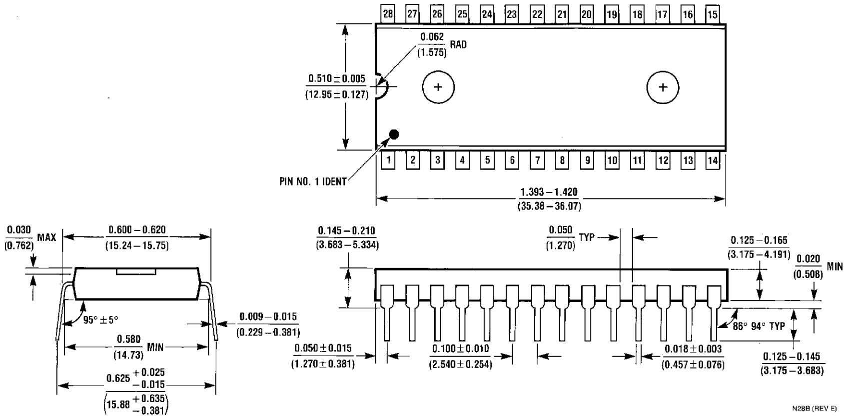
Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Book
Extract
End

Physical Dimensions inches (millimeters) unless otherwise noted

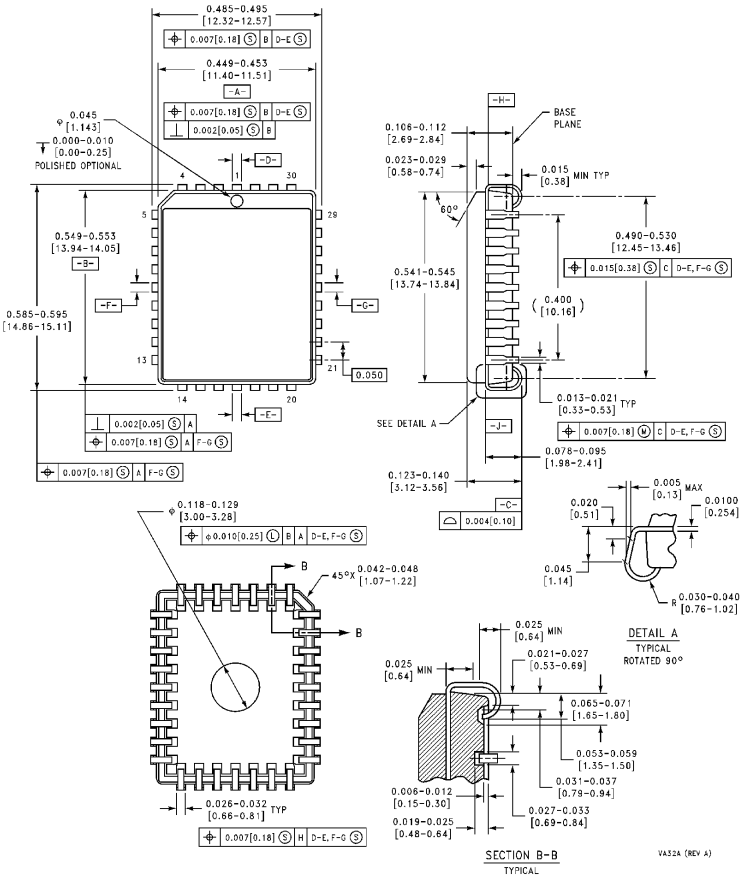


UV Window Cavity Dual-In-Line Cerdip Package (JQ)
Order Number NM27C512Q
Package Number J28CQ



28-Lead Plastic One-Time-Programmable Dual-In-Line
Order Number NM27C512N
Package Number N28B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM27C512V
Package Number VA32A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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