PRELIMINARY

16MEGA BIT (1,048,576 WORD × 16BIT/2,097,152 WORD × 8BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

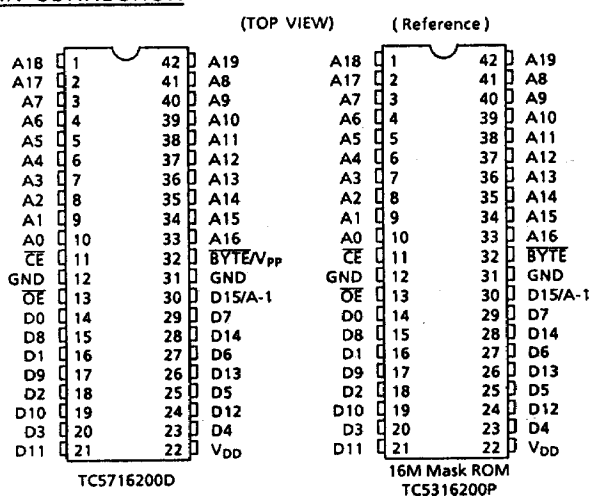
DESCRIPTION

The TC5716200D is a 16,777,216 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 1M words by 16 bits or 2M words by 8 bits. The TC5716200D is compatible with 42 pin 16M bit Mask ROM. This product is packed in 42 pin standard cerdip package. The TC5716200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 150ns/200ns and a maximum operating current of 60mA/6.7MHz. The programming time of the TC5716200D except overhead times of EPROM programmer is only 52 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Fast access time
  (V_{CC}=5V±10%, Ta=0~70°C)
  TC5716200D-150 : 150ns
  TC5716200D-200 : 200ns
- Single 5V power supply
- Low power dissipation
- Standby : 100μA
- Full static operation
- Input and output TTL compatible
- Three state output
- High speed programming operation : t_{PW} 25μs
- 16M MROM compatible pinout : TC5316200P
- Standard 42 pin DIP cerdip package : WDIP42-G-600B

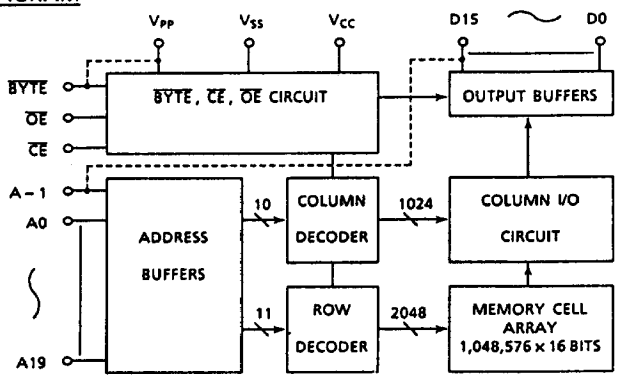
PIN CONNECTION



PIN NAMES

A0~A19	Address Input
D0~D14	Output (Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Output (Input) / Address Input
$\overline{BYTE}$/V_{PP}	Word, Byte select Input / Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS	CE	OE	BYTE / VPP	VCC	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6~7.0	V
V_{PP}	Program Supply Voltage	-0.6~14.0	V
V_{IN}	Input Voltage	-0.6~7.0	V
V_{IN} (A9)	Input Voltage (A9)	-0.6~13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6~V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec
T_{STRG}	Storage Temperature	-65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	- 0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.50	5.00	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0V~V_{CC}	-	-	± 10	μA
I_{CCO1}	Operating Current	$\overline{CE}$ = 0V I_{OUT} = 0mA f = 6.7MHz	-	-	60	mA
I_{CCO2}		$\overline{CE}$ = 0V I_{OUT} = 0mA f = 1MHz	-	-	25	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	-	-	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} - 0.2V	-	-	100	μA
V_{OH}	Output High Voltage	I_{OH} = - 400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0V~V_{CC} + 0.6V	-	-	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V~V_{CC}	-	-	± 10	μA

A.C. CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	- 150		- 200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High Impedance	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High Impedance	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	ns
t_{BT}	$\overline{BYTE}$ to Output Valid	-	150	-	200	ns
t_{BTD}	$\overline{BYTE}$ to Output in High Impedance	-	70	-	70	ns

- A.C. TEST CONDITIONS
  - Output Load : 1 TTL Gate and CL = 100PF
  - Input Pulse Rise and Fall Time : 10ns Max
  - Input Pulse Levels : 0.45V and 2.4V
  - Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

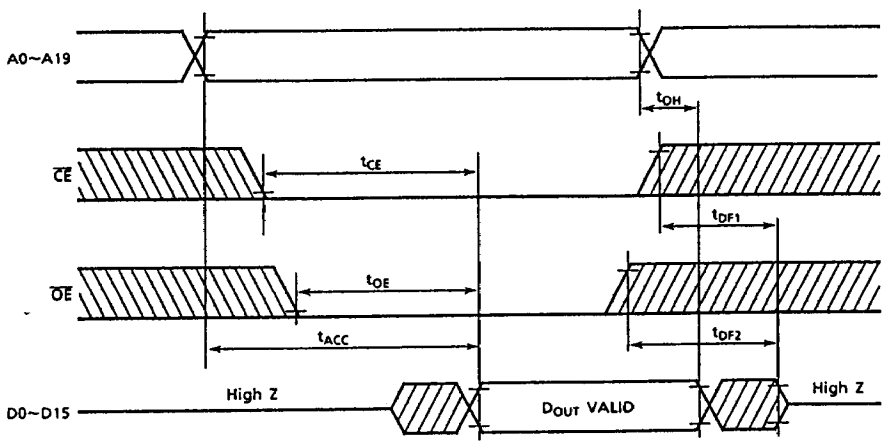
CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN} = 0V	-	6	10	pF
C_{IN2}	Input Capacitance ($\overline{BYTE}$ / V_{PP})	V_{IN} = 0V	-	110	120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	10	12	pF

* This parameter is periodically sampled and is not 100% tested.

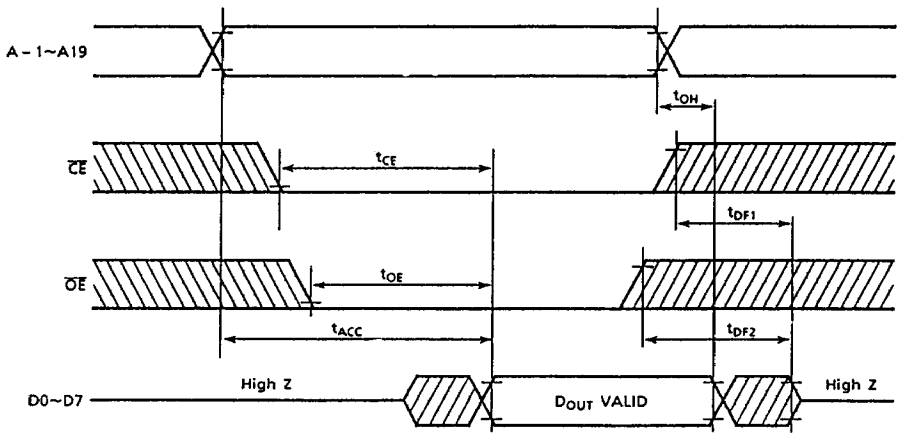
TIMING WAVEFORMS

WORD-WIDE READ MODE



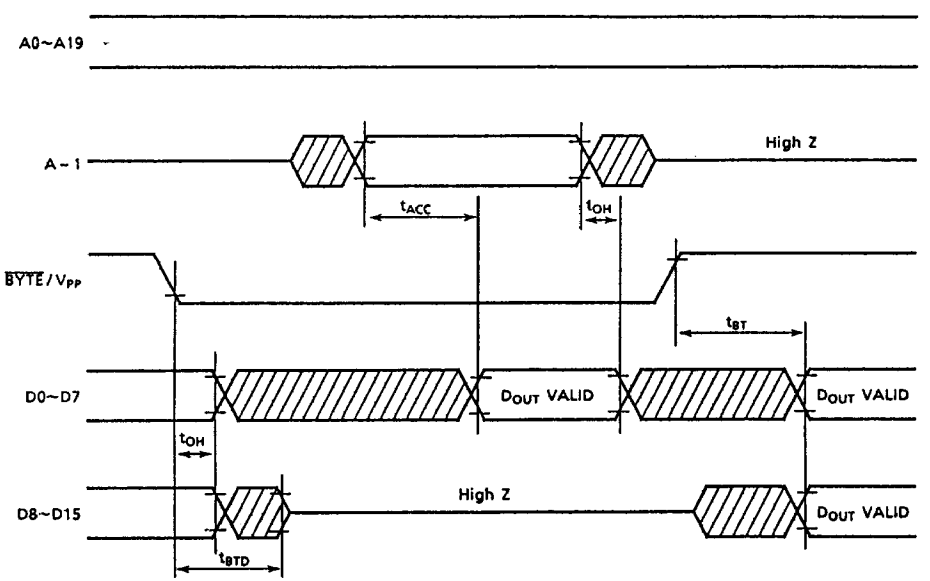
Note: $\overline{BYTE}$ / V_{PP} = V_{IH}

BYTE – WIDE READ MODE



Note: $\overline{BYTE}$ / $V_{PP} = V_{IL}$

$\overline{BYTE}$ TRANSITION



Note: $\overline{CE}$, $\overline{OE} = V_{IL}$

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	- 0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	V
V_{PP}	V_{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25 ± 0.25V, V_{PP} = 12.50 ± 0.30V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0V~V_{CC}	-	-	± 10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 12.8V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.25 ± 0.25V, V_{PP} = 12.50 ± 0.30V)

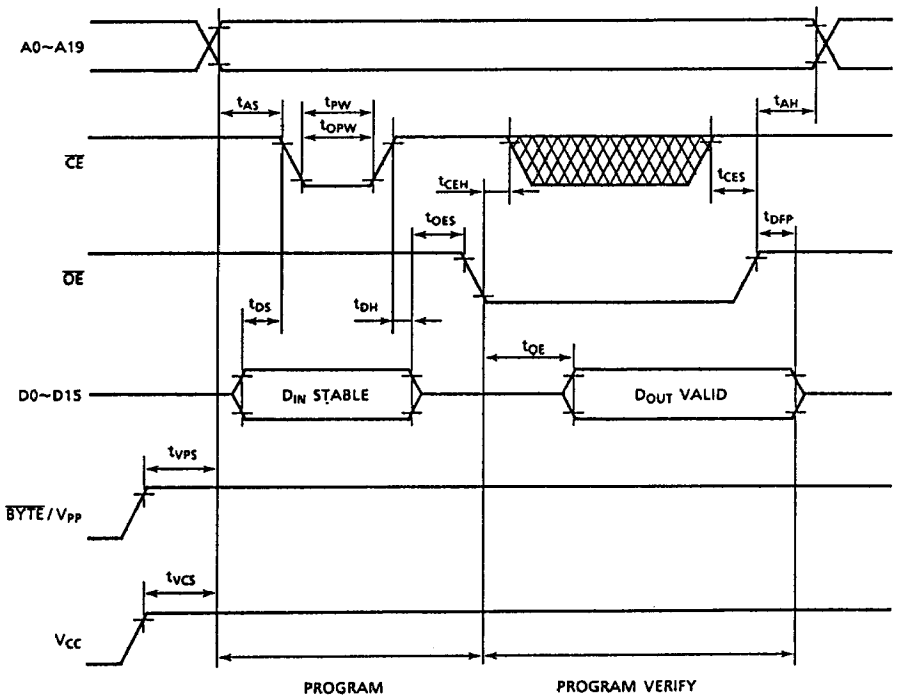
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	22.5	25	27.5	μs
t_{OPW}	Overprogram Pulse Width	Note 1	22.5	25	27.5	μs
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High Impedance	$\overline{CE}$ = V_{IH}	-	-	90	ns

- A.C. TEST CONDITIONS
  - Output Load : 1 TTL Gate and CL = 100PF
  - Input Pulse Rise and Fall Time : 10ns Max
  - Input Pulse Levels : 0.45V and 2.4V
  - Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1 : t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP} = 12.50V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TC5716200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [W / cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec / cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps of which ultraviolet light intensity is a 12000 [μW / cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW / cm^2] × (20×60) [sec] ≒ 15 [W · sec / cm^2].)

The TC5716200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC907 - are available.

OPERATION INFORMATION

The TC5716200D's eight operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ / V_{PP}	V_{CC}	D0~D7	D8~D14	D15 / A-1	Power
Read (16 Bit)	L	L	H	5V	Data Out			Active
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L	
Read (Upper 8 Bit)	L	L	L		Data Out (Upper 8 Bit)	High Impedance	H	
Output Deselect	L	H	H		High Impedance			
			L		High Impedance		*	
Standby	H	*	H		High Impedance			Standby
			L		High Impedance		*	
Program	L	H	12.5V	6.25V	Data In			Active
Program Inhibit	H	H			High Impedance			
Program Verify	*	L			Data Out			

Note: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

READ MODE

The TC5716200D has the $\overline{BYTE}$ / V_{PP} terminal that selects word-wide output or byte-wide output. When $\overline{BYTE}$ / V_{PP} is set to V_{IH}, the word-wide output is selected, and D15 / A-1 pin is used for D15 data output.

When $\overline{BYTE}$ / V_{PP} is set to V_{IL}, the byte-wide output is selected, and D15 / A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, lower 8 bits of the 16 bit data which has been programmed are selected. When A-1 is set to V_{IH}, upper 8 bits are selected.

The TC5716200D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC5716200D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC5716200D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC5716200D is placed in the standby mode which reduces the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC5716200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0" data into the desired bit location by electrically programming. The TC5716200D is in the programming mode when the V_{PP} input is at 12.50V and $\overline{CE}$ is at TTL - Low under $\overline{OE}=V_{IH}$. Data to be programmed must be applied 16 bits in parallel to the data pins.

Data can be programmed in any locations at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL}. The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC5716200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

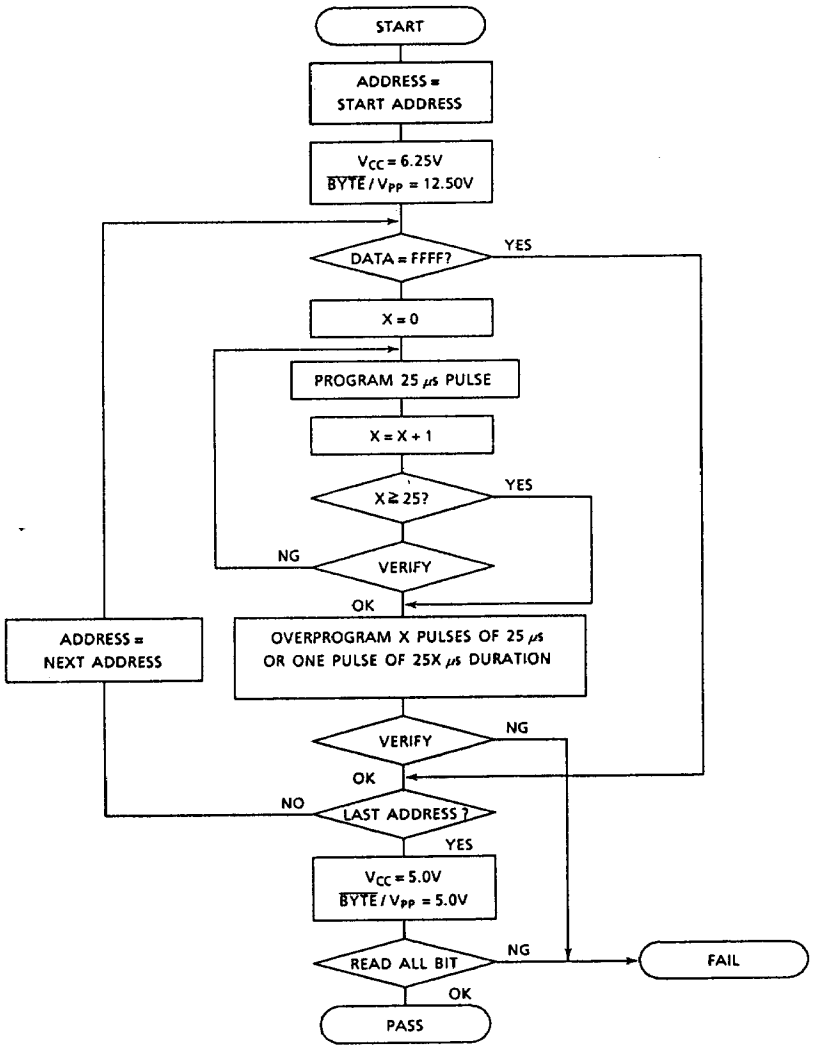
HIGH SPEED PROGRAM MODE

The device is subjected to the high speed programming mode when the programming voltage (12.50V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$. The programming is achieved by applying a single TTL low level 25μs pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, one more program pulse of 25μs is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC5716200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC5716200D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC5716200D.

PINS / SIGNATURE	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	1	1	0	1	0	**1A

Note: A1 - A8, A10 - A19, $\overline{CE}$, $\overline{OE} = V_{IL}$, A9 = 12V ± 0.5V
$\overline{BYTE}$ / VPP = V_{IH}
* Don't care

OUTLINE DRAWINGS

WDIP42-G-600B

Unit in mm