S-80 Only 020601

002042

T-2042 SGS

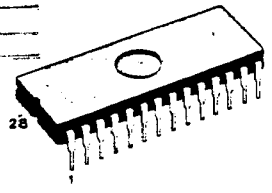
# M27256

def 9-2332

UNRES

# 256K (32K x 8) UV ERASABLE PROM

- FAST ACCESS TIME:
  200ns MAX M27256-2F1
  250ns MAX M27256F1/M27256F6/M27256-25F1
  300ns MAX M27256-3F1/M27256-30F1
  450ns MAX M27256-4F1/M27256-4F6/M27256-45F1
- 0 to 70°C STANDARD TEMPERATURE RANGE
- −40 to +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE
- ±10% $V_{CC}$ TOLERANCE AVAILABLE




F
Ceramic Package

ORDERING NUMBERS: M27256-2F1
M27256F1
M27256-3F1
M27256-4F1
M27256-25F1
M27256-30F1
M27256-45F1
M27256F6
M27256-4F6

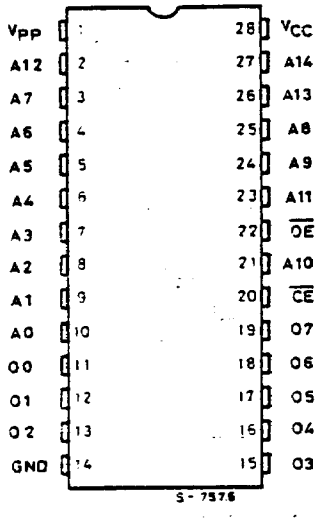
## DESCRIPTION

The M27256 is a 262,144-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 32.768 words by 8 bits and manufactured using SGS' NMOS-E3 process. The M27256 with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8®, Z80® and Z8000™. The M27256 has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminate bus contention in multiple bus microprocessor systems.

The M27256 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40 mA, a 60% saving. The standby mode is achieved by appling a TTL-high signal to the $\overline{CE}$ input. The M27256 enables implementation of new, advanced systems with firmware-intensive architectures.

The combination of the M27256's high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27256 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27256 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27256 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

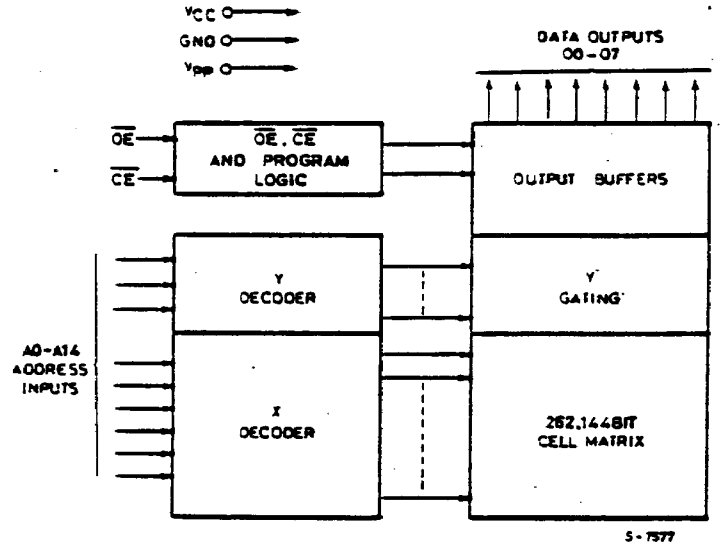
## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| A0-A14 | ADDRESS INPUT |
| $\overline{CE}$ | CHIP ENABLE INPUT |
| $\overline{OE}$ | OUTPUT ENABLE INPUT |
| O0-O7 | DATA INPUT/OUTPUT |

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_I$ | All Input or Output voltages with respect to ground | +6.25 to −0.6 | V |
| $V_{PP}$ | Supply voltage with respect to ground | +14 to −0.6 | V |
| $T_{amb}$ | Ambient temperature under bias /F1<br>/F6 | −10 to +80<br>− 50 to +95 | °C<br>°C |
| $T_{stg}$ | Storage temperature range | − 65 to +125 | °C |
| | Voltage on pin 24 with respect to ground | +13.5 to −0.6 | V |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating on and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specificatio is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## OPERATING MODES

| MODE \ PINS | $\overline{CE}$ (20) | $\overline{OE}$ (22) | A9 (24) | A0 (10) | $V_{PP}$ (1) | $V_{CC}$ (28) | OUTPUTS (11-13, 15-19) |
|---|---|---|---|---|---|---|---|
| READ | $V_{IL}$ | $V_{IL}$ | X | X | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| OUTPUT DISABLE | $V_{IL}$ | $V_{IH}$ | X | X | $V_{CC}$ | $V_{CC}$ | HIGH Z |
| STANDBY | $V_{IH}$ | X | X | X | $V_{CC}$ | $V_{CC}$ | HIGH Z |
| PROGRAM | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |
| VERIFY | $V_{IH}$ | $V_{IL}$ | X | X | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| OPTIONAL VERIFY | $V_{IL}$ | $V_{IL}$ | X | X | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| PROGRAM INHIBIT | $V_{IH}$ | $V_{IH}$ | X | X | $V_{PP}$ | $V_{CC}$ | HIGH Z |
| ELECTRONIC SIGNATURE | $V_{IL}$<br>$V_{IL}$ | $V_{IL}$<br>$V_{IL}$ | $V_H$<br>$V_H$ | $V_{IL}$<br>$V_{IH}$ | $V_{CC}$<br>$V_{CC}$ | $V_{CC}$<br>$V_{CC}$ | MAN.CODE<br>DEV.CODE |

NOTE: X can be $V_{IH}$ or $V_{IL}$ $V_H$ = 12V ±0.5V

## READ OPERATION
## DC AND AC CONDITIONS

| | F1/ – 2F1 – 3F1/ – 4F1 | – 25F1/ – 30F1/ – 45F1 | F6/ – 4F6 |
|---|---|---|---|
| Operating Temperature Range | 0 to 70°C | 0 to 70°C | – 40 to 85°C |
| $V_{CC}$ Power Supply (1,2) | 5V ±5% | 5V ±10% | 5V ±5% |
| $V_{PP}$ Voltage (2) | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ | $V_{PP} = V_{CC}$ |

## DC AND OPERATING CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. (3) | Max. | |
| $I_{LI}$ | Input Load Current | $V_{IN} = 5.5V$ | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = 5.5V$ | | | 10 | µA |
| $I_{PP1(2)}$ | $V_{PP}$ Current Read Standby | $V_{PP} = 5.5V$ | | | 5 | mA |
| $I_{CC1(2)}$ | $V_{CC}$ Current Standby | $\overline{CE} = V_{IH}$ | | 20 | 40 | mA |
| $I_{CC2(2)}$ | $V_{CC}$ Current Active | $\overline{CE} = \overline{OE} = V_{IL}$<br>$V_{PP} = V_{CC}$ | | 45 | 100 | mA |
| $V_{IL}$ | Input Low Voltage | | – 0.1 | | + 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC} + 1$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1$ mA | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -400$ µA | 2.4 | | | V |
| $V_{PP(2)}$ | $V_{PP}$ Read Voltage | $V_{CC} = 5V \pm 0.25V$ | 3.8 | | $V_{CC}$ | V |

## AC CHARACTERISTICS

| Symbol | Parameter | Test Conditions | 27256-2 | | 27256-25 / 27256 | | 27256-30 / 27256-3 | | 27256-45 / 27256-4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 200 | | 250 | | 300 | | 450 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE} = V_{IL}$ | | 200 | | 250 | | 300 | | 450 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | $\overline{CE} = V_{IL}$ | | 75 | | 100 | | 120 | | 150 | ns |
| $t_{DF(4)}$ | $\overline{OE}$ High to Output Float | $\overline{CE} = V_{IL}$ | 0 | 55 | 0 | 60 | 0 | 105 | 0 | 130 | ns |
| $t_{OH}$ | Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns |

## CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

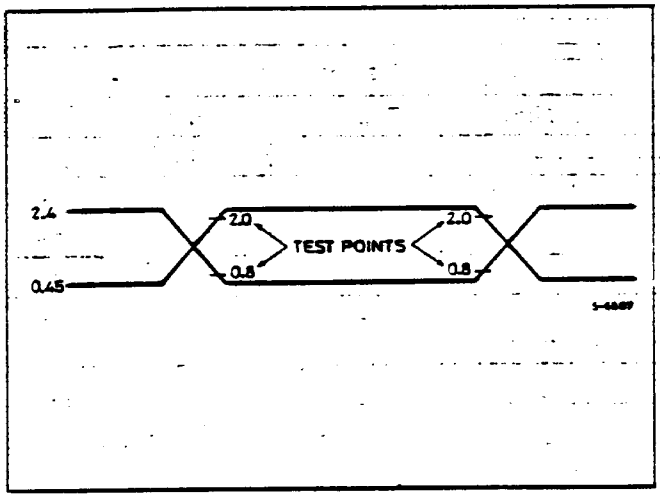
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | | 8 | 12 | pF |

**Notes:**
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would than be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

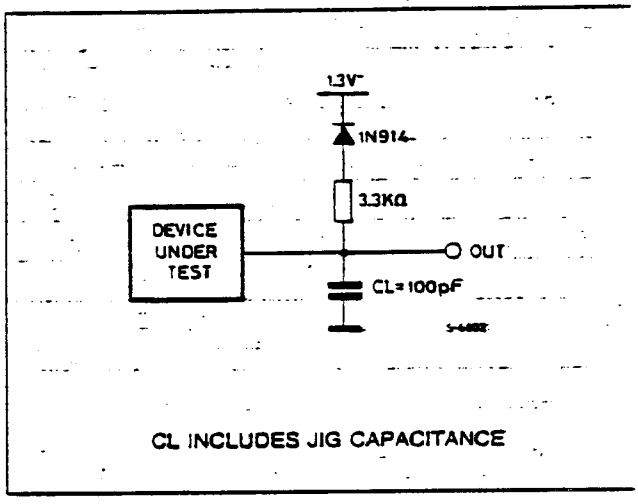
## AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

### AC TESTING INPUT/OUTPUT WAVEFORM

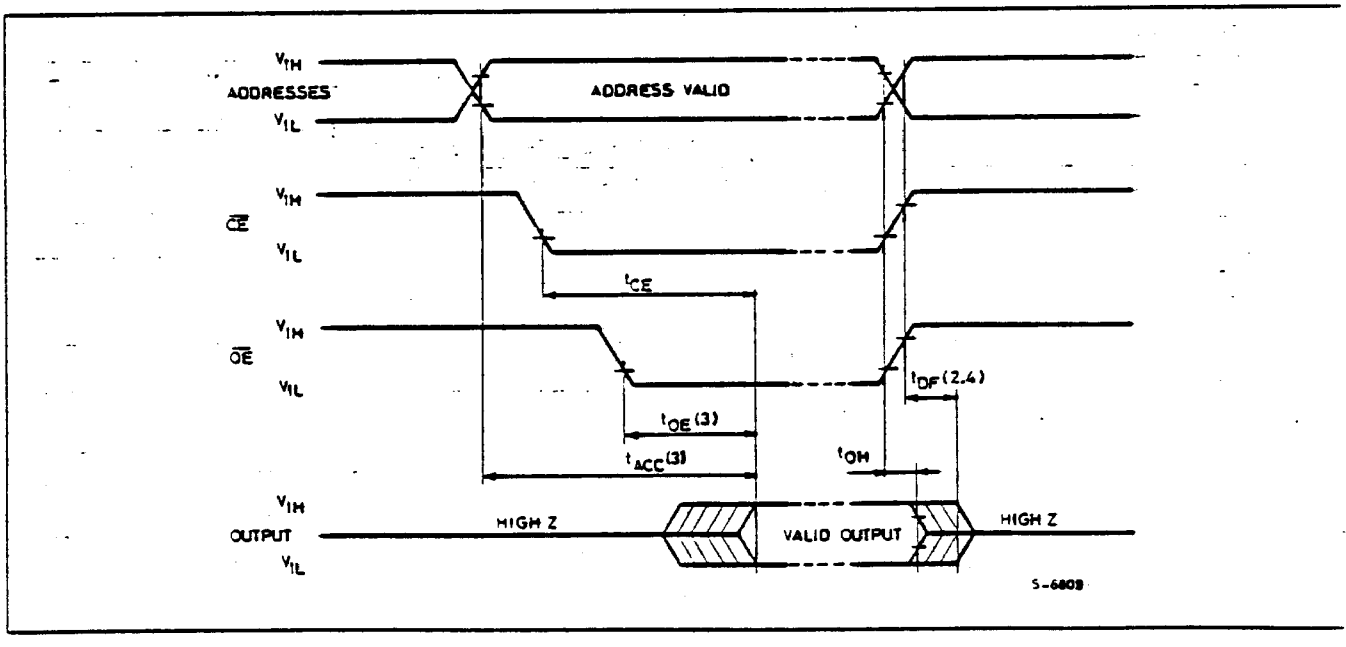



### AC TESTING LOAD CIRCUIT




CL INCLUDES JIG CAPACITANCE

### AC WAVEFORMS




**Notes:**
1. Typical values are for $T_{amb}$ = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on $t_{ACC}$.
4. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

## DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $V_{PP}$ and 12V on A9 for Electronic Signature.

### READ MODE

The M27256 has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}$-$t_{OE}$.

### STANDBY MODE

The M27256 has a standby mode which reduces the maximum active power current from 100 mA to 40 mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

### SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices the supply current, $I_{CC}$, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 $\mu$F ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 $\mu$F bulk electrolytic capacitors should be used between $V_{CC}$ and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PCB traces.

### PROGRAMMING

*Caution: exceeding 13V on pin 1 ($V_{PP}$) will damage the M27256.*

When delivered, and after each erasure, all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when $V_{PP}$ input is at 12.5V and $\overline{CE}$ and is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

### FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will than be followed by a

longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{CE}$ input, with $V_{PP}$ at 12.5V, will program that M27256. A high level $\overline{CE}$ input inhibits the other M27256s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at $V_{IL}$, $\overline{CE}$ at $V_{IH}$ and $V_{PP}$ at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at $V_{IL}$, $\overline{CE}$ at $V_{IL}$ (as opposed to the standard verify which has $\overline{CE}$ at $V_{IH}$), and $V_{PP}$ at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with $V_{PP} = 12.5V$ and $\overline{OE} = V_{IL}$ will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, $V_{PP}$ should be lowered to $V_{CC}$ (=6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to b programmed with its corresponding programmin algorithm. This mode is functional in the 25° ±5°C ambient temperature range that is require when programming the M27256. To activate thi mode, the programming equipment must forc 11.5V to 12.5V on address line A9 (pin 24) of th M27256. Two identifier bytes may than be sequenc ed from the device outputs by toggling address lin A0 (pin 10) from $V_{IL}$ to $V_{IH}$. All other address line must be held at $V_{IL}$ during Electronic Signatur mode. Byte 0 ($A0 = V_{IL}$) represents the manufac turer code and byte 1 ($A0 = V_{IH}$) the device ider tifier code. For the SGS M27256, these two ider tifier bytes are given below. All identifiers fc manufacturer and device codes will possess od parity, with the MSB (07) defined as the parity bi

ERASURE OPERATION

The erasure characteristic of the M27256 is suc that erasure begins when the cells are exposed t light with wavelengths shorter than approximatel 4000 Angstrom Å. It should be noted that sunligh and some type of fluorescent lamps hav wavelengths in the 3000-4000 A range. Data show that constant exposure to room level fluorescen lighting could erase a typical M27256 in about years, while it would take approximately 1 week t cause erasure when expose to direct sunlight. the M27256 is to be exposed to these type c lighting conditions for extended periods of time, is suggested that opaque labels to put over th M27256 window to prevent unintentional erasure The recommended erasure procedure for th M27256 is exposure to short wave ultraviolet ligh which has wavelength 2537 Å. The integrated dos (i.e. UV intensity x exposure time) for erasur should be a minimum of 15 W-sec/cm². Th erasure time with this dosage is approximately 1 to 20 minutes using an ultraviolet lamp with 1200 µW/cm² power rating. The M27256 should be plac ed within 2.5 cm (1 inch) of the lamp tubes durin the erasure. Some lamps have a filter on their tube which should be removed before erasure.

**ELECTRONIC SIGNATURE MODE**

| PINS / IDENTIFIER | A0 (10) | O7 (19) | O6 (18) | O5 (17) | O4 (16) | O3 (15) | O2 (13) | O1 (12) | O0 (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer code | $V_{IL}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| Device code | $V_{IH}$ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |

## PROGRAMMING OPERATION ($T_{amb}$ = 25°C ±5°C, $V_{CC}$(1) = 6V ±0.25V, $V_{PP}$(1) = 12.5V ±0.3V

### DC AND OPERATING CHARACTERISTIC:

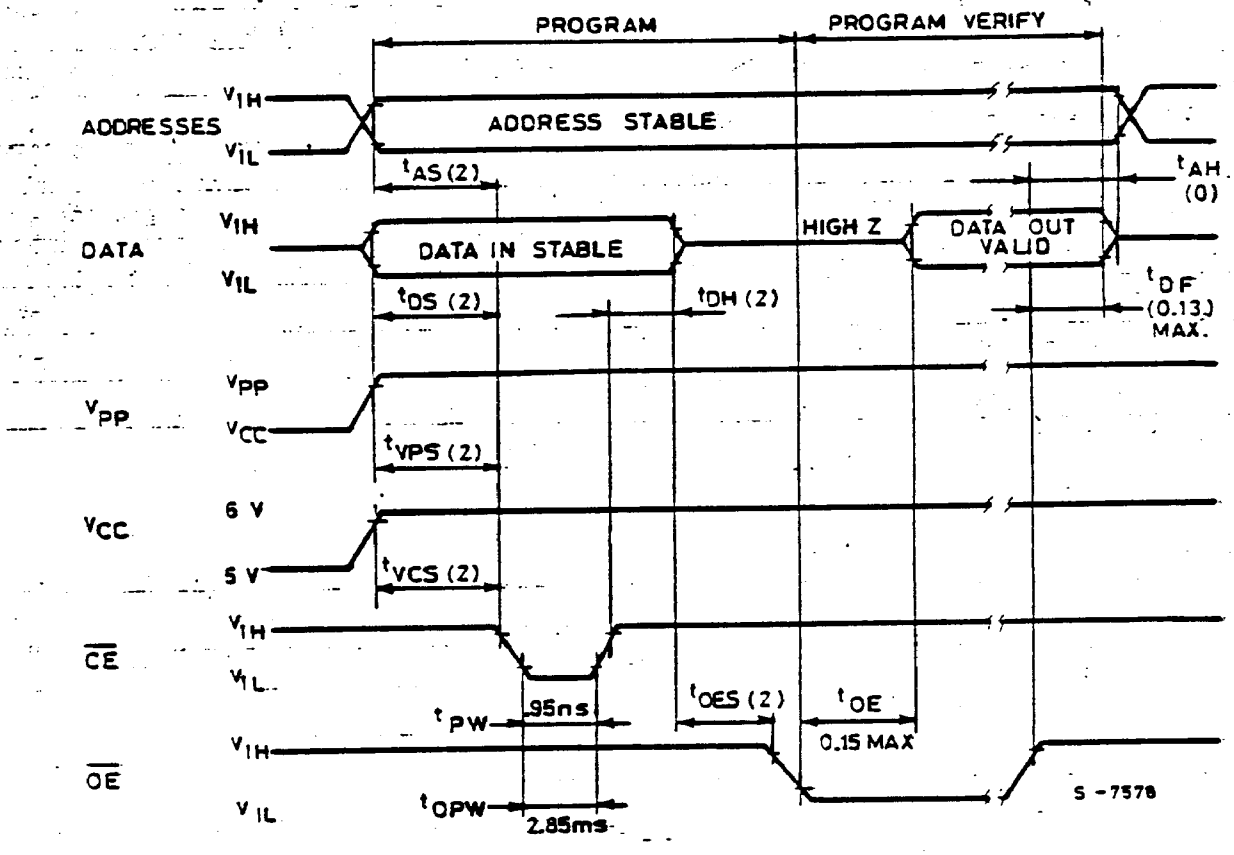
| Symbol | Parameter | Test Conditions (See note 1) | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | µA |
| $V_{IL}$ | Input Low Level (All Inputs) | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL}$ = 2.1 mA | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = −400 µA | 2.4 | | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program & Verify) | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | $\overline{CE} = V_{IL}$ | | | 50 | mA |
| $V_{ID}$ | A9 Electronic Signature Voltage | | 11.5 | | 12.5 | V |

### AC CHARACTERISTICS

| Symbol | Parameter | Test Conditions (See note 1) | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{AS}$ | Address Setup Time | | 2 | | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | | µs |
| $t_{DH}$ | Data Hodl Time | | 2 | | | µs |
| $t_{DFP}$(4) | Output Enable Output Float Delay | | 0 | | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | | µs |
| $t_{PW}$ | $\overline{CE}$ Initial Program Pulse Width | (see Note 3) | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{CE}$ Overprogram Pulse Width | (see Note 2) | 2.85 | | 78.75 | ms |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | | 150 | ns |

**Notes:**
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

## PROGRAMMING WAFEFORMS




**Notes:**

1. All times shown in ( ) are minimum and in usec unless otherwise specified.
2. The input timing reference level is 0.8V for a $V_{IL}$ and 2V for a $V_{IH}$
3. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer
4. When programming the M27256 a 0.1$\mu$F capacitor is required across $V_{PP}$ and GROUND to suppress spurious voltage transients whi can damage the device.

## FAST PROGRAMMING FLOWCHART