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TECHNICAL DATA

MC68HC711D3

Technical Summary
8-Bit Microcontroller

Introduction

The MC68HC711D3 high-performance microcontroller unit (MCU) is a simplified erasable programmable ROM (EPROM)-based derivative of the MC68HC11E9 with 4K bytes of EPROM and 192 bytes of RAM. It is a high-speed, low power consumption chip with a multiplexed bus and a fully static design. The chip runs at frequencies from 3 MHz to dc and is an economical alternative for applications where the HC11 CPU is necessary, but fewer peripheral functions and less memory are required.

For more detailed information on subsystems, programming and the instruction set, refer to the *M68HC11 Reference Manual*, document number M68HC11 RM/AD.

Features

- MC68HC11 CPU
- Power Saving STOP and WAIT Modes
- 4K Bytes of On-Chip EPROM or One-Time Programmable Read-Only Memory (OTPROM)
- 192 Bytes of On-Chip RAM (All Saved During Standby)
- 16-Bit Timer System
  - 3 Input Capture (IC) Channels/4 Output Compare (OC) Channels
  - Additional Channel; Software Selectable as either Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- 32 General-Purpose Input/Output (I/O) Pins
  - 26 Bidirectional Input/Output (I/O) Pins
  - 3 Input-Only Pins and 3 Output-Only Pins (One Output-Only Pin in 40-Pin DIP)
- Available in a Variety of Packages
  - 44-Pin Plastic Leaded Chip Carrier (OTPROM)
  - 40-Pin Plastic Dual In-Line Package (OTPROM)
  - 44-Pin Windowed Ceramic Leaded Chip Carrier (EPROM)
  - 40-Pin Windowed Ceramic Dual In-Line Package (EPROM)

Ordering Information

		MC Order Number	
Package	**Temperature**	**Ceramic (EPROM)**	**Plastic (OTPROM)**
40-Pin DIP	–40° to +85° C	MC68HC711D3S	MC68HC711D3P
44-Pin Quad	–40° to +85°C	MC68HC711D3FS	MC68HC711D3FN

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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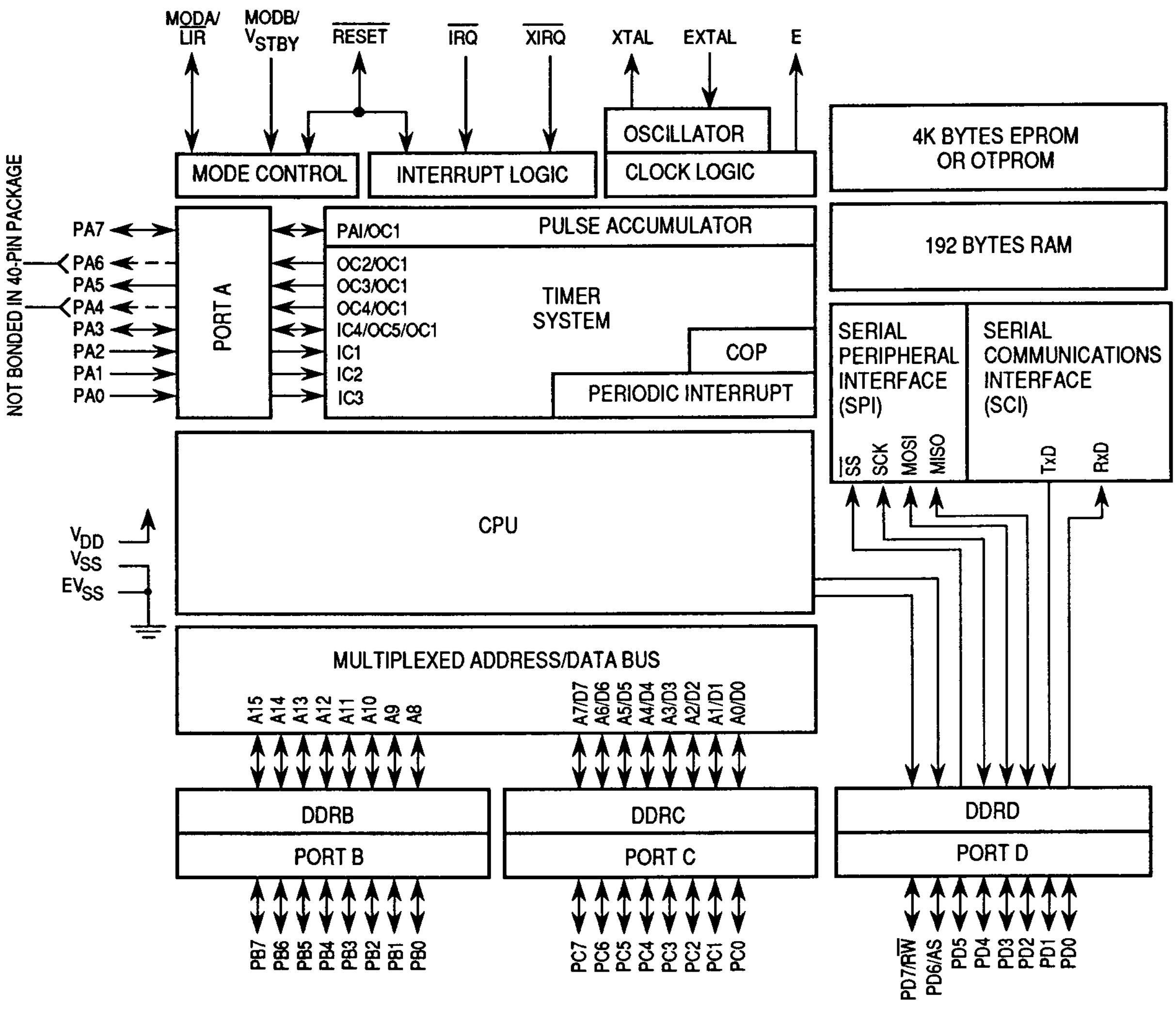
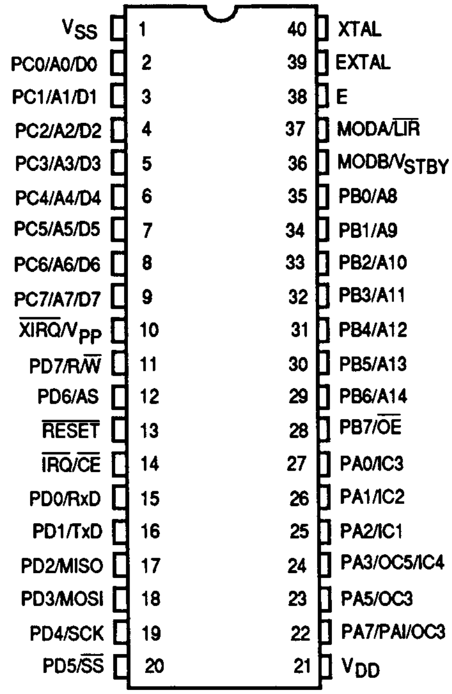
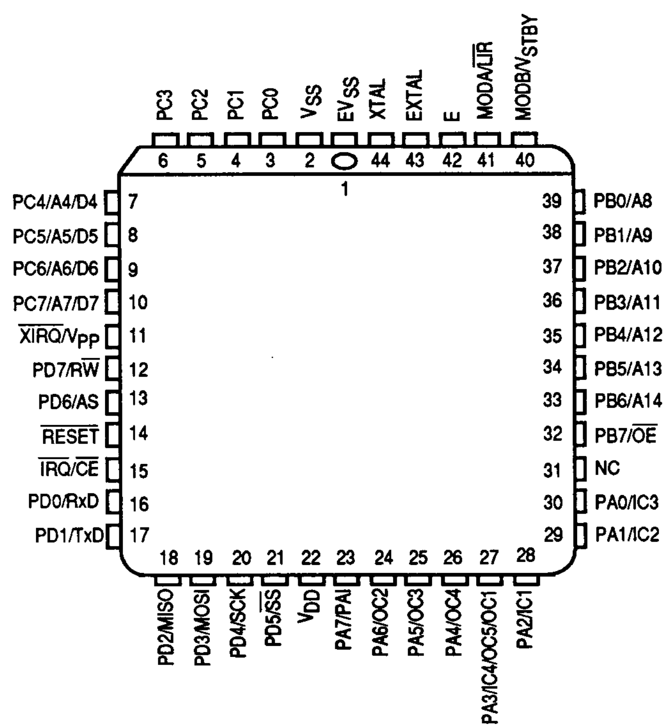


Block Diagram



Pin Assignments for 40-Pin DIP

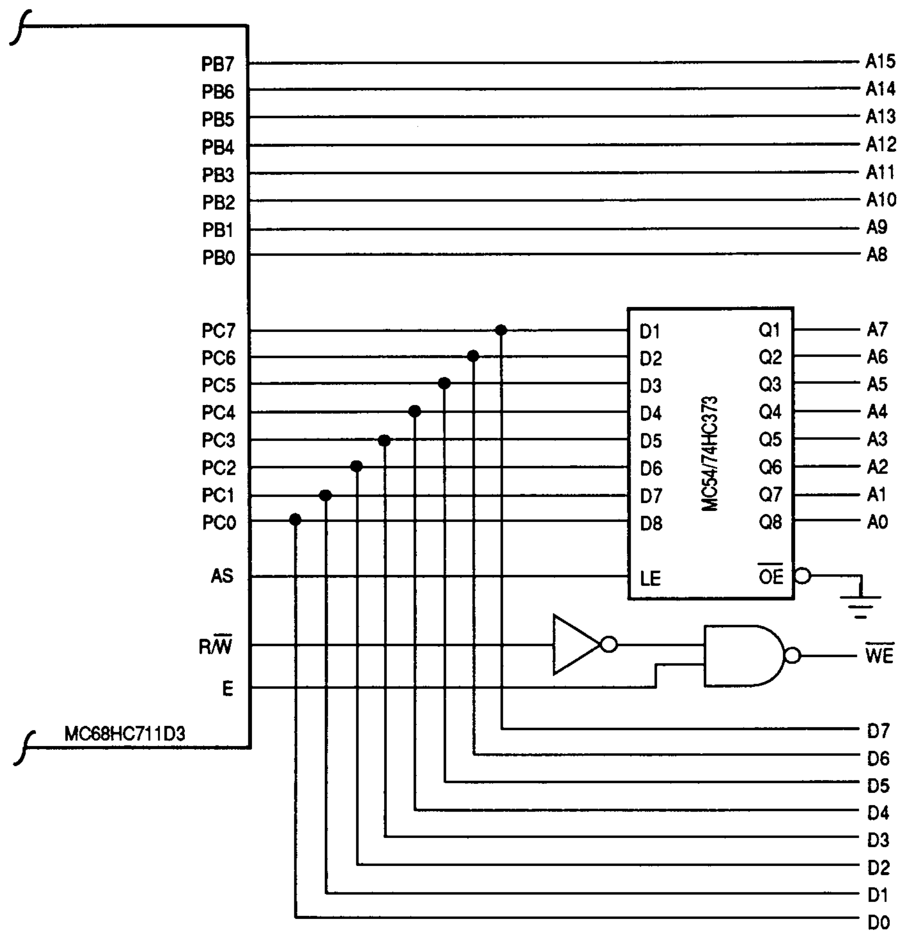


Pin Assignments for 44-Pin PLCC

Operating Modes

In single-chip operating mode, the MC68HC711D3 is a monolithic microcontroller without external address or data buses.

In expanded multiplexed operating mode, the MCU can access a 64K-byte address space. The space includes the same on-chip memory addresses used for single-chip mode, in addition to external peripheral and memory devices. The expansion bus is composed of ports B and C, and control signals AS and R/$\overline{W}$. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles, including accesses to internal memory locations. The following figure illustrates a recommended method of demultiplexing low order addresses from data at port C.



Address/Data Demultiplexing

Special bootstrap mode allows special purpose programs to be entered into internal RAM. The bootloader program uses the SCI to read up to a 192-byte program into on-chip RAM at $0040 through $00FF. After receiving the character for address $00FF, or a 4-character delay (to allow a variable length download), control passes to the program loaded at $0040.

Special test mode is used primarily for factory testing.

Memory Maps

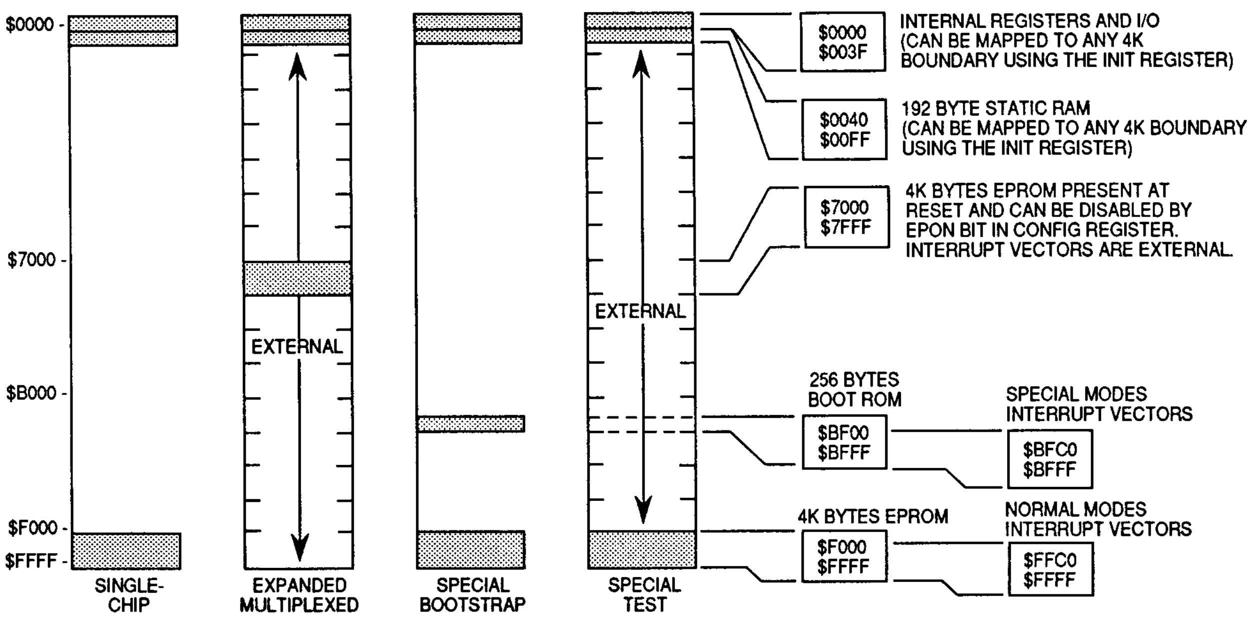
Memory locations are the same for expanded multiplexed and single-chip modes, except for EPROM/OTPROM in expanded mode, and the bootloader ROM in bootstrap mode. The on-board 192-byte RAM is initially located at $0040 after reset, but can be placed at any other 4K boundary ($x040) by writing an appropriate value to the INIT register. The 64-byte register block originates at $0000 after reset, but can be placed at any other 4K boundary ($x000) after reset by writing an appropriate value to the INIT register.

The 4K-byte EPROM is located at $F000 through $FFFF in all modes except expanded multiplexed, where it is located at $7000. The EPROM can be located at $F000 in expanded multiplexed mode by entering single-chip mode out of reset and setting the MDA bit in the HPRIO register to 1, thereby entering expanded mode from internal ROM. The EPROM can be removed from the memory map in all modes except single chip by writing the EPON bit in the CONFIG register to zero.

Hardware priority is built into the memory remapping. Registers and RAM have priority over EPROM; in case of conflicts, the higher priority resource covers the lower, making the underlying locations inaccessible.

In special bootstrap mode, a bootloader ROM is enabled at locations $BF40 through $BFFF.

In special test and special bootstrap modes, reset and interrupt vectors are located at $BFC0 through $BFFF.



Memory Map

MC68HC711D3 Registers (1 of 2)

(The register block can be remapped to any 4K boundary)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Register
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001									Reserved
$0002			CWOM						PIOC
$0003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$0004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$0005									Reserved
$0006	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
$0007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$0008	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$0009	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$000A									Reserved
$000B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$000C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$000D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$000E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$000F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$0010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$0011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$0012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$0013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$0014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (High)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$001C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$001D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)

MC68HC711D3 Registers (2 of 2)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Register
$001E	Bit 15	14	13	12	11	10	9	Bit 8	TI4O5 (High)
$001F	Bit 7	6	5	4	3	2	1	Bit 0	TI4O5 (Low)
$0020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$0021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$0022	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I	TMSK1
$0023	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F	TFLG1
$0024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$0025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$0026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$0027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$0028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$0029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$002A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$002B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$002C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$002D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$002E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$002F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$0030									Reserved
to									
$0038									Reserved
$0039	0	0	IRQE	DLY	CME	0	CR1	CR0	OPTION
$003A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$003B	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM	PPROG
$003C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$003D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$003E	TILOP	EPTST	OCCR	CBYP	DISR	FCM	FCOP	0	TEST1
$003F	0	0	0	0	0	NOCOP	EPON	0	CONFIG

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$003C**

	Bit 7	6	5	4	3	2	1	Bit 0	
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	
RESETS:									
	0	0	0	0	0	1	0	1	Single-Chip Mode
	0	0	1	0	0	1	0	1	Exp'd-NonMux'd
	1	1	0	0	0	1	0	1	Bootstrap
	0	1	1	1	0	1	0	1	Special Test

RBOOT, SMOD, MDA, and IRVNE reset depend on mode selected at power-up.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set to one (special bootstrap or special test mode). Can only be written in special modes.

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BF40–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time. They reflect the status of the MODB and MODA pins at the rising edge of reset. SMOD can only be written in special modes; MDA can be written at any time in special modes, but only once in normal modes.

Inputs		Mode	Latched at Reset		
MODB	MODA		RBOOT	SMOD	MDA
1	0	Single-Chip	0	0	0
1	1	Expanded Multiplexed	0	0	1
0	0	Special Bootstrap	1	1	0
0	1	Special Test	0	1	1

IRVNE — Internal Read Visibility/Not E (IRVNE can be written once in any mode.)

In expanded modes IRVNE determines whether IRV is on or off. In special test mode IRVNE is set to 1, and in all other modes IRVNE is reset to 0.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out the external data bus

In single-chip modes this bit determines whether the E-clock drives out of the chip.

0 = E is driven out from the chip

1 = E pin is driven low

Mode	IRVNE Out of Reset	E-Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only
Single-Chip	0	On	Off	E
Expanded	0	On	Off	IRV
Bootstrap	0	On	Off	E
Special Test	1	On	On	IRV

Bits 3–0 — Refer to **Resets and Interrupts**.

INIT — RAM and I/O Mapping **$003D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	0

RAM3–RAM0 — 192-Byte Internal RAM Map Position

RAM3–RAM0 determine the upper four bits of the RAM address, positioning RAM at the selected 4K boundary ($x040).

REG3–REG0 — 64-Byte Register Block Map Position

REG3–REG0 determine the upper four bits of the register address, positioning registers at the selected 4K boundary ($x000).

NOTE

Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes. Refer to **Operating Modes** and **Memory Maps** for more information.

TEST1 — Factory Test **$003E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	EPTST	OCCR	CBYP	DISR	FCM	FCOP	0
RESET:	0	0	0	0	—	0	0	0

Test Modes Only

TILOP — Test Illegal Opcode

EPTST — EPROM Test

OCCR — Output Condition Code Register to Timer Port (and Ports D4 and D5 on 40-Pin DIP)

CBYP — Timer Divider Chain Bypass

DISR — Disable Resets from COP and Clock Monitor

FCM — Force Clock Monitor Failure

FCOP — Force COP Watchdog Failure

Bit 0 — Not implemented; always read zero

CONFIG — ROM Mapping, COP, ROM, Enables **$003F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET:	0	0	0	0	0	—	1	0

Bits 7–3 and 0 — Not implemented; always read zero

Bit 2 — Refer to **Resets and Interrupts**.

EPON — EPROM Enable

Set out of reset, enabling EPROM (OTPROM) in all modes. Writable once in normal modes and writable at any time in special modes.

0 = EPROM removed from the memory map

1 = EPROM present in the memory map

NOTE

In expanded mode, the EPROM is located at $7000–$7FFF out of reset. In all other modes, the EPROM is located at $F000–$FFFF.

Resets and Interrupts

The MC68HC711D3 has 3 reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 22 interrupt sources, 3 non-maskable and 19 maskable. The 3 non-maskable interrupt vectors are as follows:

- Illegal Opcode Trap
- Software Interrupt
- $\overline{\text{XIRQ}}$ Pin (Pseudo Non-Maskable Interrupt)

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Nineteen interrupt sources in the MC68HC711D3 are subject to masking. Maskable interrupts are prioritized according to a default arrangement. Any source, however, can be elevated to the highest maskable priority position by a software-accessible control register (HPRIO). The HPRIO register can be written at any time, provided the I-bit in the CCR is set.

In addition to the global I-bit, all of these sources, except the external interrupt ($\overline{\text{IRQ}}$ pin), are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors and there is usually no need for software to poll control registers to determine the cause of an interrupt. Refer to the following list of interrupt and reset vector assignments.

Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I-Bit	—
	SCI Transmit Complete		TCIE
	SCI Transmit Data Register Empty		TIE
	SCI Idle Line Detect		ILIE
	SCI Receiver Overrun		RIE
	SCI Receive Data Register Full		RIE
FFD8, D9	SPI Serial Transfer Complete	I-Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I-Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I-Bit	PAOVI
FFDE, DF	Timer Overflow	I-Bit	TOI
FFE0, E1	Timer Input Capture 4/Output Compare 5	I-Bit	I4O5I
FFE2, E3	Timer Output Compare 4	I-Bit	OC4I
FFE4, E5	Timer Output Compare 3	I-Bit	OC3I
FFE6, E7	Timer Output Compare 2	I-Bit	OC2I
FFE8, E9	Timer Output Compare 1	I-Bit	OC1I
FFEA, EB	Timer Input Capture 3	I-Bit	IC3I
FFEC, ED	Timer Input Capture 2	I-Bit	IC2I
FFEE, EF	Timer Input Capture 1	I-Bit	IC1I
FFF0, F1	Real-Time Interrupt	I-Bit	RTII
FFF2, F3	$\overline{IRQ}$ (External Pin)	I-Bit	None
FFF4, F5	$\overline{XIRQ}$ Pin	I-Bit	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	$\overline{RESET}$	None	None

For some interrupt sources, such as the SCI interrupts, flags are automatically cleared during the response to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism, consisting of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request is to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

OPTION — System Configuration Options **$0039**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

Bits 7, 6, and 2 — Not implemented; always read zero

IRQE — $\overline{IRQ}$ Select Edge Sensitive Only
0 = Low level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

CR1, CR0 — COP Timer Rate Select

COP Timer Rate Select

CR [1:0]	Divide E/2^{15} By	XTAL = 4.0 MHz Timeout −0/+32.8 ms	XTAL = 8.0 MHz Timeout −0/+16.4 ms	XTAL = 12.0 MHz Timeout −0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.07 ms	65.536 ms	43.691 ms
1 0	16	524.29 ms	262.14 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

COPRST — Arm/Reset COP Timer Circuitry **$003A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$003C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

Bits 7–4 — Refer to **Operating Modes** and **Memory Maps**.

PSEL3–PSEL0 — Priority Select Bits 3–0

Writable only while the I-bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSEL [3:0]	Interrupt Source Promoted
0000	Timer Overflow
0001	Pulse Accumulator Overflow
0010	Pulse Accumulator Input Edge
0011	SPI Serial Transfer Complete
0100	SCI Serial System
0101	Reserved (Default to $\overline{\text{IRQ}}$)
0110	$\overline{\text{IRQ}}$ (External Pin)
0111	Real-Time Interrupt
1000	Timer Input Capture 1
1001	Timer Input Capture 2
1010	Timer Input Capture 3
1011	Timer Output Compare 1
1100	Timer Output Compare 2
1101	Timer Output Compare 3
1110	Timer Output Compare 4
1111	Timer Output Compare 5/Input Capture 4

CONFIG — ROM Mapping, COP, ROM, Enables **$003F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET:	0	0	0	0	0	—	1	0

Bits 7–3 and 0 — Not implemented; always read zero

NOCOP — COP system disable

Cleared out of reset in normal modes, enabling COP system. Set out of reset in special modes. Writable once in normal modes and writable at any time in special modes.

0 = COP enabled (forces reset on timeout)

1 = COP disabled (does not force reset on timeout)

Bit 1 — Refer to **Operating Modes** and **Memory Maps.**

Erasable Programmable Read-Only Memory (EPROM)

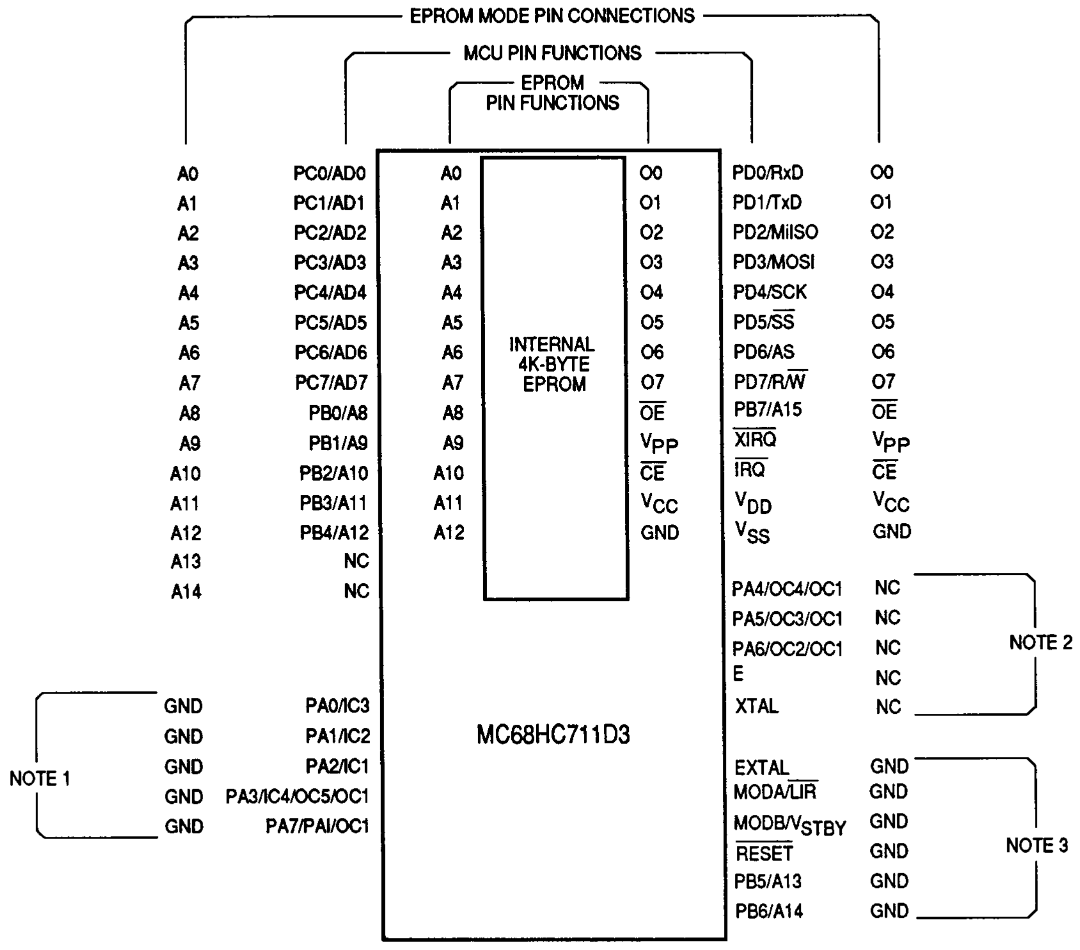
The MC68HC711D3 has 4K bytes of ultraviolet (UV) erasable programmable read-only memory. The 4K-byte EPROM is located at $F000 through $FFFF in all modes except expanded multiplexed, where it is located at $7000. The EPROM can be located at $F000 in expanded multiplexed mode by entering single-chip mode out of reset and setting the MDA bit in the HPRIO register to one, thereby entering expanded mode from internal ROM. The EPROM can be removed from the memory map in all modes except single-chip by writing the EPON bit in the CONFIG register to zero.

Programming EPROM requires an external 12.25-volt nominal power supply (V_{PP}). There are two methods used to program and verify EPROM:

1. In PROG mode, the EPROM is programmed as a stand-alone by adapting the MCU footprint to the 27256-type EPROM and using an appropriate EPROM programmer.

2. In normal MCU mode, the EPROM can be programmed in any operating mode. Special test and bootstrap modes are preferred, however. Normal programming is accomplished using the PPROG register.

The EPON bit in the CONFIG register enables or disables the EPROM in the internal memory map. The erased state of EPROM is $FF (all ones).



NOTES:
1. Unused inputs — grounding is recommended.
2. Unused outputs — these pins should be left unterminated.
3. These pins must be grounded for PROG mode.

MC68HC711D3 Block Diagram — PROG Mode

PPROG — EPROM Programming Control **$003B**

	Bit 7	6	5	4	3	2	1	Bit 0
	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM
RESET:	0	0	0	0	0	0	0	0

MBE — Multiple Byte Program Enable (TEST)

Bits 6 and 2 –1 — Not implemented; always read zero

ELAT — EPROM (OTPROM) Latch Control
- 0 = EPROM address and data bus configured for normal reads and cannot be programmed
- 1 = EPROM address and data bus configured for programming and cannot be read

EXCOL — Select Extra Columns (TEST)

EXROW — Select Extra Row (TEST)

PGM — EPROM (OTPROM) Program Command
- 0 = Programming voltage switched off to EPROM array
- 1 = Programming voltage switched on to EPROM array

CONFIG — ROM Mapping, COP, ROM, Enables **$003F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET:	0	0	0	0	0	—	1	0

Bits 7–3 and 0 — Not implemented; always read zero

Bit 2 — Refer to **Resets and Interrupts**.

EPON — EPROM Enable

Set out of reset, enabling EPROM (OTPROM) in all modes. Writable once in normal modes and writable at any time in special modes.
- 0 = EPROM removed from the memory map
- 1 = EPROM present in the memory map

NOTE

In expanded mode, the EPROM is located at $7000–$7FFF out of reset. In all other modes, the EPROM is located at $F000–$FFFF.

Parallel Input/Output

The MC68HC711D3 has four 8-bit I/O ports — A, B, C, and D. In the 40-pin package, port A bits 4 and 6 are not connected to pins. In single-chip and bootstrap modes, all ports are parallel I/O data ports. In expanded multiplexed and test modes, ports B and C and lines D6/AS and D7/R/$\overline{W}$ are a memory expansion bus with port B serving as the high-order address bus; port C as the multiplexed address and data bus; AS as the demultiplexing signal; and R/$\overline{W}$ as the data bus direction control.

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	3	3	2	Timer
Port B	—	—	8	High Order Address
Port C	—	—	8	Low Order Address and Data Bus
Port D	—	—	8	SCI, SPI, AS, andR/$\overline{W}$

PORTA — Port A Data **$0000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	HiZ	0	0	0	HiZ	HiZ	HiZ	HiZ
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PIOC — Parallel I/O Control **$0002**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	CWOM	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

CWOM — Port C Wire-OR Mode (affects all eight Port C pins)
- 0 = Port C outputs are normal CMOS outputs
- 1 = Port C outputs are open-drain outputs

PORTC — Port C Data **$0003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	Reset configures pins as HiZ inputs							
Expan. or Test:	A7/D7	A6/D6	A5/D5	A4/D4	A3/D3	A2/D2	A1/D1	A0/D0
RESET:	Reset configures pins as multiplexed, low-order address/data I/O							

PORTB — Port B Data **$0004**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	Reset configures pins as HiZ inputs							
Expan. or Test:	A15	A14	A13	A12	A11	A10	A9	A8
RESET:	Reset configures pins as high-order address outputs							

DDRB — Data Direction Register for Port B **$0006**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RESET:	0	0	0	0	0	0	0	0

DDB7–DDB0 — Data Direction for Port B
- 0 = Configure corresponding I/O pin for input
- 1 = Configure corresponding I/O pin for output

DDRC — Data Direction Register for Port C **$0007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC7–DDC0 — Data Direction for Port C
- 0 = Configure corresponding I/O pin for input
- 1 = Configure corresponding I/O pin for output

PORTD — Port D Data **$0008**

	Bit 7	6	5	4	3	2	1	Bit 0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	Reset configures pins as HiZ inputs							
Alt. Pin Func.:	$R/\overline{W}$	AS	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Data Direction Register for Port D **$0009**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

In expanded modes, Port D bits 6 and 7 are AS and $R/\overline{W}$ outputs.

DDD7–DDD0 — Data Direction for Port D
0 = Configure corresponding I/O pin for input
1 = Configure corresponding I/O pin for output

PACTL — Pulse Accumulator Control **$0026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
0 = Input only
1 = Output

Bits 6–4 — Refer to **Pulse Accumulator.**

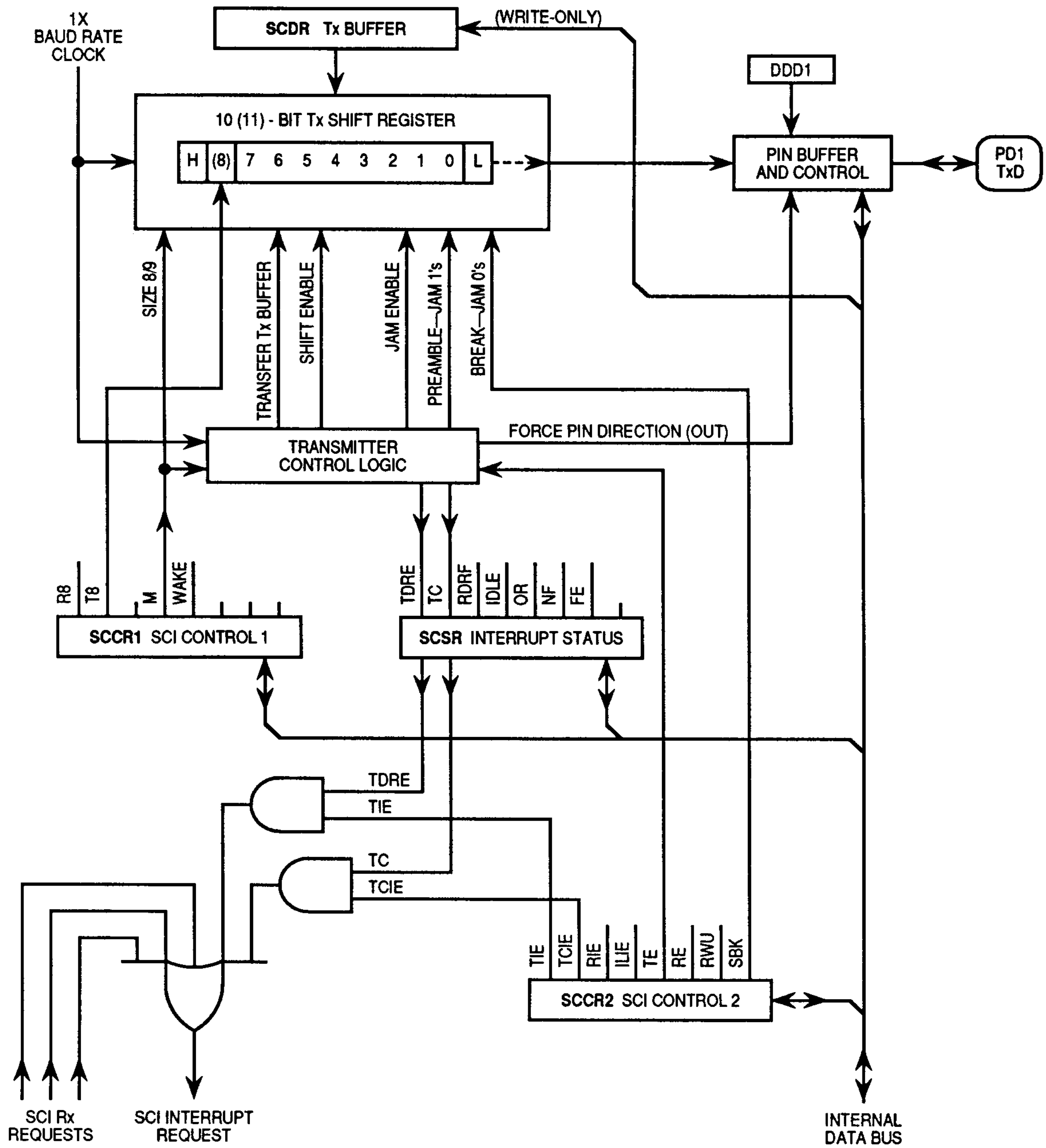
DDRA3 — Data Direction for Port A Bit 3
0 = Input only
1 = Output

I4/O5 — Input Capture 4 or Output Compare 5 (IC4 or OC5)
0 = OC5 (No IC4)
1 = IC4 (No OC5)

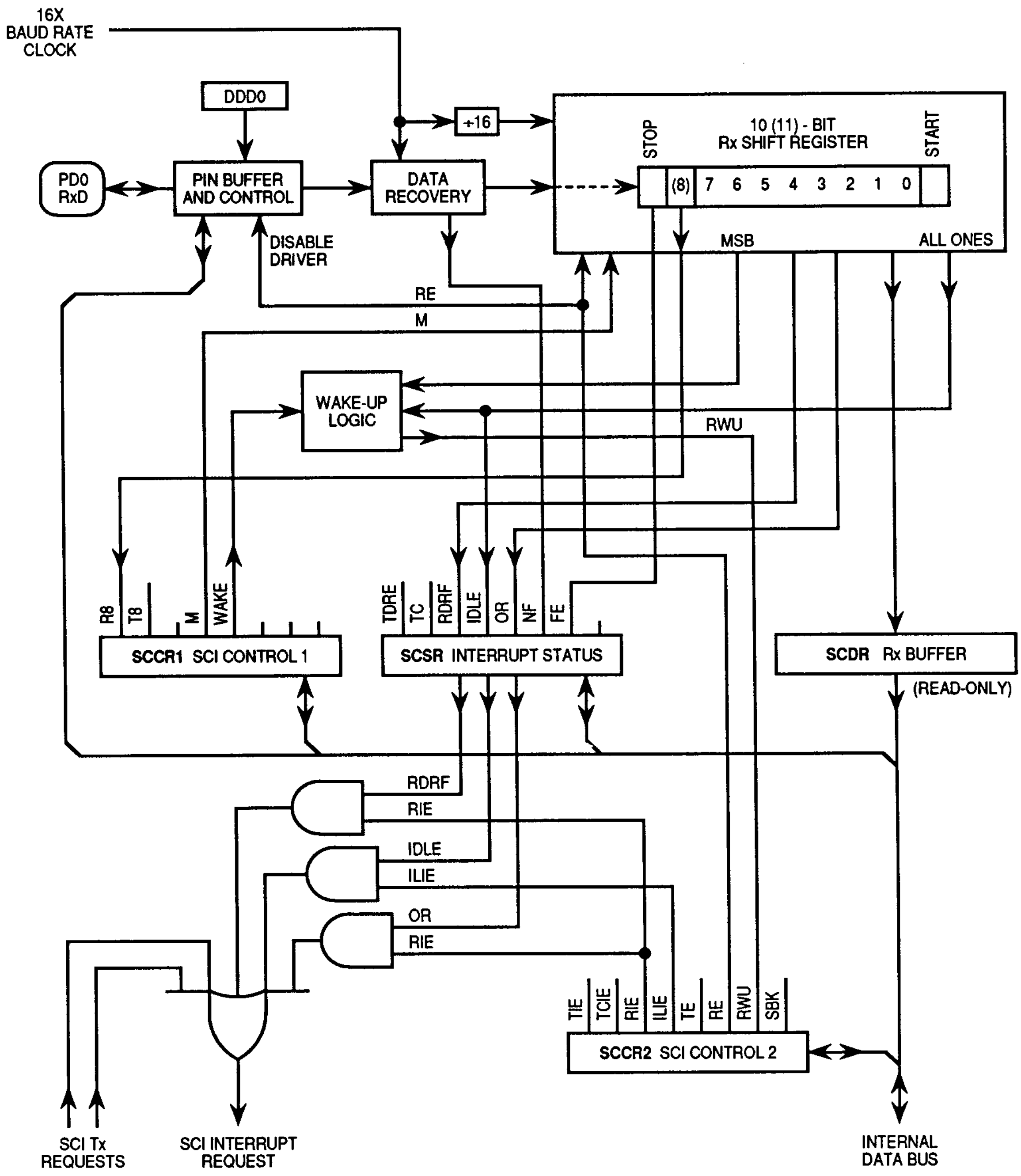
Bits 1–0 — Refer to **Main Timer.**

Serial Communications Interface (SCI)

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is one of two independent serial I/O subsystems in the MC68HC711D3. It has a standard nonreturn to zero (NRZ) format (one start, eight or nine data and one stop bit) with several baud rates available. The SCI transmitter and receiver are independent, but use the same data format and bit rate.



SCI Transmitter Block Diagram



SCI Receiver Block Diagram

SPCR — Serial Peripheral Control **$0028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

Bits 7–6 and 4–0 — Refer to **Serial Peripheral Interface (SPI).**

DWOM — Port D Wired-OR Mode Option for Pins PD5–PD0
0 = Normal CMOS outputs
1 = Open-drain outputs

BAUD — Baud Rate **$002B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)

Bit 6 — Not implemented; this bit always reads zero

SCP1, SCP0 — SCI Baud Rate Prescaler Selects
Refer to the baud rate prescaler and baud rate selection tables.

RCKB – SCI Baud-Rate Clock Check (TEST)

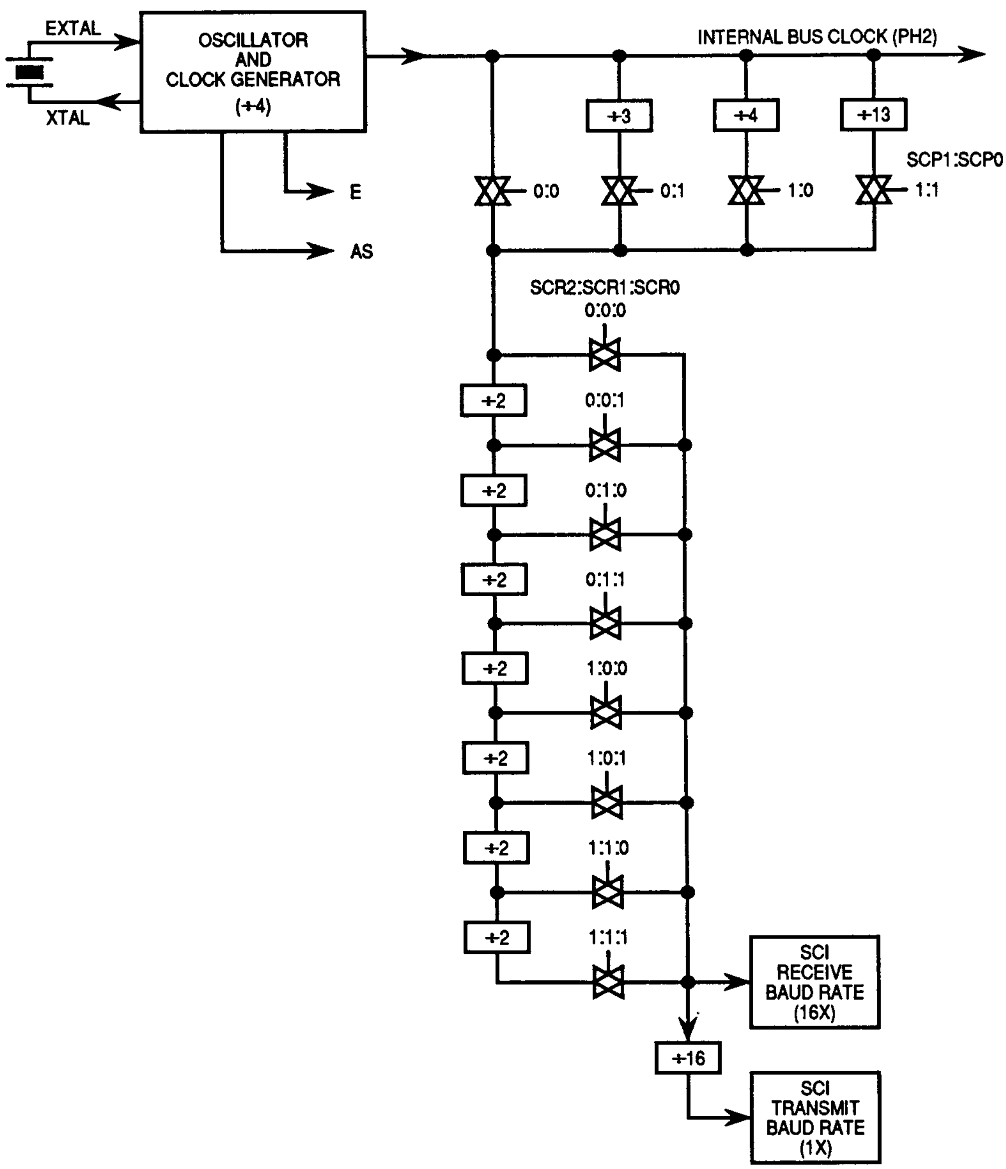
SCR2, SCR1, and SCR0 — SCI Baud Rate Selects
Selects receiver and transmitter baud rate. Refer to the schematic of the baud rate clock divider chain.

Baud-Rate Prescaler Sets Highest Rate

SCP [1:0]	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
0 0	1	62.50K	125.0K	156.25K	187.5K
0 1	3	20.83K	41.67K	52.08K	62.5K
1 0	4	15.625K	31.25K	38.4K	46.88K
1 1	13	4800	9600	12.02K	14.42K

Baud Rate Selection Table

SCR [2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)		
		4800	9600	38.4K
0 0 0	1	4800	9600	38.4K
0 0 1	2	2400	4800	19.2K
0 1 0	4	1200	2400	9600
0 1 1	8	600	1200	4800
1 0 0	16	300	600	2400
1 0 1	32	150	300	1200
1 1 0	64	—	150	600
1 1 1	128	—	—	300



Baud Rate Clock Diagram

SCCR1 — SCI Control 1 **$002C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	0	M	WAKE	0	0	0
RESET:	0	0	0	0	0	0	0	0

R8 — Receive Data Bit 8
If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data Bit 8
If M bit is set, T8 stores ninth bit in transmit data character.

Bits 5 and 2–0 — These bits are not implemented; always read zero.

M — Mode (Select Character Format)
0 = Start, 8 data bits, 1 stop bit
1 = Start, 9 data bits, 1 stop bit

WAKE — Wake-Up by Address Mark/Idle
0 = Wake-up by IDLE line recognition
1 = Wake-up by address mark (most significant data bit set)

SCCR2 — SCI Control 2 **$002D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
- 0 = TDRE interrupts disabled
- 1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
- 0 = TC interrupts disabled
- 1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
- 0 = RDRF and OR interrupts disabled
- 1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
- 0 = IDLE interrupts disabled
- 1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable

When TE goes from zero to one, one unit of idle character time (logic one) is queued as a preamble.
- 0 = Transmitter disabled
- 1 = Transmitter enabled

RE — Receiver Enable
- 0 = Receiver disabled
- 1 = Receiver enabled

RWU — Receiver Wake-Up Control
- 0 = Normal SCI receiver
- 1 = Wake-up enabled and inhibits receiver interrupts

SBK — Send Break
- 0 = Break generator off
- 1 = Break codes generated as long as SBK = 1

SCSR — SCI Status **$002E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag

Set if transmit data can be written to SCDR; if TDRE = 0, transmit data register is busy. Cleared by SCSR read with TDRE set, followed by SCDR write.

TC — Transmit Complete Flag

Set if transmitter is idle (no data, preamble, or break transmission in progress). Cleared by SCSR read with TC set, followed by SCDR write.

RDRF — Receive Data Register Full Flag

Set if a received character is ready to be read from SCDR. Cleared by SCSR read with RDRF set, followed by SCDR read.

IDLE — Idle Line Detected Flag

Set if the RxD line is idle. Cleared by SCSR read with IDLE set, followed by SCDR read. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again.

OR — Overrun Error Flag

Set if a new character is received before a previously received character is read from SCDR. Cleared by SCSR read with OR set, followed by SCDR read.

NF — Noise Error Flag

Set if majority sample logic detects anything other than a unanimous decision. Cleared by SCSR read with NF set, followed by SCDR read.

FE — Framing Error

Set if a 0 is detected where a stop bit was expected. Cleared by SCSR read with FE set, followed by SCDR read.

Bit 0 — Not implemented; this bit always reads zero.

SCDR — SCI Data Register **$002F**

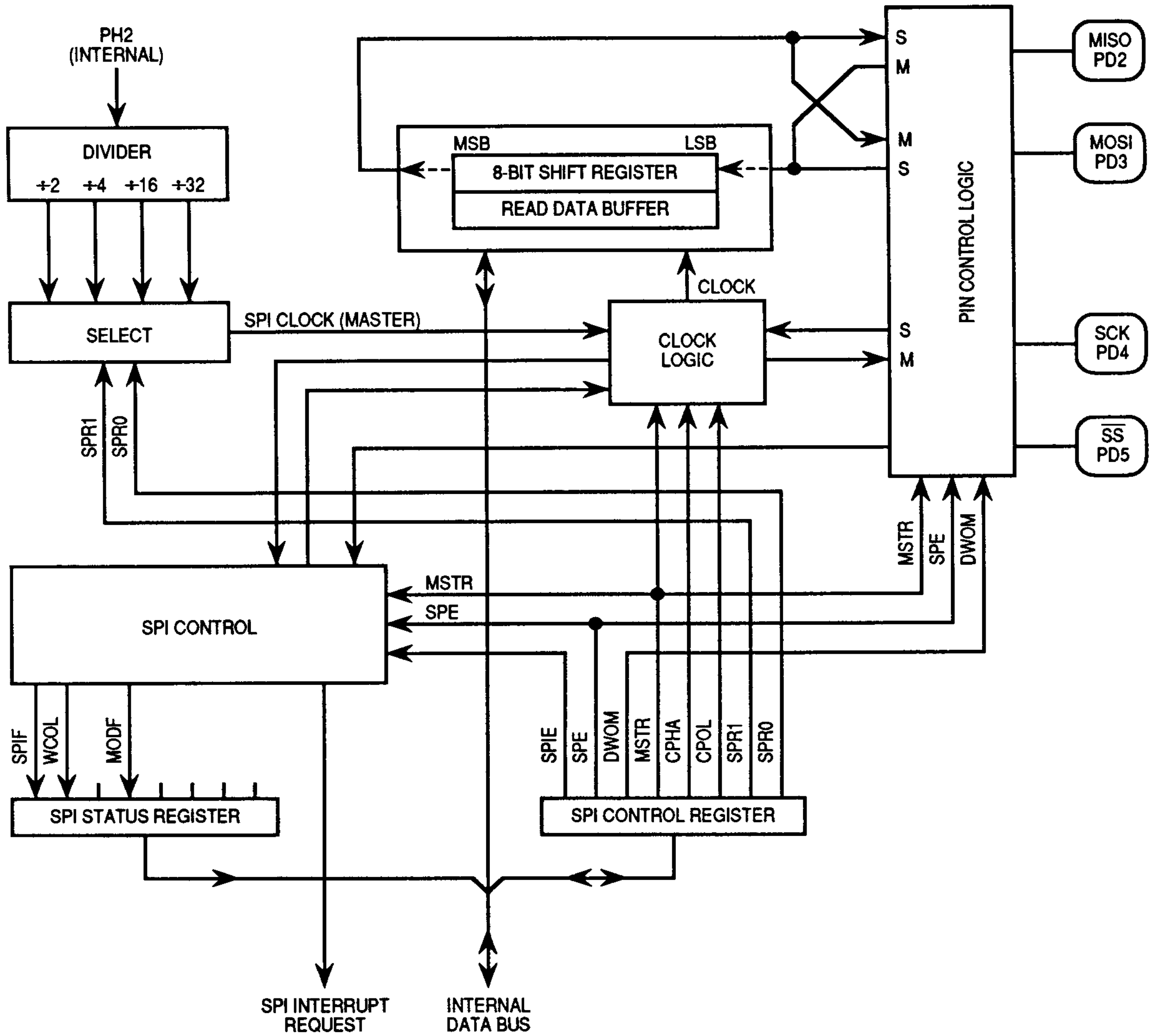
	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

NOTE

Receive and transmit are double buffered. Reads access the receive data buffer and writes access the transmit data buffer.

Serial Peripheral Interface (SPI)

The SPI is an independent serial communications subsystems that allows the MCU to communicate synchronously with peripheral devices and other microprocessors. The SPI protocol facilitates rapid exchange of serial data between devices in a control system. Each SPI compatible component in a system can be set up for master or slave operation. Data rates can be as high as one half of the E-clock rate when configured as master and as fast as the E-clock rate when configured as slave.



SPI Block Diagram

DDRD — Data Direction Register for Port D **$0009**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	R/$\overline{W}$	AS	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDD7–DDD0 — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

SPCR — Serial Peripheral Control **$0028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

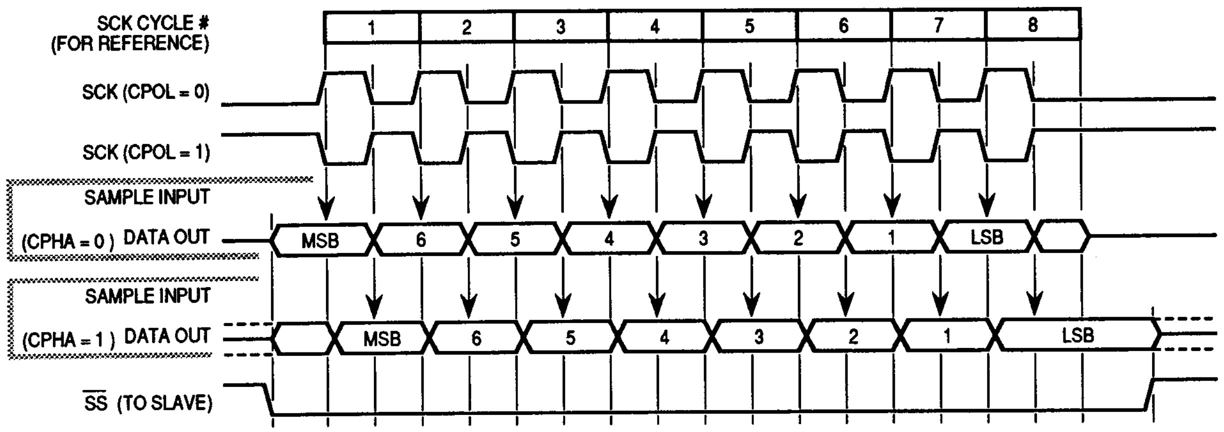
SPIE — Serial Peripheral Interrupt Enable
0 = SPI interrupt disabled
1 = SPI interrupt enabled

SPE — Serial Peripheral System Enable
0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode Option for Pins PD5–PD0
0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select
0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase (Refer to the illustration of the SPI transfer format.)



SPI Transfer Format

SPR1 and SPR0 — SPI Clock Rate Selects

SPR [1:0]	E-Clock Divide By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPSR — Serial Peripheral Status **$0029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

Set when an SPI transfer is complete. Cleared by reading SPSR with SPIF set, followed by SPDR access.

WCOL — Write Collision

Set when SPDR is written while transfer is in progress. Cleared by SPSR with WCOL set, followed by SPDR access.

Bits 5 and 3–0 — Not implemented; always read zero

MODF — Mode Fault (A Mode Fault Terminates SPI Operation.)

Set when $\overline{SS}$ is pulled low while MSTR = 1. Cleared by SPSR read with MODF set, followed by SPCR write.

SPDR — SPI Data **$002A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

NOTE

SPI is double buffered in, single buffered out.

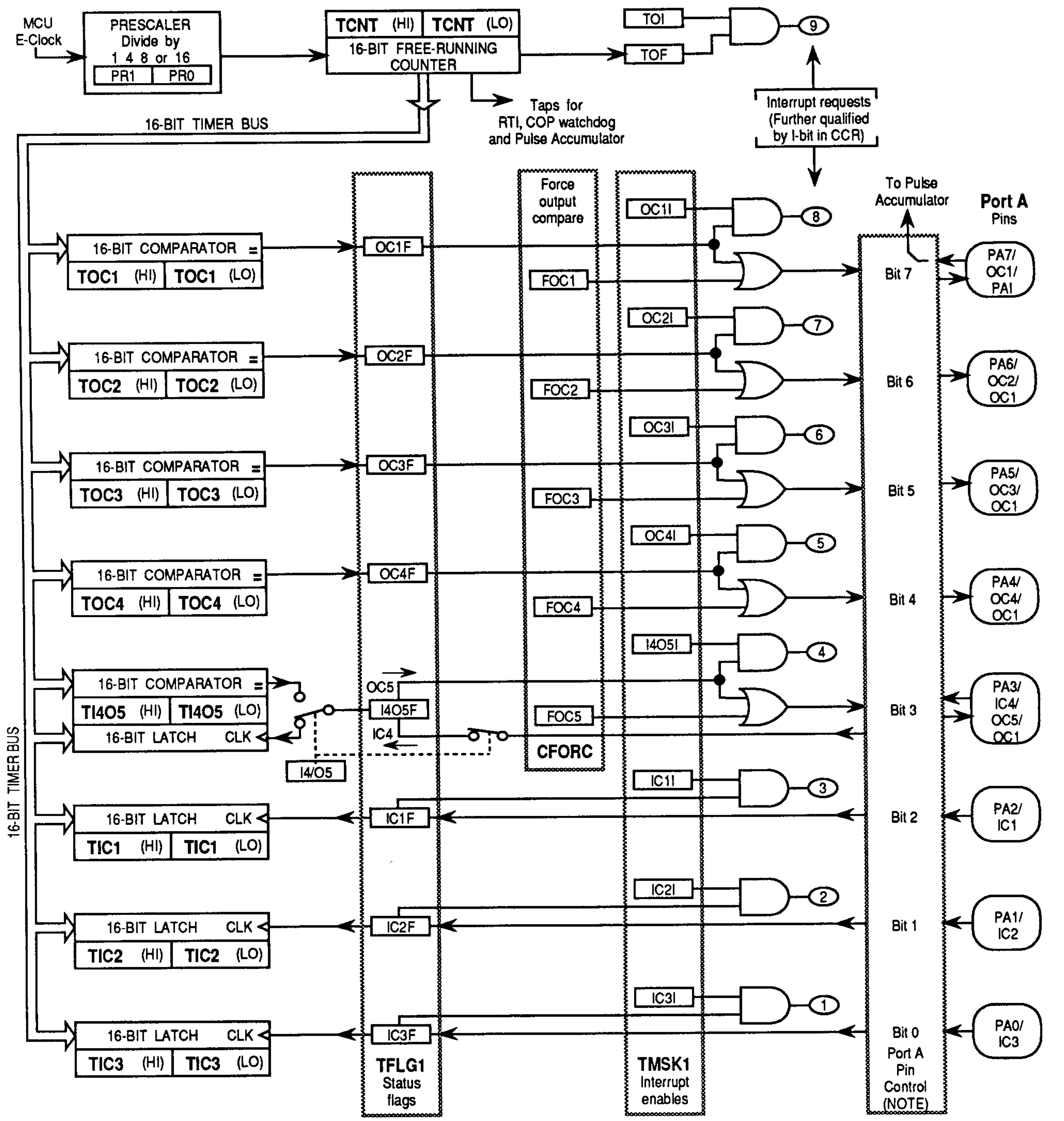
Main Timer

The main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. The timer shares port A pins, which can be configured for three timer input capture (IC) and four timer output compare (OC), and either a fourth IC or a fifth OC. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

The following table summarizes crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	**8.0 MHz**	**12.0 MHz**	**Other Rates**
	1.0 MHz	**2.0 MHz**	**3.0 MHz**	**(E)**
	1000 ns	**500 ns**	**333 ns**	**(1/E)**
PR [1:0]	**Main Timer Count Rates**			
0 0 1 count overflow	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) $(E/2^{16})$
0 1 1 count overflow	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) $(E/2^{18})$
1 0 1 count overflow	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) $(E/2^{19})$
1 1 1 count overflow	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) $(E/2^{20})$
RTR [1:0]	**Periodic (RTI) Interrupt Rates**			
0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	2.731 ms 5.461 ms 10.923 ms 21.845 ms	$(E/2^{13})$ $(E/2^{14})$ $(E/2^{15})$ $(E/2^{16})$
CR [1:0]	**COP Watchdog Timeout Rates**			
0 0 0 1 1 0 1 1	32.768 ms 131.07 ms 524.29 ms 2.097 s	16.384 ms 65.536 ms 262.14 ms 1.049 s	10.923 ms 43.691 ms 174.76 ms 699.05 ms	$(E/2^{15})$ $(E/2^{17})$ $(E/2^{19})$ $(E/2^{21})$
Timeout Tolerance (–0 ms/+...)	32.768 ms	16.4 ms	10.9 ms	$(E/2^{15})$



Main Timer

NOTE: Port A pin actions are controlled by OC1M, OC1D, PACTL, TCTL1, and TCTL2 registers.

CFORC — Timer Compare Force **$000B**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC5–FOC1 — Write Ones to Force Compare(s)
- 0 = Not affected
- 1 = Output compare x action occurs, but OCxF flag bit is not set

Bits 2 – 0 — Not implemented; always read zero

OC1M — Output Compare 1 Mask **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1D to control corresponding pin(s) of port A.

OC1M7–OC1M3 — Output Compare Masks
- 0 = OC1 is disabled
- 1 = OC1 is enabled to control the corresponding pin(s) of Port A

Bits 2–0 — Not implemented; always read zero

OC1D — Output Compare 1 Data **$000D**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit-x on successful OC1D compares.

Bits 2–0 — Not implemented; always read zero

TCNT — Timer Count **$000E, $000F**

$000E	Bit 15	14	13	12	11	10	9	Bit 8	High	TCNT
$000F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture **$0010–$0015**

$0010	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC1
$0011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$0012	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC2
$0013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$0014	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC3
$0015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset.

TOC1–TOC4 — Timer Output Compare **$0016–$001D**

$0016	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC1
$0017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$0018	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC2
$0019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$001A	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC3
$001B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$001C	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC4
$001D	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF).

TI4O5 — Timer Input Capture 4/Output Compare 5 $001E, $001F

$001E	Bit 15	14	13	12	11	10	9	Bit 8	High	TI4O5
$001F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TI4O5 register pair resets to ones ($FFFF).

TCTL1 — Timer Control 1 $0020

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM2–OM5 — Output Mode

OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2 — Timer Control 2 $0021

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$0022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable

I4O5I — Input Capture 4 or Output Compare 5 Interrupt Enable

IC1I–IC3I — Input Capture x Interrupt Enable

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$0023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4O5 of PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TMSK2 — Timer Interrupt Mask 2 **$0024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable

RTII — Real-Time Interrupt Enable

PAOVI — Pulse Accumulator Overflow Interrupt Enable

PAII — Pulse Accumulator Input Interrupt Enable

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

Bits 3–2 — Not implemented; always read zero

PR1 and PR0 — Timer Prescaler Select

In normal modes, PR1 and PR0 can only be written once, and the write must be within 64 cycles after reset. Refer to the timer summary table for specific timing values.

PR [1:0]	Prescaler (Divide E-Clock By)
0 0	1
0 1	4
1 0	8
1 1	16

TFLG2 — Timer Interrupt Flag 2 **$0025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000.

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. See RTR1:0 bits in PACTL register.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits 3–0 — Not implemented; always read zero

PACTL — Pulse Accumulator Control $0026

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits 7 and 3–2 — Refer to **Parallel I/O.**

Bits 6–4 — Refer to **Pulse Accumulator.**

RTR1–RTR0 — RTI Interrupt Rate Selects

These two bits select one of four rates for the real-time periodic interrupt circuit. Refer to the following table.

Real-Time Interrupt Rates

RTR [1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.38 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.77 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.54 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

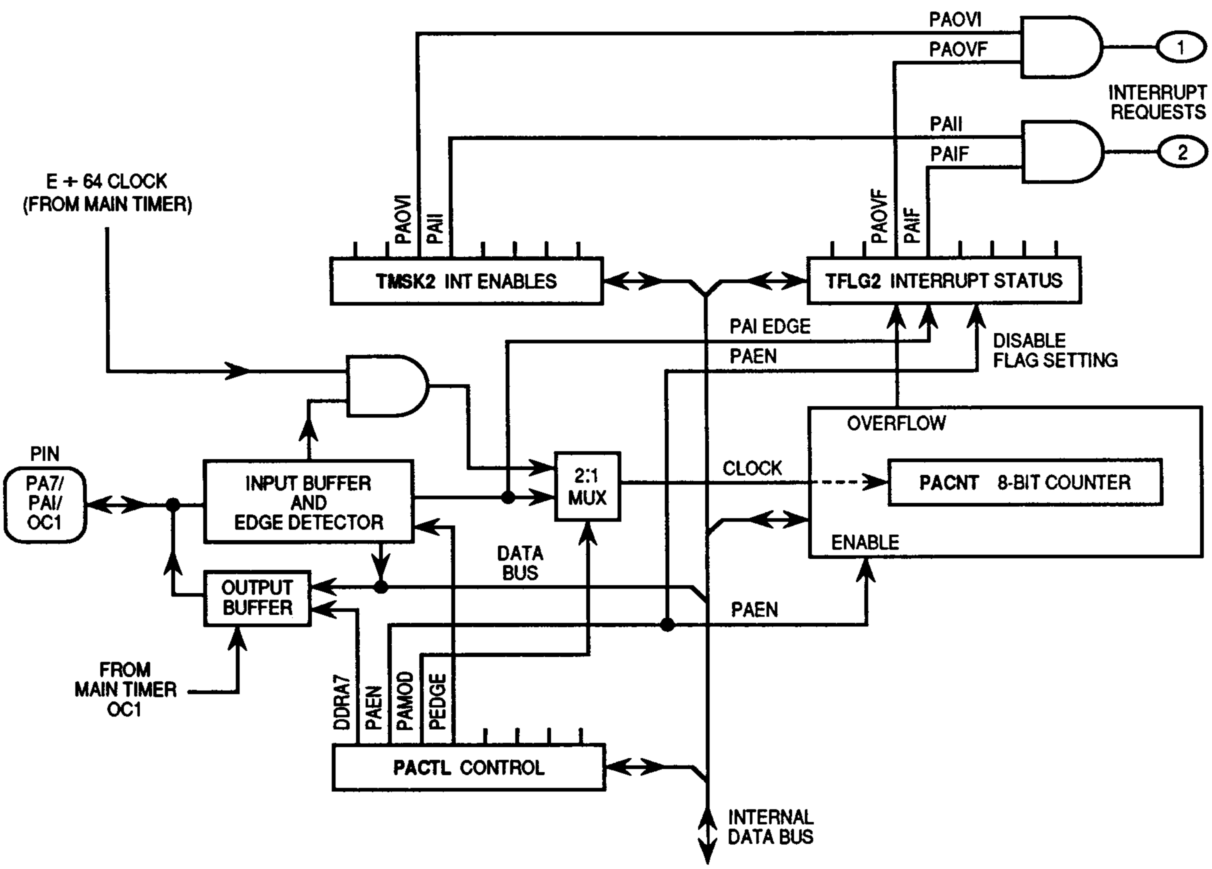
Pulse Accumulator

The pulse accumulator system is based on an 8-bit counter that can be configured to operate as a simple event counter or as a gated time accumulator. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time.

The port A bit 7 I/O pin (PA7/PAI/OC1) associated with the pulse accumulator can be configured to act as a clock (event counting mode), or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode).

Pulse Accumulator Timing

	Selected Crystal	Common XTAL Frequencies 4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**	**3.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**	**333 ns**
Pulse Accumulator (in Gated Mode)				
$(E/2^6)$	1 count	64.0 µs	32.0 µs	21.33 µs
$(E/2^{14})$	overflow	16.384 ms	8.192 ms	5.461 ms



Pulse Accumulator System Block Diagram

TMSK2 — Timer Interrupt Mask 2 **$0024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

Bits 7–6 and 1–0 — Refer to **Main Timer.**

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = Pulse accumulator overflow interrupt disabled
1 = Interrupt requested when bit PAOVF of TFLG2 is set

PAII — Pulse Accumulator Interrupt Enable
0 = Pulse accumulator interrupt disabled
1 = Interrupt requested when bit PAIF of TFLG2 is set

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

Bits 3–2 — Not implemented; always read zero

TFLG2 — Timer Interrupt Flag 2 **$0025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

Bits 7–6 — Refer to **Main Timer.**

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits 3–0 — Not implemented; always read zero

PACTL — Pulse Accumulator Control $0026

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits 7 and 3–2 — Refer to **Parallel I/O.**

PAEN — Pulse Accumulator System Enable
- 0 = Pulse Accumulator disabled
- 1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
- 0 = Event counter
- 1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
- 0 = Falling edges increment counter: high level enables accumulation
- 1 = Rising edges increment counter: low level enables accumulation

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A Zero on PAI Inhibits Counting
1	1	A One on PAI Inhibits Counting

Bits 1–0 — Refer to **Main Timer.**

PACNT — Pulse Accumulator Counter $0027

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

Readable and writable.