GAL20XV10

High-Speed E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 100 MHz**
  - **— 7 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 90mA Maximum Icc**
  - **— 75mA Typical Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100 ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— XOR Gate Capability on all Outputs**
  - **— Full Function and Parametric Compatibility with PAL12L10, 20L10, 20X10, 20X8, 20X4**
  - **— Registered or Combinatorial with Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
- **APPLICATIONS INCLUDE:**
  - **— High Speed Counters**
  - **— Graphics Processing**
  - **— Comparators**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

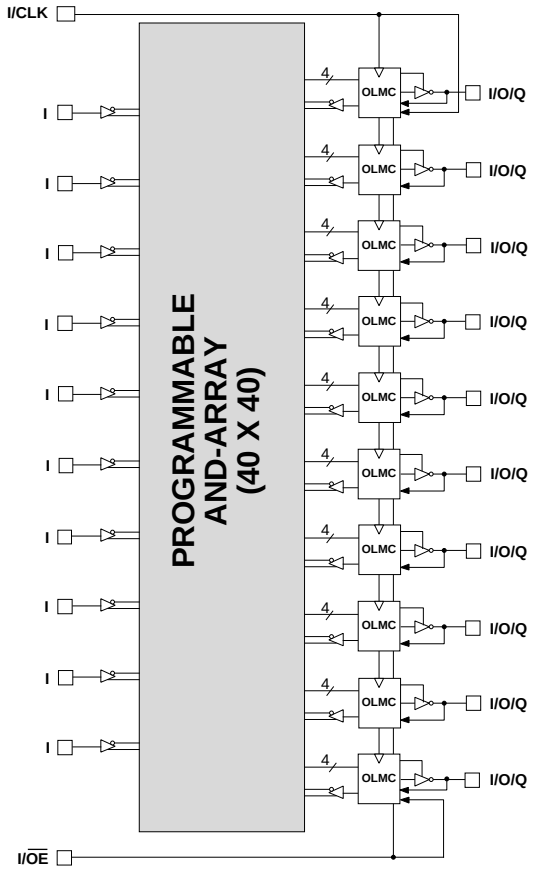
DESCRIPTION

The GAL20XV10 combines a high performance CMOS process with electrically erasable (E^2) floating gate technology to provide the highest speed Exclusive-OR PLD available in the market. At 90mA maximum Icc (75mA typical Icc), the GAL20XV10 provides a substantial savings in power when compared to bipolar counterparts. E²CMOS technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20XV10 are the PAL® architectures listed in the macrocell description section of this document. The GAL20XV10 is capable of emulating these PAL architectures with full function and parametric compatibility.

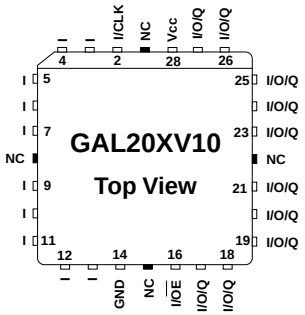
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

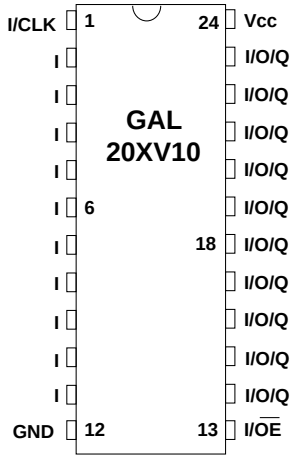


PIN CONFIGURATION

PLCC



DIP



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LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
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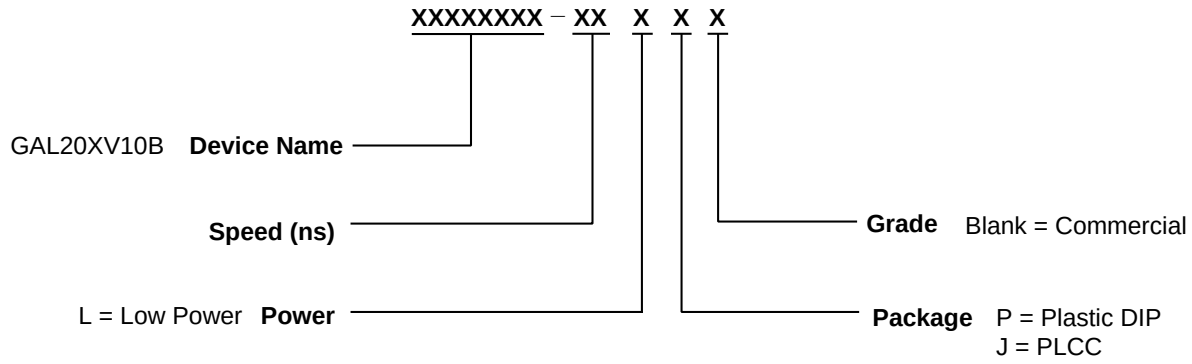
GAL20XV10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	6	7	90	GAL20XV10B-10LP	24-Pin Plastic DIP
				GAL20XV10B-10LJ	28-Lead PLCC
15	8	8	90	GAL20XV10B-15LP	24-Pin Plastic DIP
				GAL20XV10B-15LJ	28-Lead PLCC
20	10	10	90	GAL20XV10B-20LP	24-Pin Plastic DIP
				GAL20XV10B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the Output Logic Macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The GAL20XV10 has two global architecture configurations that allow it to emulate PAL architectures. The Input mode emulates combinatorial PAL devices, with the I/CLK and I/$\overline{OE}$ pins used as inputs. The Feedback mode emulates registered PAL devices with the I/CLK pin used as the register clock and the I/$\overline{OE}$ pin as an output enable for all registers. The following is a list of PAL architectures that the GAL20XV10 can emulate. It also shows the global architecture mode used to emulate the PAL architecture.

PAL Architectures Emulated by GAL20XV10	GAL20XV10 Global OLMC Mode
PAL12L10	Input Mode
PAL20L10	Input Mode
PAL20X10	Feedback Mode
PAL20X8	Feedback Mode
PAL20X4	Feedback Mode

INPUT MODE
The Input mode architecture is defined when the global architecture bit SYN = 1. In this mode, the I/CLK pin becomes an input to the AND array and also provides the clock source for all registers. The I/OE pin becomes an input into the AND array and provides the output enable control for any macrocell configured as an Exclusive-OR function. Feedback into the AND array is provided from macrocells 2 through 9 only. In this mode, macrocells 1 and 10 have no feedback into the AND array.

FEEDBACK MODE
The Feedback mode architecture is defined when the global architecture bit SYN = 0. In this mode the I/CLK pin becomes a dedicated clock source for all registers. The I/$\overline{OE}$ pin is a dedicated output enable control for any macrocell configured as an Exclusive-OR function. The I/CLK and I/$\overline{OE}$ pins are not available to the AND array in this mode. Feedback into the AND array is provided on all macrocells 1 through 10.

FEATURES
Each Output Logic Macrocell has four possible logic function configurations controlled by architecture control bits AC0 and AC1. Four product terms are fed into each macrocell.

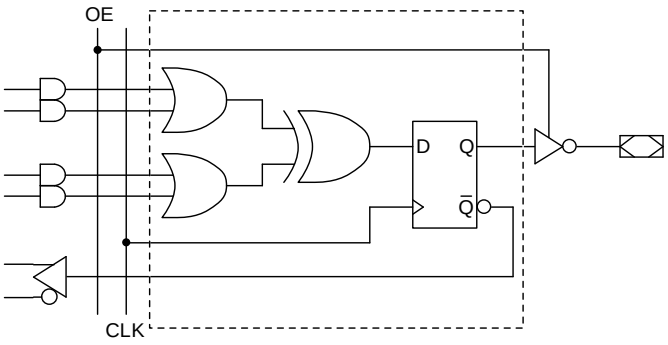
XOR REGISTERED CONFIGURATION
The Macrocell is set to the Exclusive-OR Registered configuration when AC0 = 0 and AC1 = 0. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register. The register is clocked by the low-to-high transition of the I/CLK pin. The inverting output buffer is enabled by the I/$\overline{OE}$ pin, which is an active low output enable common to all Exclusive-OR macrocells. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

REGISTERED CONFIGURATION
The Macrocell is set to Registered configuration when AC0 = 1 and AC1 = 0. Three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output. The register is clocked by the low-to-high transition of the I/CLK. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

XOR COMBINATORIAL CONFIGURATION
The Macrocell is set to the Exclusive-OR Combinatorial configuration when AC0 = 0 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer. The inverting output buffer is enabled by the I/$\overline{OE}$ pin, which is an active low output enable that is common to all XOR macrocells. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

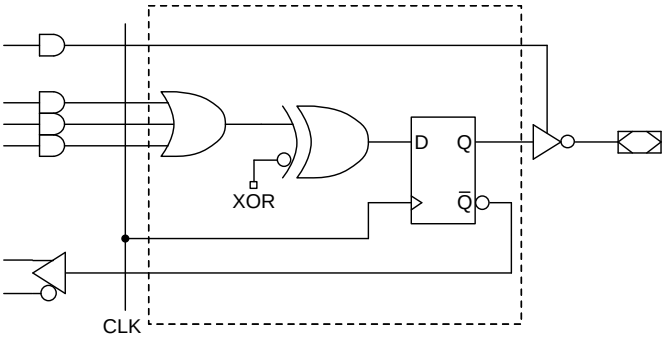
COMBINATORIAL CONFIGURATION
The Macrocell is set to Combinatorial mode when AC0 = 1 and AC1 = 1. Three of the four product terms are used as sum-of-product terms for the combinatorial output. The XOR bit controls the polarity of the output. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

INPUT MODE



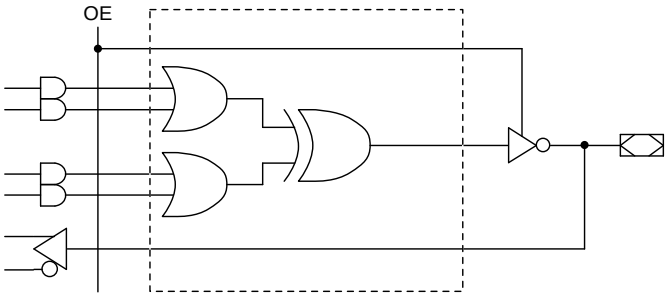
XOR Registered Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 0.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- Pin 13(16) can be $\overline{OE}$ and/or Input.



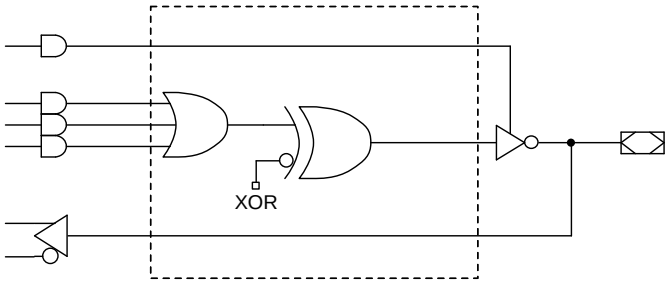
Registered Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- OE controlled by product term.



XOR Combinatorial Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 1.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 13(16) can be $\overline{OE}$ and/or Input.

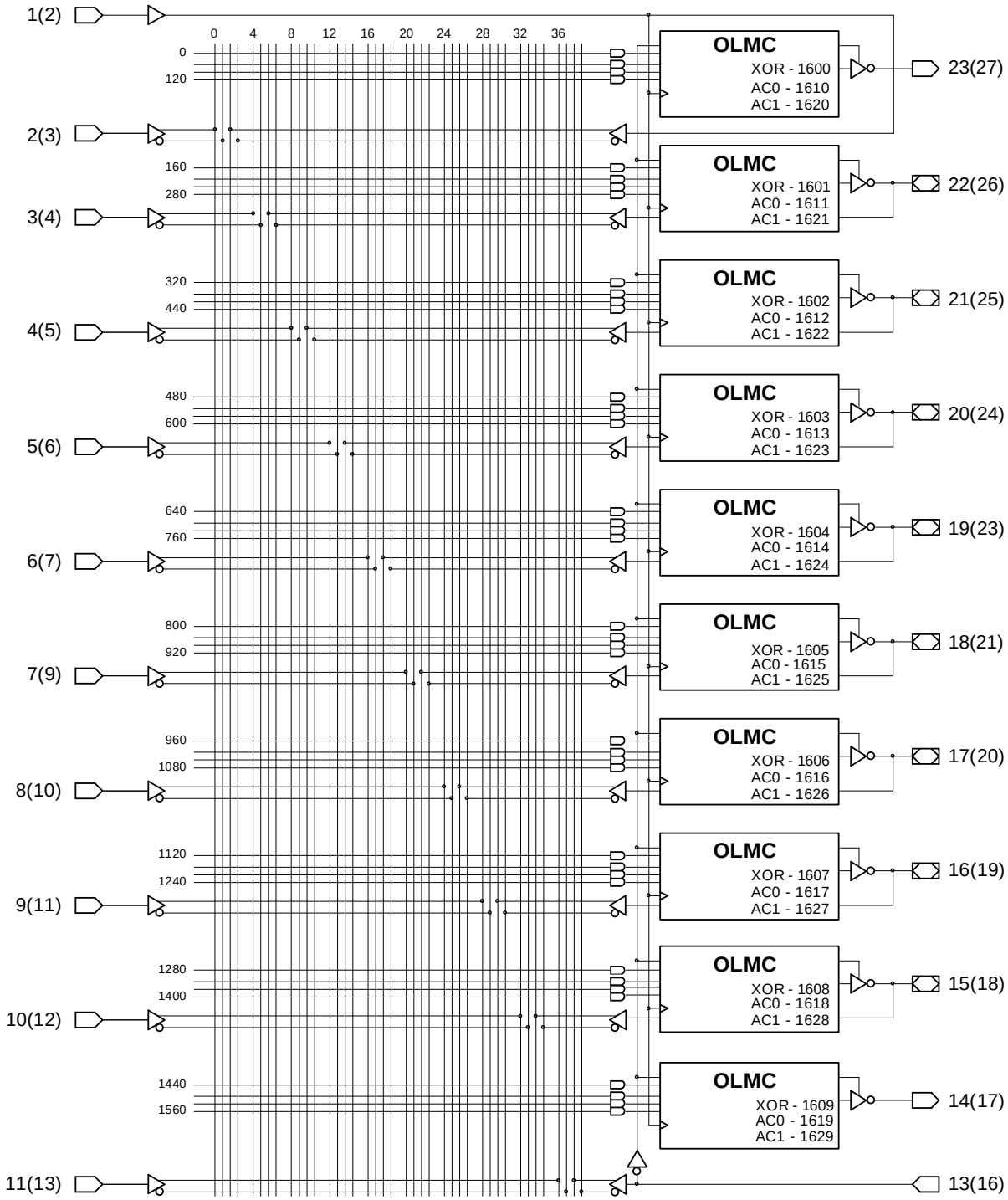


Combinatorial Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- OE controlled by product term.

INPUT MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts

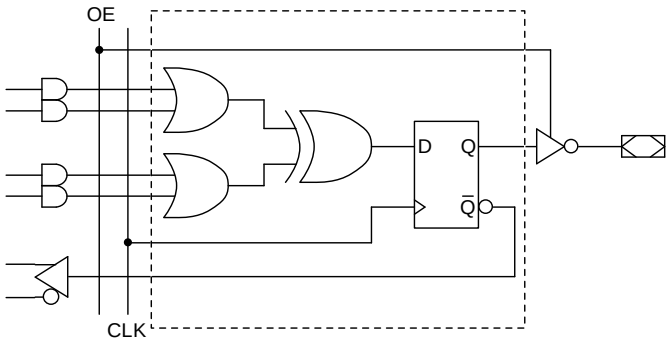


40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, ...			.... 1669, 1670
Byte4	Byte3	.... Byte1	Byte0

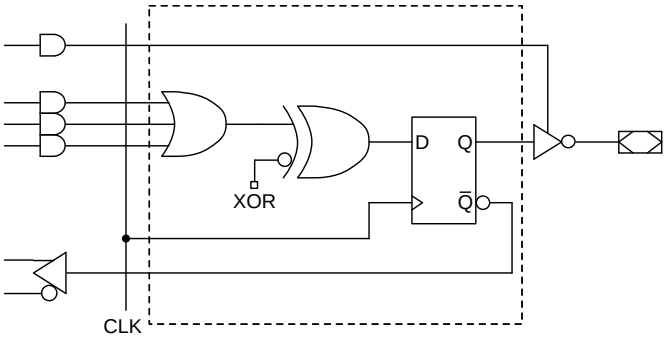
SYN - 1630

FEEDBACK MODE



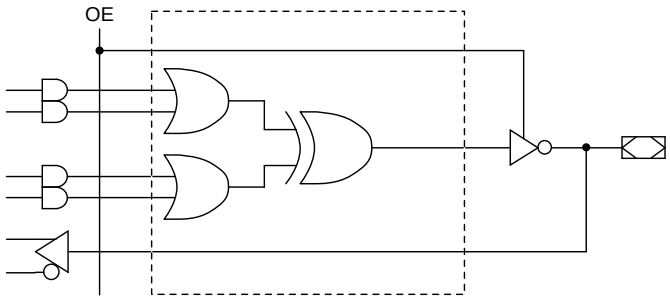
XOR Registered Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 0.
- Dedicated CLK input on Pin 1(2).
- Dedicated $\overline{OE}$ input on Pin 13(16).



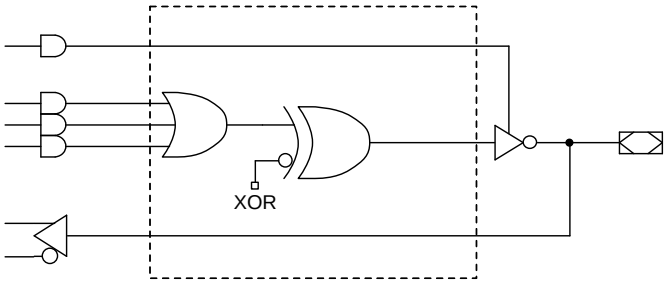
Registered Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- Dedicated CLK input on Pin 1(2).
- OE controlled by product term.
- Pin 13(16) is not connected to this configuration.



XOR Combinatorial Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 1.
- Dedicated $\overline{OE}$ input on Pin 13(16).
- Pin 1(2) is not connected to this configuration.

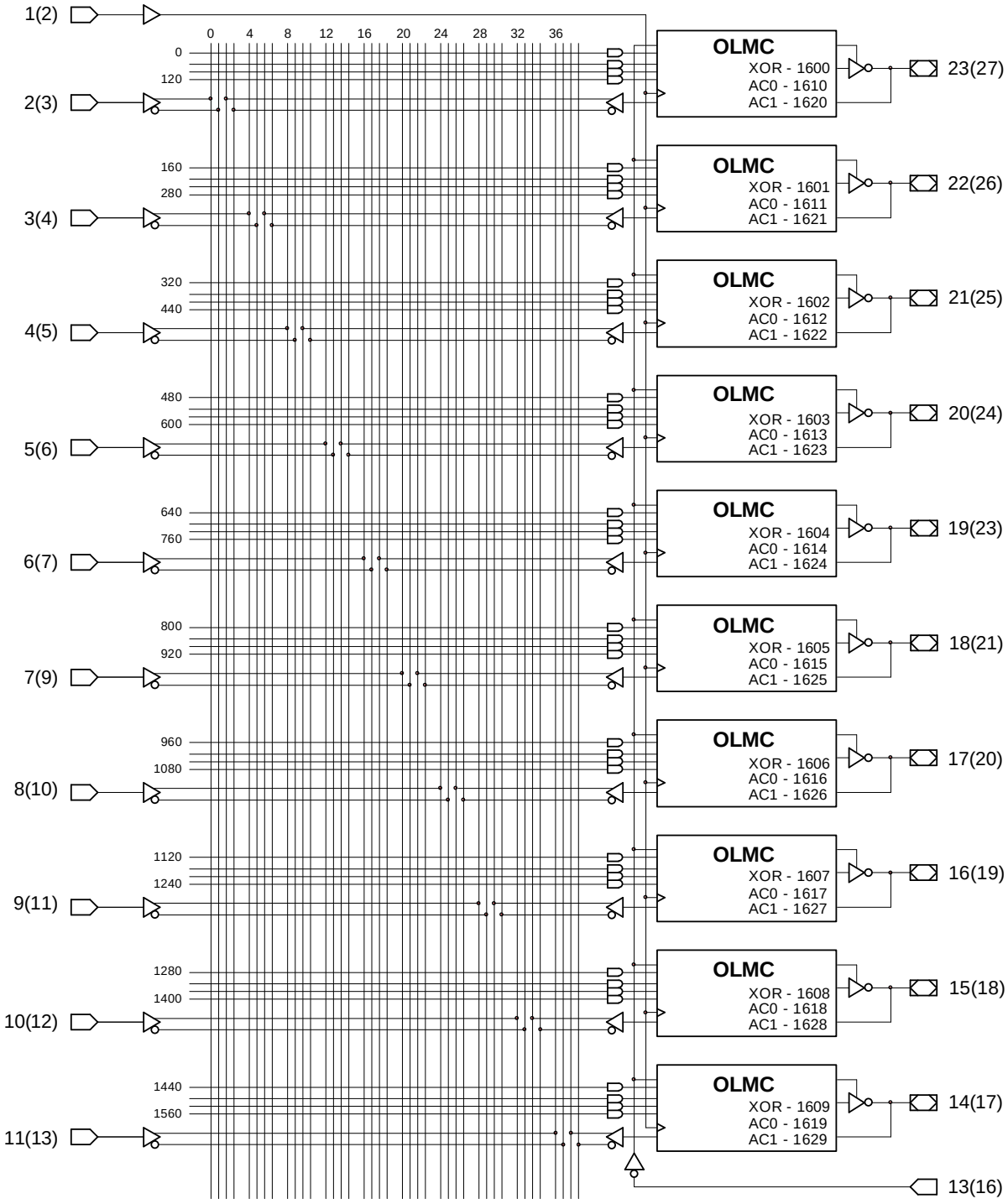


Combinatorial Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OE controlled by product term.
- Both pin1(2) and pin 13(16) are not connected to this configuration.

FEEDBACK MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, ...			.... 1669, 1670
Byte4	Byte3	.... Byte1	Byte0

SYN - 1630

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage Vcc ..... –0.5 to+7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		V_{SS} – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	V_{CC}+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A= 25°C	–50	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/-20	—	75	90	mA

1) The leakage current is due to the internal pull-up on all input and I/O pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at V_{CC} = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -10		COM -15		COM -20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
t_{co}	A	Clock to Output Delay	2	7	2	8	2	10	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	4	—	4	—	4	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	6	—	8	—	10	—	ns
t_{h}	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	62.5	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	100	—	83.3	—	71.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	83.3	—	71.4	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	6	—	7	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	6	—	7	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
	B	$\overline{OE}$ to Output Enabled	2	9	2	10	2	15	ns
t_{dis}	C	Input or I/O to Output Disabled	3	9	3	15	3	20	ns
	C	$\overline{OE}$ to Output Disabled	2	9	2	10	2	15	ns

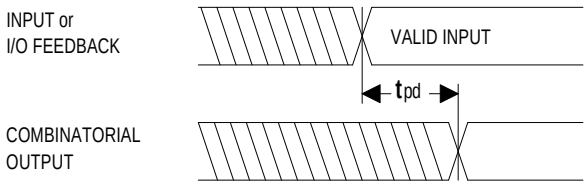
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

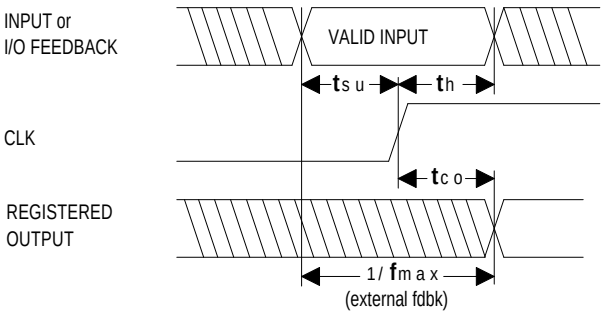
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

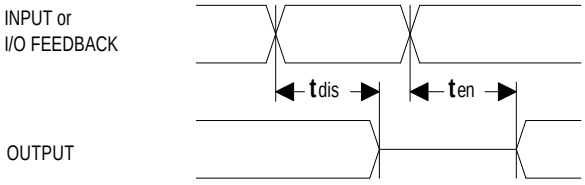
SWITCHING WAVEFORMS



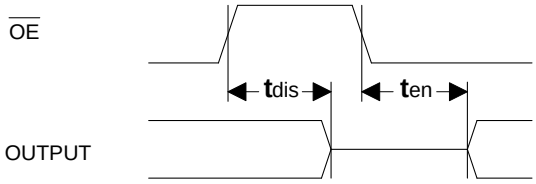
Combinatorial Output



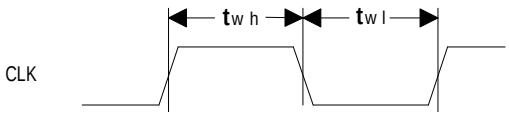
Registered Output



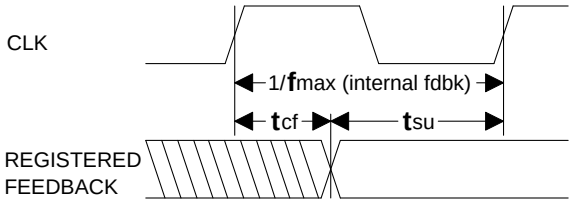
Input or I/O Feedback to Enable/Disable



$\overline{OE}$ to Output Enable/Disable

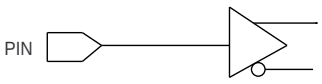


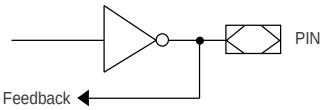
Clock Width

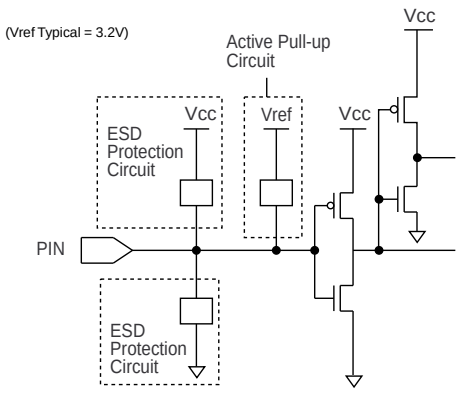


fmax with Feedback

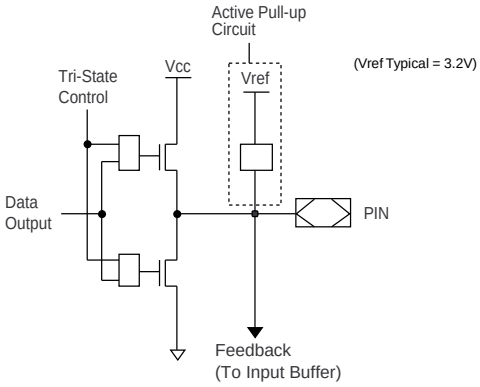
INPUT/OUTPUT EQUIVALENT SCHEMATICS





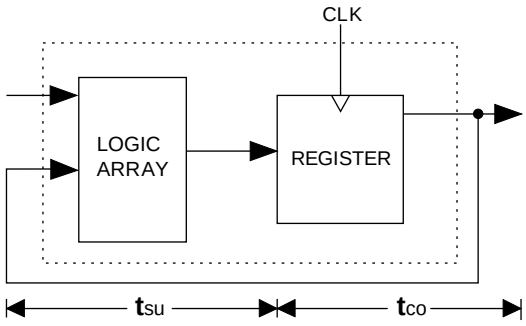


Typical Input



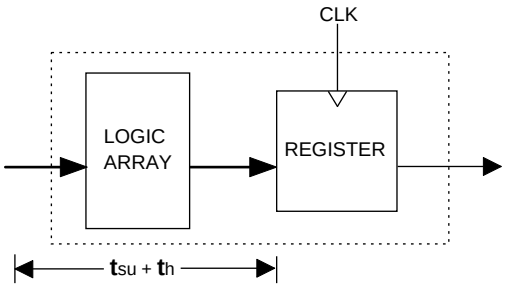
Typical Output

fmax DESCRIPTIONS



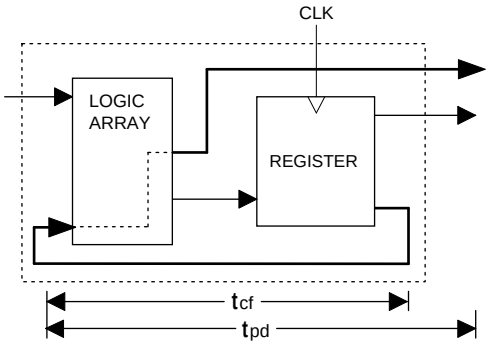
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

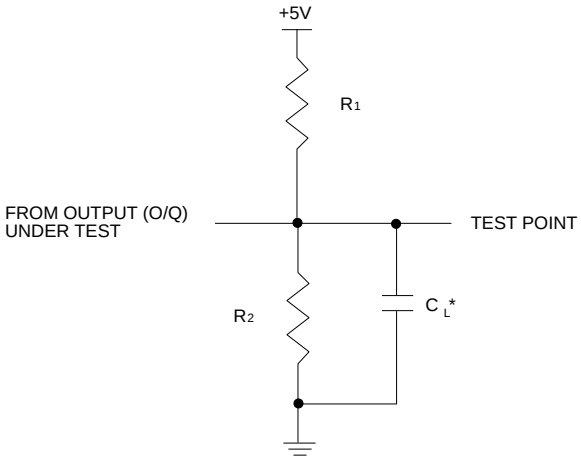
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20XV10 device. It contains 40 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits, if programmed to any value other then zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20XV10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes less than a second. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

LATCH-UP PROTECTION

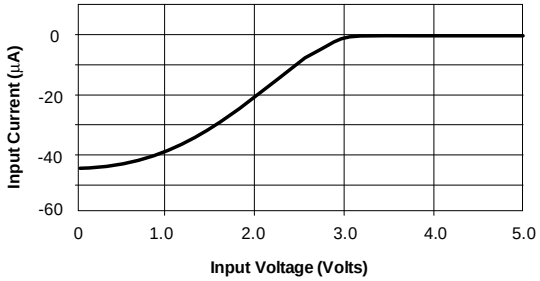
GAL20XV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL20XV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

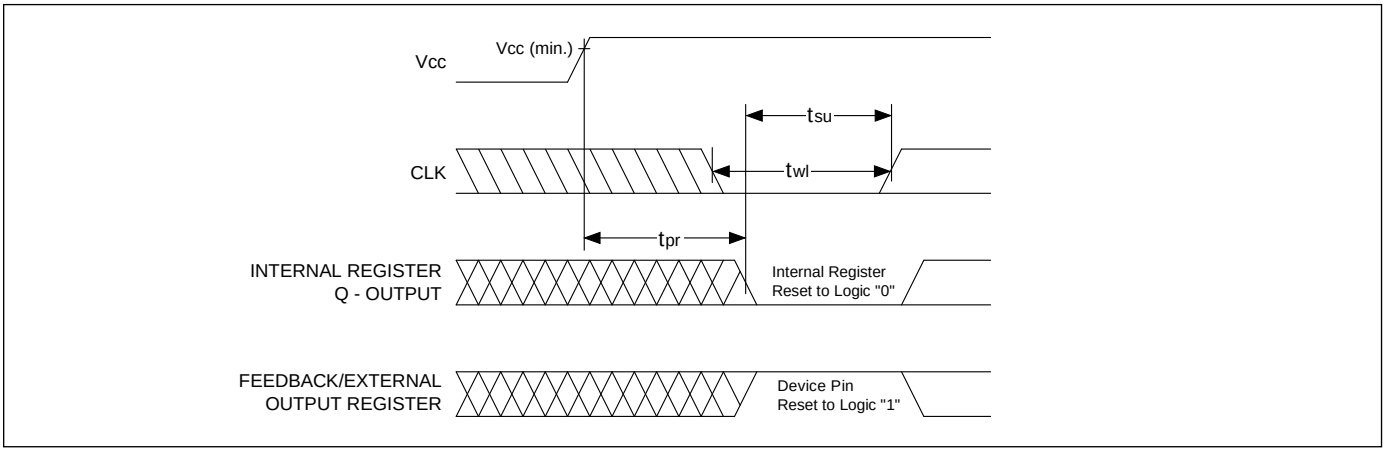
GAL20XV10 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic



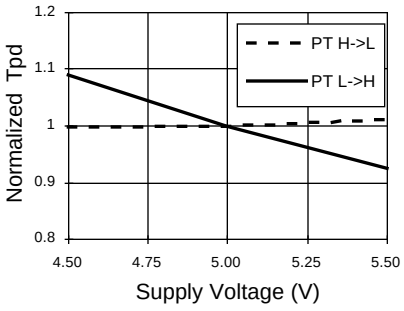
POWER-UP RESET

Circuitry within the GAL20XV10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20XV10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

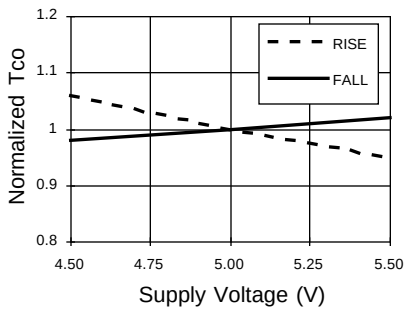


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

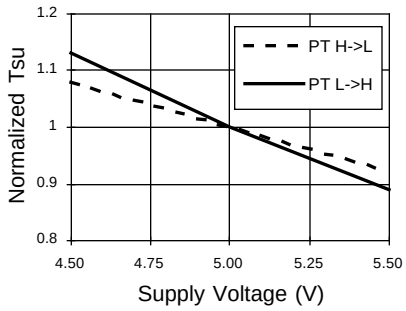
Normalized Tpd vs Vcc



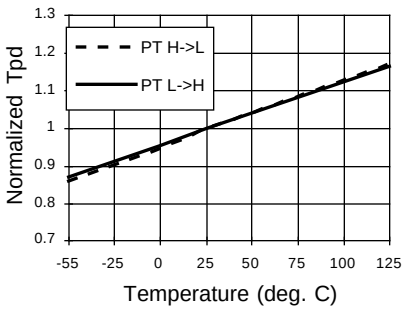
Normalized Tco vs Vcc



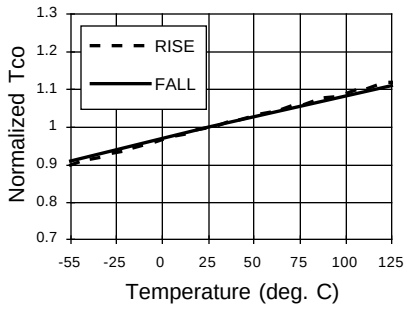
Normalized Tsu vs Vcc



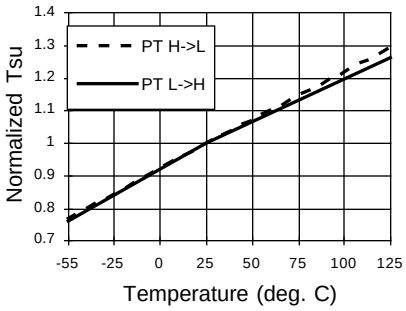
Normalized Tpd vs Temp



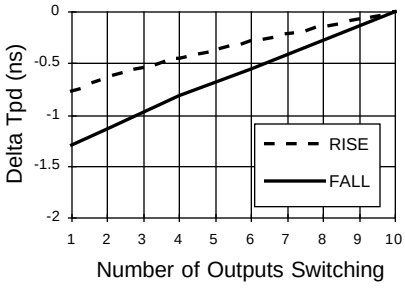
Normalized Tco vs Temp



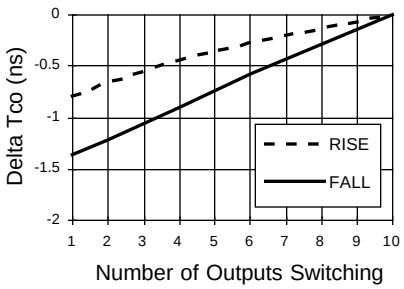
Normalized Tsu vs Temp



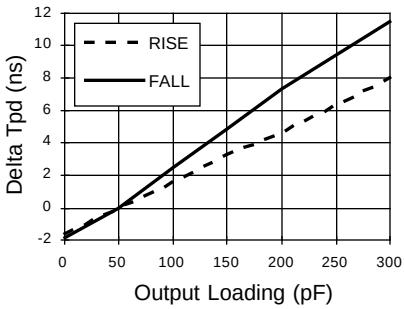
Delta Tpd vs # of Outputs Switching



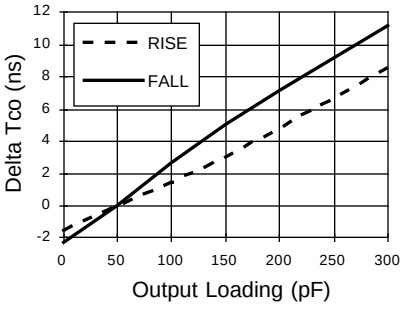
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

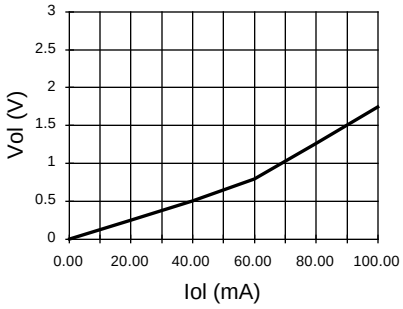


Delta Tco vs Output Loading

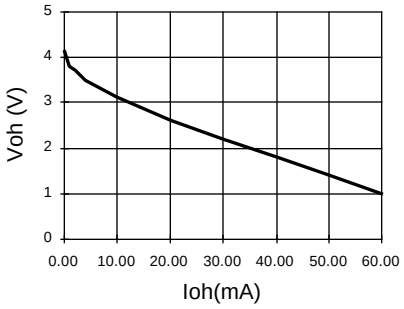


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

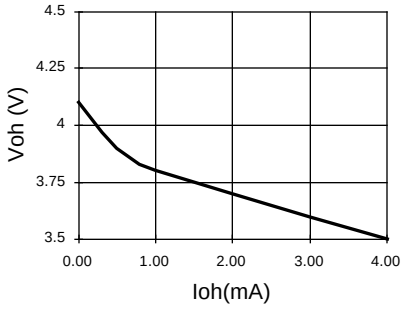
Vol vs Iol



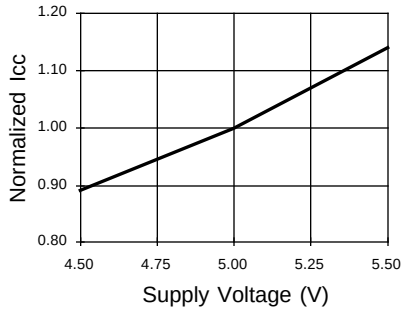
Voh vs Ioh



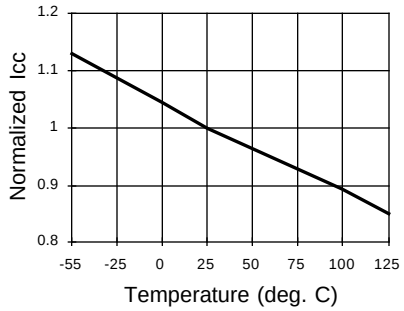
Voh vs Ioh



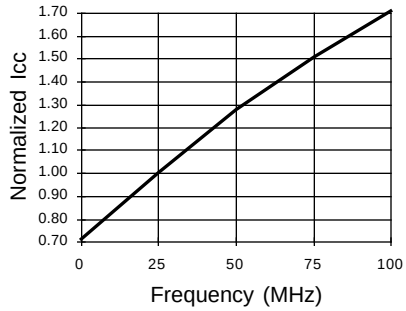
Normalized Icc vs Vcc



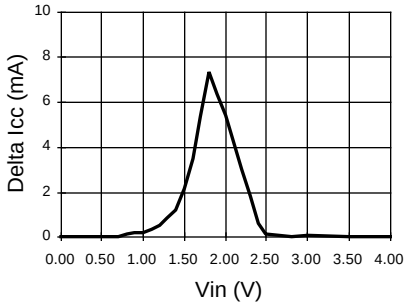
Normalized Icc vs Temp



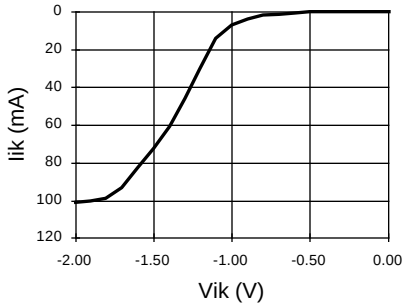
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



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