SHARP

Scope

The following covers logic, electric, packaging and crating specifications for LH-0080 and LH-0080A 8-bit microprocessors. The LH-0080A is a high speed microprocessor with an upper frequency limit of 4MHz.

Paragraphs 1 to 5 cover logic specifications common to both the LH-0080 and LH-0080A. Paragraphs 6 and 7 cover electric specifications for the LH-0080, and paragraphs 6' and 7' cover electric specifications for the LH-0080A. For Packaging and crating specifications for LH-0080 and LH-0080A plastic DIP and ceramic DIP types, refer to "Packaging and Crating Specifications".

Introduction

The LH-0080 and LH-0080A are third generation Z80-CPU microprocessors constructed using the N-channel silicon gate E/D MOS process. They provide more efficient memory utilization and higher system throughput Peripheral circuits are controlled by decoded signals. For operation, they require only a single 5V DC supply and single-phase 5V clock. Wiring of peripheral circuits is extremely simple.

1. Features

- 8-bit, single chip, parallel processing
- N-channel, silicon gate E/D MOS process
- 158 basic instructions includes all 78 of the 8080A instructions with a machine language compatibility. New instructions include 4-bit, 8-bit and 16-bit operations and additional useful address modes such as index, bit and relative address.
- 22 internal registers
- Powerful interrupt with three maskable interrupt modes plus non-maskable interrupt
- Direct interface with standard static and dynamic memories with a minimum of external circuitry. Refresh circuit is included.
- 1.0μs instruction execution speed (LH-0080A)
- Single 5V DC supply with single-phase 5V clock
- All pins are TTL compatible
- 40-pin DIP package

SHARP

2. Internal construction

The internal construction is shown in Fig. 1.

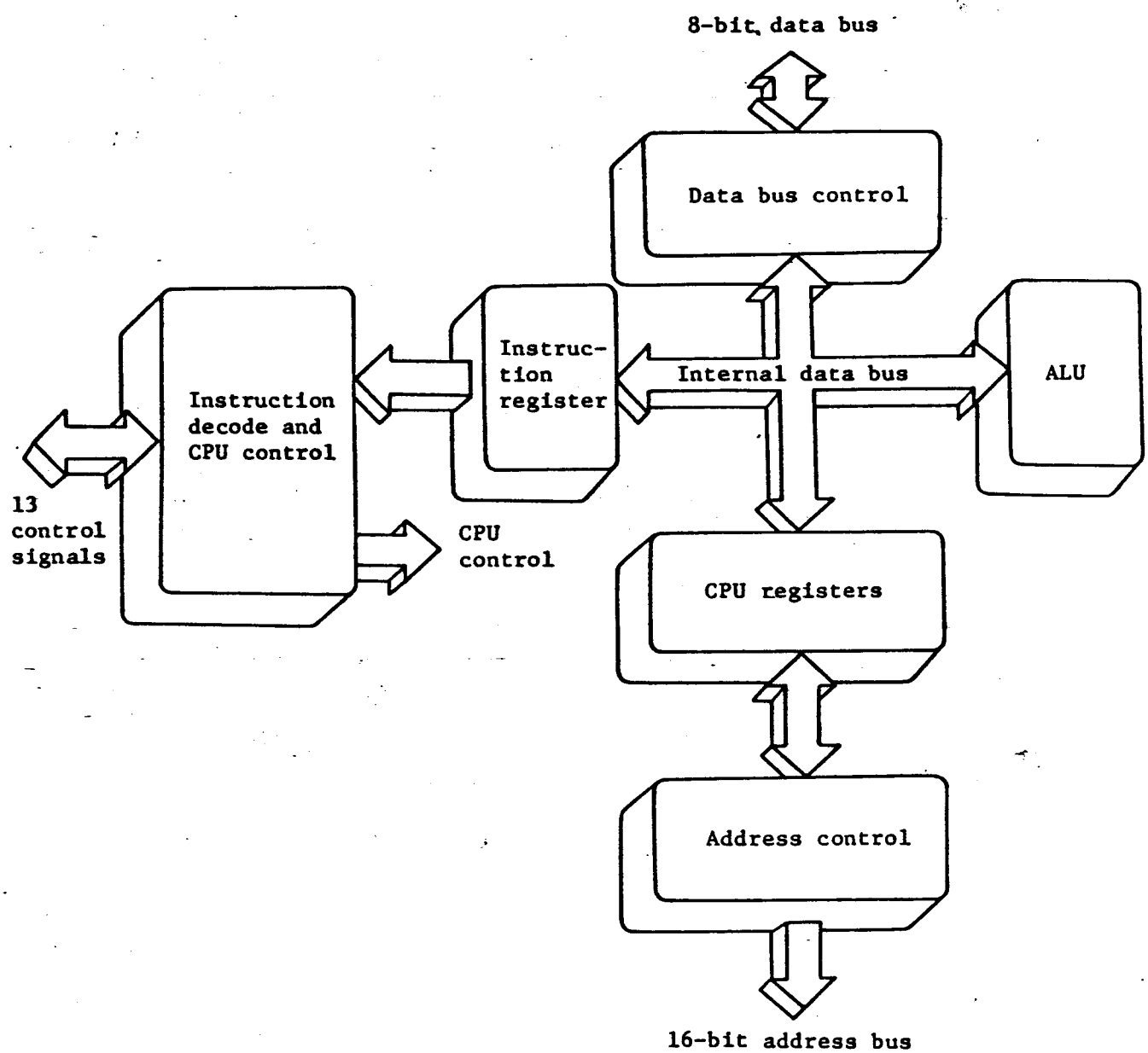


Fig. 1 Block diagram of LH-0080 (Z80-CPU) and LH-0080A (Z80A-CPU)

SHARP

The internal register is composed of a 207-bit read/write memory.

Register configuration is shown in Fig. 2.

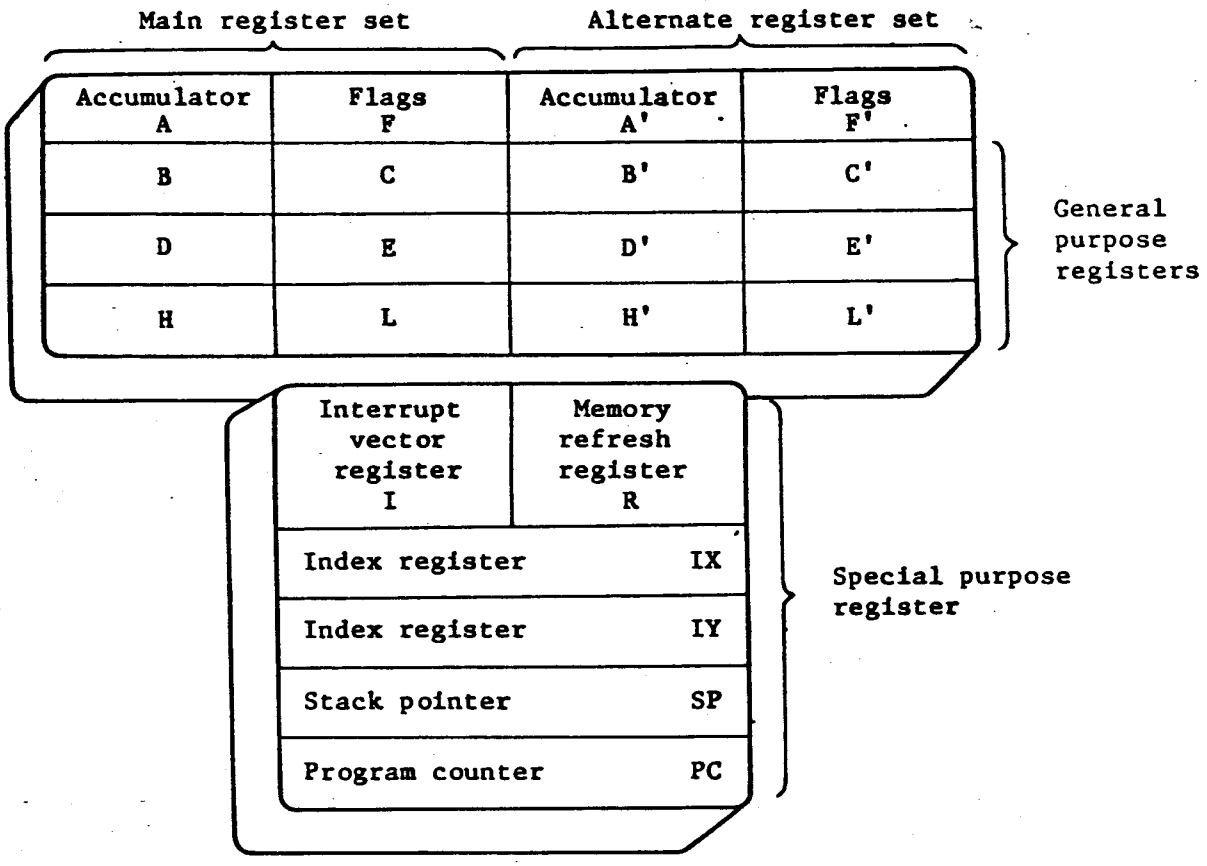


Fig. 2 - CPU register

The CPU register is composed of general purpose registers and special purpose registers. The general purpose registers are divided into main register sets and alternate register sets. With an exchange instruction, contents in the two register sets can be exchanged. Each register set is composed of an 8-bit accumulator, an 8-bit flag register and six 8-bit general purpose registers. Two 8-bit general purpose registers can be paired (as BC, DE, HL) to form a 16-bit register.

The special purpose register is composed of the 8-bit interrupt vector register I, the 7-bit memory refresh register R, two 16-bit index registers, the 16 bit stack pointer SP, and the 16-bit program counter PC. For interrupt vector register I provides the upper 8 bits of an indirect address for the interrupt service routine. The lower 8 bits are provided by the interrupt device. The memory refresh register R automatically issues memory refresh addresses when a dynamic RAM is used as the external memory.

SHARP

3. Pin configurations

Pin configurations are shown in Fig. 3.

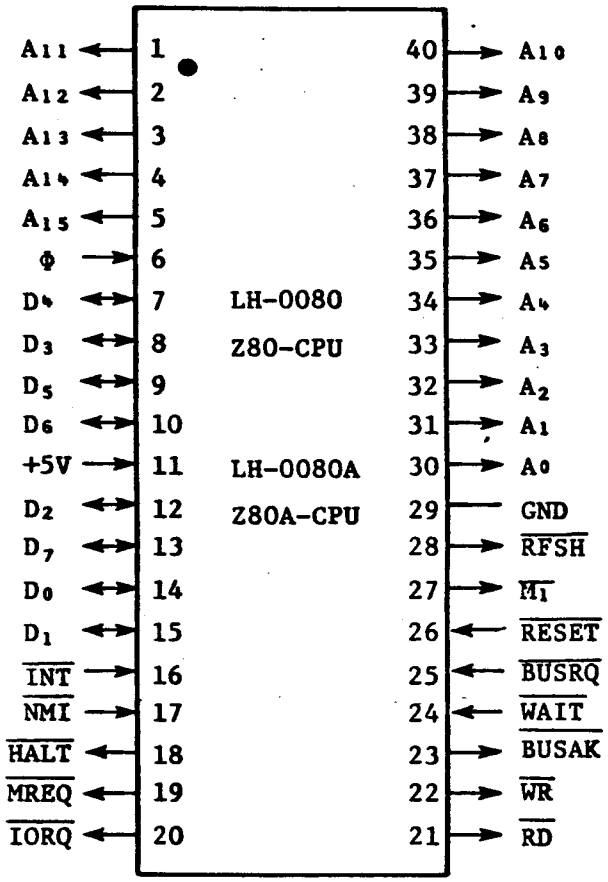


Fig. 3 LH-0080, LH-0080A Pin Configuration

SHARP

The pin signals are functionally divided into 5 groups:

(1) Address bus : $A_0 - A_{15}$

(2) Data bus : $D_0 - D_7$

(3) System control : $\overline{M_1}$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{WR}$, $\overline{RD}$, $\overline{RFSH}$

(4) CPU control : $\overline{HALT}$, $\overline{WAIT}$, $\overline{INT}$, $\overline{NMI}$, $\overline{RESET}$

(5) CPU bus control : $\overline{BUSRQ}$, $\overline{BUSAK}$

$A_0 - A_{15}$ (Address bus) : This is a 16-bit address bus providing addresses for memory data exchange (up to 64K bytes) and I/O device data exchange. (Tri-state output)

$D_0 - D_7$ (Data bus) : This is an 8-bit bidirectional data bus for data exchange between memory and I/O devices.

$\overline{M_1}$ (Machine Cycle One) : Indicates that OP code fetch cycle is the current machine cycle. (Output)

$\overline{MREQ}$ (Memory Request) : Indicates when the address bus is holding a valid memory address. (Tri-state output)

$\overline{IORQ}$ (Input/Output Request) : Indicates the lower 8 bits of the address bus are holding a valid I/O device address. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. (Tri-state output)

$\overline{RD}$ (Memory Read) : Indicates that the LH-0080 or LH-0080A CPU is wanting to read data from memory or an I/O device. The memory or the I/O device should use this signal to gate data onto the CPU data bus. (Tri-state output)

$\overline{WR}$ (Memory Write) : Indicates that the CPU data bus holds valid data for storage in the addressed memory or I/O device. (Tri-state output)

$\overline{RFSH}$ (Refresh) : Indicates that the lower 7 bits of the address bus contain a refresh address for the dynamic RAM. At this time, $\overline{MREQ}$ signal is also generated. (Output)

SHARP

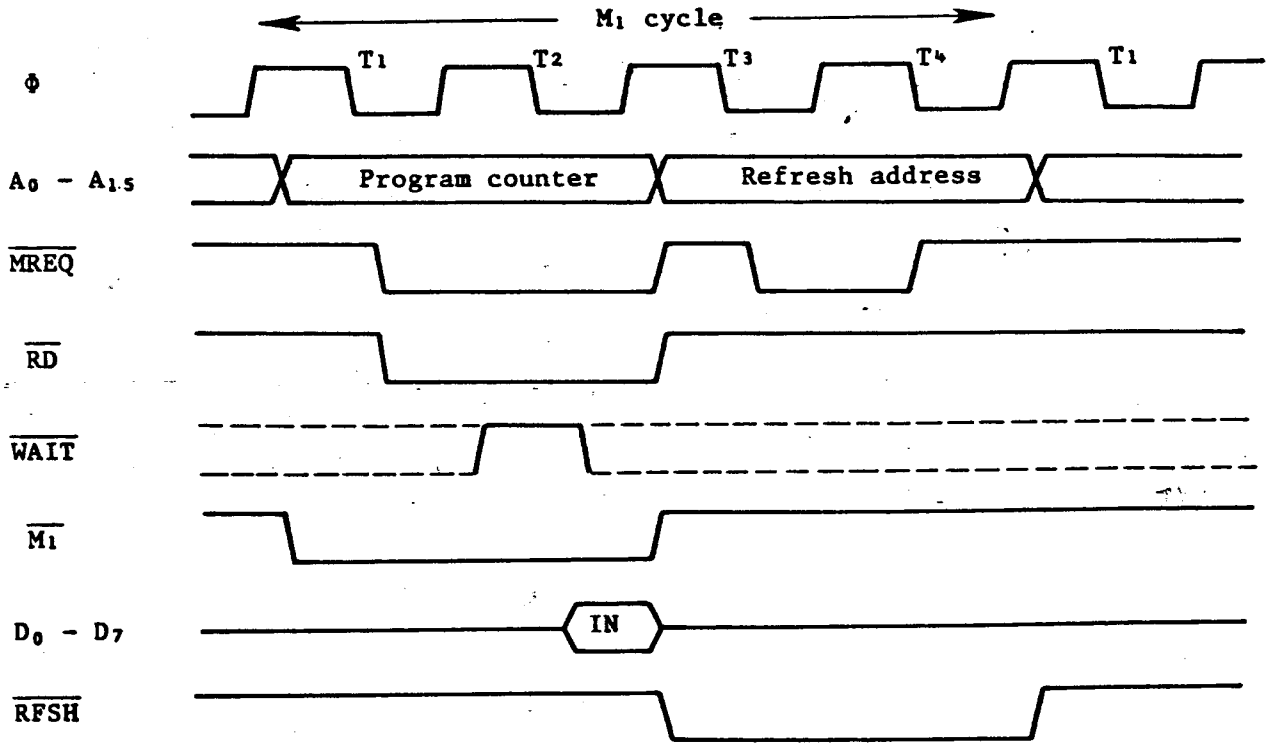
$\overline{\text{HALT}}$ (Halt)	:	Indicates that the CPU has executed a HALT instruction. While halted, the CPU executes a NOP instruction to maintain memory refresh condition. HALT condition is cancelled by a reset signal, non-maskable interruption, or maskable interruption (with the mask enabled). (Output)
$\overline{\text{WAIT}}$ (Wait)	:	Indicates to LH-0080 or LH-0080A CPU that the addressed memory or I/O devices are not ready for data transfer. (Input)
$\overline{\text{INT}}$ (Interrupt request)	:	Generated by I/O devices to request interrupt to LH-0080 or LH-0080A. A request will be accepted at the end of the current instruction if the interrupt flip-flop (IFF) is enabled. (Input)
$\overline{\text{NMI}}$ (Non-Maskable Interrupt)	:	The non-maskable interrupt line has a higher priority than $\overline{\text{INT}}$ and is not maskable even with sofrware. $\overline{\text{NMI}}$ is always accepted at the end of the current instruction and interrupt is started. $\overline{\text{NMI}}$ automatically forces the LH-0080 or LH-0080A to restart at location 0066H. (Input)
$\overline{\text{RESET}}$ (Reset)	:	Initializes LH-0080 or LH-0080A as follows. Reset interrupts enable flip-flop, program counter, interrupt vector register, and memory refresh register, and then sets interrupt mode to 0 mode. During reset time, the address and data bus enter a high impedance state and the control signals enter the inactive state. (Input)
$\overline{\text{BUSREQ}}$ (Bus Request)	:	The bus request signal has a higher priority than $\overline{\text{MNI}}$, and is always accepted at the end of the current machine cycle. (Input)
$\overline{\text{BUSAK}}$ (Bus Acknowledge)	:	Indicates that the LH-0080 or LH-0080A has accepted bus request signal and that the address bus, data bus, and tri-state control output are in their high impedance states. At this time, the external devices can utilize these bus and control lines. (Output)

SHARP

4. Timing waveforms

- Instruction OP code fetch cycle

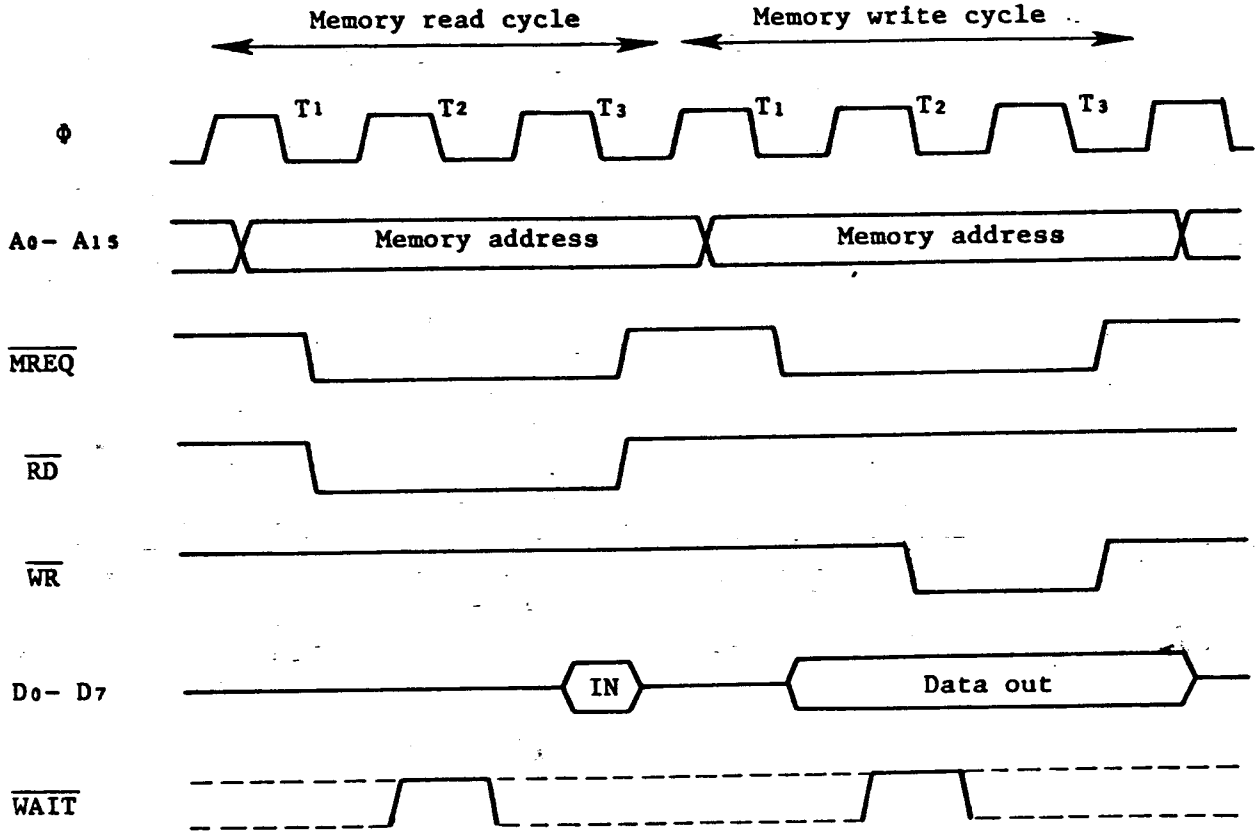
The program counter content is placed on the address bus immediately at the start of the instruction cycle. One-half clock time later, $\overline{MREQ}$ goes to L. The falling edge of $\overline{MREQ}$ can be used as a chip enable input to the dynamic memories. With an $\overline{RD}$ signal, memory data is transferred to the data bus, and the LH-0080 or LH-0080A CPU reads the data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle (referred to as M_1 cycle, in the following) are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. With $\overline{RFSH}$ signal, all dynamic memories are refreshed. At this time, the address bus holds a refresh address. The timing is shown in the following chart.



SHARP

° Memory access timing

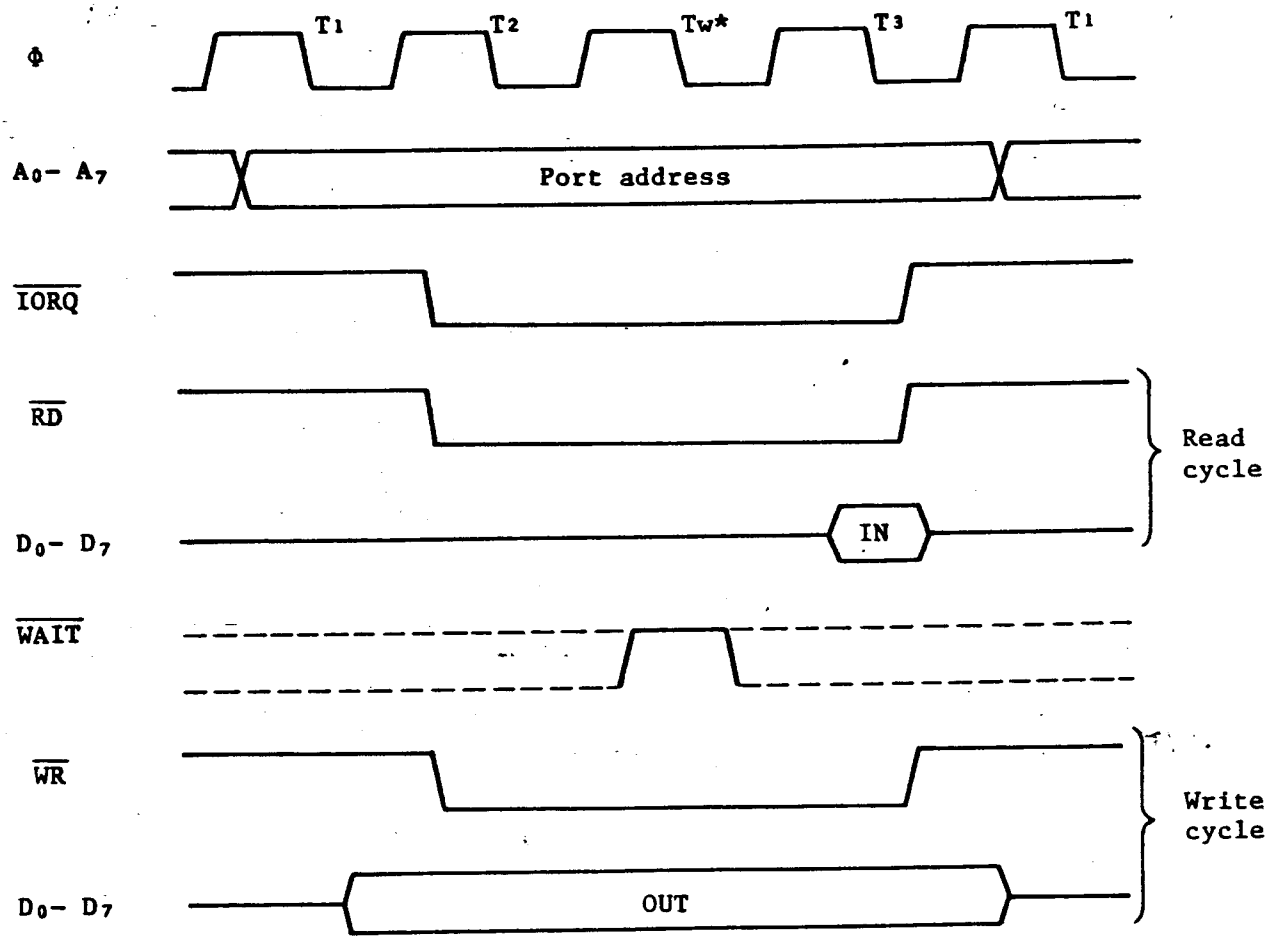
The following chart shows the timing of memory access except for the M1 cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the M1 cycle. The $\overline{MREQ}$ goes to L when the address bus is stable so that it can be used directly as a chip enable input for dynamic memories. In the memory write cycle, $\overline{WR}$ goes to L when the data bus is stable so that it can be used directly as a R/W pulse to general RAM.



SHARP

- Input/Output cycle

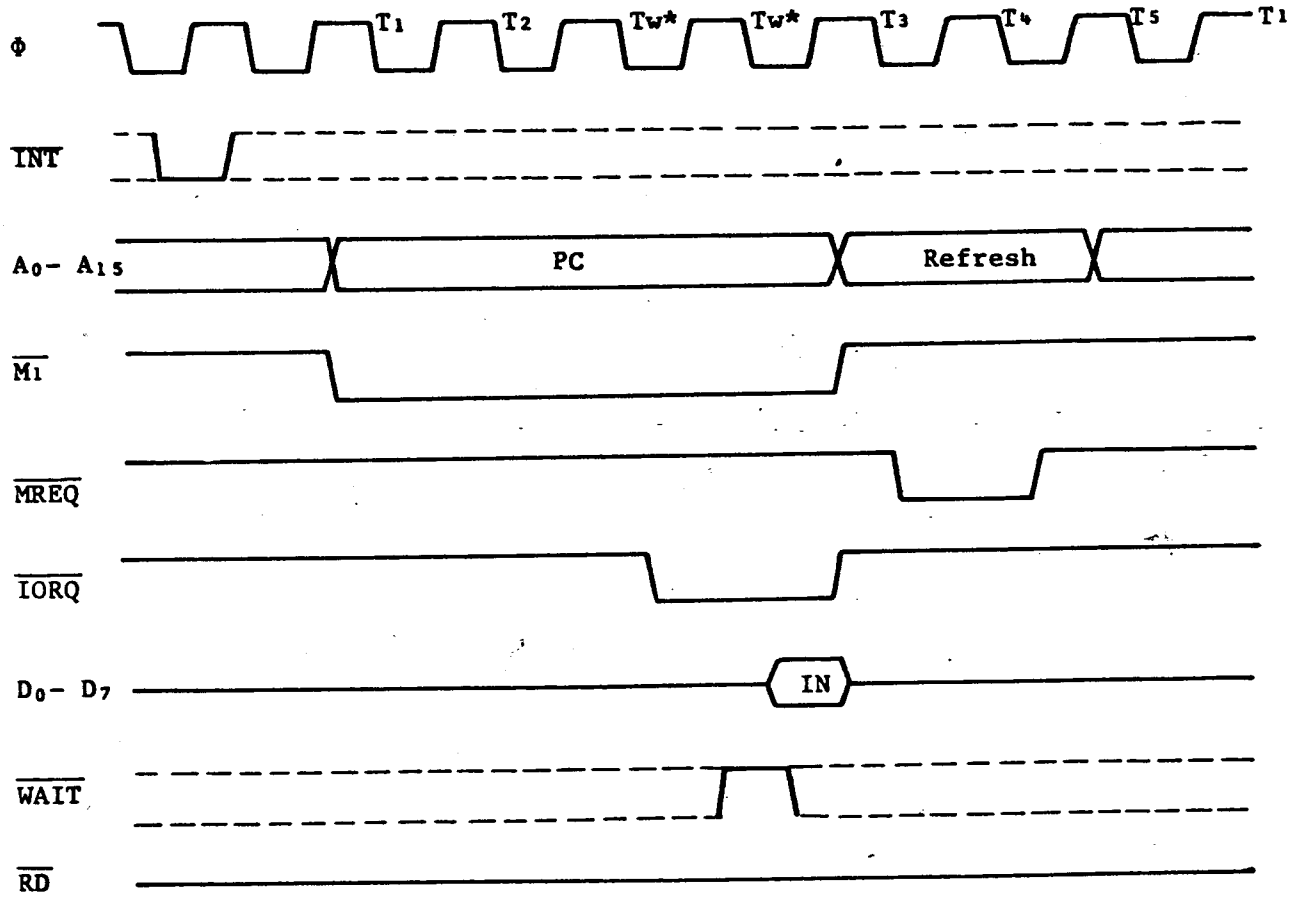
The following chart shows the timing of the I/O cycle. During I/O operations, the LH-0080 or LH-0080A automatically inserts a single wait state (Tw*) to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



SHARP

- Interrupt request/Acknowledge cycle

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of an instruction. When an interrupt is accepted, a special M1 cycle is started. During the special M1 cycle, the $\overline{IORQ}$ signal (instead of $\overline{MREQ}$) becomes active to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that the ripple priority interrupt scheme used in the peripherals can be implemented. The timing is shown in the chart below.



[NOTE] When a CALL instruction is executed with mode 0, cycle T_5 is not generated and the M_1 cycle is composed of six clock cycles.

SHARP

5. Instruction set

The following is a summary of the LH-0080 or LH-0080A instruction set. The instructions are expressed in the assembly language mnemonic.

In the table the following terminology is used.

b : a bit number in any 8-bit register or memory location
cc : flag condition code
- NZ : non zero
- Z : zero
- NC : non carry
- C : carry
- PO : parity odd or no overflow
- PE : parity even or overflow
- P : positive
- M : negative (minus)

d : 8-bit data storage location when an instruction is executed.
dd : 16-bit data storage location when an instruction is executed.
e : 8-bit signed binary number used to calculate relative address or index address.
p : Special address for zero page.
n : 8-bit binary number
nn : 16-bit binary number
r : 8-bit general purpose register (A, B, C, D, E, H, or L)
s : 8-bit data source used to execute an instruction
Sb : A bit in a specific 8-bit register or memory location
ss : 16-bit data source used to execute an instruction
subscript L : the low order 8 bits of a 16-bit register
subscript H : the high order 8 bits of a 16-bit register
( ) : The contents within parentheses are for use as pointers to a memory location or I/O port number.

7-bit register is R
8-bit registers are A, B, C, D, E, H, L, and I.
16-bit registers are SP, PC, IX, and IY.

Addressing modes include any combination of the following :

Immediate
Immediate extended
Modified zero page
Relative
Direct
Index
Register
Implied
Register indirect
Bit

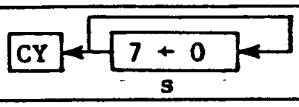
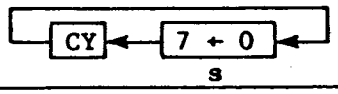
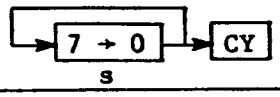
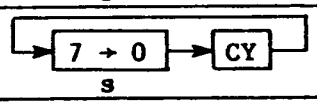
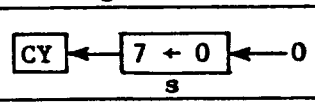
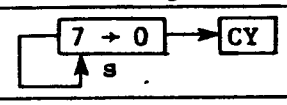
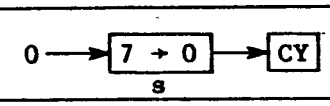
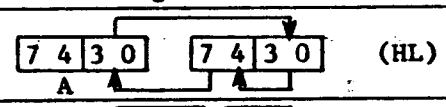
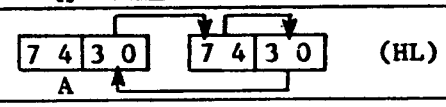
SHARP

	Mnemonic	Operation	Comments
8-bit loads	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ r, (HL), (IX+e) (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ same as the above
16-bit loads	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	
	LD (nn), ss	(nn) ← ss	ss ≡ same as the above
	LD SP, ss	SP ← ss	ss ≡ HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$, $(SP-2) \leftarrow ss_L$	ss ≡ BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$, $dd_H \leftarrow (SP+1)$	dd ≡ same as the above
Exchanges	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY
Memory block moves	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	Repeat LDI until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	Repeat LDD until BC = 0	
Memory block searches	CPI	A-(HL), HL ← HL+1 BC ← BC-1	A-(HL) sets the flags only. A is not affected.
	CPIR	Repeat CPI until BC=0 or A=(HL)	
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	Repeat CPD untio BC=0 or A=(HL)	

SHARP

	Mnemonic	Operation	Comments
8-bit arithmetic	ADD A, s	A ← A + s	CY is the carry flag. s ≡ r, n, (HL), (IX+e), (IY+e)
	ADC A, s	A ← A + s + CY	
	SUB s	A ← A − s	
	SBC A, s	A ← A − s − CY	
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	
	CP s	A − s	A content is not affected.
	INC d DEC d	d ← d + 1 d ← d − 1	d ≡ r, (HL), (IX+e), (IY+e)
16-bit arithmetic	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE, HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL − ss − CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP IX, IY
	DEC dd	dd ← dd − 1	
Accumulator & flag	DAA	Perform decimal correction of A after adding or subtracting.	Operands must be in packed BCD format.
	CPL	$A \leftarrow \overline{A}$	
	NEG	$A \leftarrow 00_H - A$	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
CPU control	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable interrupts	
	EI	Enable interrupts	

SHARP

	Mnemonic	Operation	Comments
CPU control (cont.)	IM 0	Set interrupt mode 0	same as 8080A
	IM 1	Set interrupt mode 1	Restart from 0038_{16}
	IM 2	Set interrupt mode 2	Use register I to make indirect call
Rotates & Shifts	RLC s		s ≡ r, (HL), (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD	 (HL)	
	RRD	 (HL)	
Bit Operation	BIT b, s	Z ← $\overline{Sb}$	Z is zero flag.
	SET b, s	Sb ← 1	s ≡ r, (HL), (IX+e), (IY+e)
	RES b, s	Sb ← 0	
Re-starts	RST p	(SP - 1) ← PC_H, (SP - 2) ← PC_L PC_H ← 0, PC_L ← L	
Input & Output	IN A, (n)	A ← (n)	Set flags.
	IN r, (C)	r ← (C)	
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	Repeat INI until B = 0	

SHARP

	Mnemonic	Operation	Comments
Input & Output (cont.)	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	Set flags.
	INDR	Repeat IND until B = 0	
	OUT (n), A	(n) ← A	
	OUT (C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	Repeat OUTI until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	Repeat OUTD until B = 0	
Jumps	JP nn	PC ← nn	cc { NZ PO; Z PE; NC P; C M
	JP cc, nn	If condition cc is true, PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true, PC ← PC + e, else continue	kk { NZ NC; Z C
	JP (ss)	PC ← ss	ss HL, IX, IY
	DJNZ e	B ← B-1, if B=0, continue, else PC ← PC + e	
Calls	CALL nn	(SP - 1) ← PC_H, (SP - 2) ← PC_L PC ← nn	
	CALL cc, nn	If condition cc is false, continue; else same as CALL nn.	cc { NZ PO; Z PE; NC P; C M
Returns	RET	PC_L ← (SP), PC_H ← (SP + 1)	cc { NZ PO; Z PE; NC P; C M
	RET cc	If condition cc is true, same as RET, else continue.	
	RETI	Return from interrupt, same as RET.	
	RETN	Return from non-maskable interrupt.	

SHARP

6. LH-0080 (Z80-CPU) Absolute maximum ratings

Ambient temperature under bias	0°C ∿ + 70°C
Storage temperature	-65°C ∿ +150°C
Input voltage	-0.3V ∿ + 7V
Output voltage	-0.3V ∿ + 7V

7. LH-0080 (Z80-CPU) Electrical characteristics

7-1 D.C. Characteristics

T_A=0°C ∿+70°C, V_{CC}=+5V±5%

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{ILC}	Clock input low voltage	-0.3	0.45	V	
V_{IHC}	Clock input high voltage	V_{CC}-0.6	V_{CC}+0.3	V	
V_{IL}	Input low voltage	-0.3	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}	V	
V_{OL}	Output low voltage		0.4	V	I_{OL}=1.8mA
V_{OH}	Output high voltage	2.4		V	I_{OH}=250μA
I_{CC}	Current consumption		150	mA	
I_{LI}	Input leakage current		10	μA	V_{IN}=0∿V_{CC}
I_{LOH}	Tri-state output leakage current		10	μA	V_{OUT}=2.4 ∿V_{CC}
I_{LOL}	Tri-state output leakage current		10	μA	V_{OUT}=0.4
I_{LD}	Data bus leakage current in input mode		±10	μA	$0 \leq V_{IN} \leq V_{CC}$

7-2 Pin Capacitance

T_A=+25°C, f=1MHz

Symbol		Max.	Unit	Condition
C_ϕ	Clock input capacitance	35	pF	Unmeasured pins tied to ground.
C_{IN}	Input capacitance	5	pF	
C_{OUT}	Output capacitance	10	pF	

16

SHARP

7-3 A.C. Characteristics

T_A=0°C ∿ +70°C, V_{CC}=+5V±5%

Signal	Symbol		Min.	Max.	Unit	
Φ	tc	Clock period	0.4	200	μs	
	$t_w(\Phi_H)$	Clock pulse width (H)	180		ns	
	$t_w(\Phi_L)$	Clock pulse width (L)	180	2000	ns	
	t_r. t_f	Clock rise and fall time		30	ns	
A_0-A_{15}	t_D(AD)	Output delay from rising edge of clock		145	ns	C_L=50pF
	t_F(AD)	Delay to float		110	ns	
	t_{acm}	Output stable time prior to $\overline{MREQ}$ (Memory cycle)	[1]		ns	
	t_{aci}	Output stable time prior to $\overline{IORQ}$, $\overline{RD}$, or $\overline{WR}$ (I/O cycle)	[2]		ns	
	t_{ca}	Output stable time from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, or $\overline{MREQ}$	[3]		ns	
	t_{caf}	Output stable time from $\overline{RD}$ or $\overline{WR}$ (during float)	[4]		ns	
D_0-D_7	t_D (D)	Output delay from falling edge of clock		230	ns	C_L=50pF
	t_F (D)	Delay to float during write cycle		90	ns	
	$t_{s\Phi}$(D)	Data setup time to rising edge of clock during M_1 cycle	50		ns	
	$t_{s\overline{\Phi}}$(D)	Data setup time to falling edge of clock during M_2 to M_5 cycles	60		ns	
	t_{dcm}	Output stable time prior to $\overline{WR}$ (memory cycle)	[5]		ns	
	t_{dci}	Output stable time prior to $\overline{WR}$ (I/O cycle)	[6]		ns	
	t_{cdf}	Output stable time from $\overline{WR}$	[7]		ns	
	t_H	Any hold time for setup time	0		ns	
$\overline{MREQ}$	$t_{DL\overline{\Phi}}$(MR)	Delay from falling edge of clock to $\overline{MREQ}$=L		100	ns	C_L=50pF

SHARP

Signal	Symbol		Min.	Max.	Unit	
$\overline{MREQ}$	$t_{DH\phi}(MR)$	Delay from rising edge of clock to $\overline{MREQ}$ = H during M_1 cycle		100	ns	C_L=50pF
	$t_{DH\overline{\phi}}(MR)$	Delay from falling edge of clock to $\overline{MREQ}$ = H during M_2 to M_5 cycles		100	ns	
	$t_w(\overline{MR_L})$	$\overline{MREQ}$ pulse width (L)	[8]		ns	
	$t_w(\overline{MR_H})$	$\overline{MREQ}$ pulse width (H)	[9]		ns	
$\overline{IORQ}$	$t_{DL\phi}(IR)$	Delay from rising edge of clock to $\overline{IORQ}$ = L during I/O cycle		90	ns	C_L=50pF
	$t_{DL\overline{\phi}}(IR)$	Delay from falling edge of clock to $\overline{IORQ}$ = L during INTA cycle		110	ns	
	$t_{DH\phi}(IR)$	Delay from rising edge of clock to $\overline{IORQ}$ = H during INTA cycle		100	ns	
	$t_{DH\overline{\phi}}(IR)$	Delay from falling edge of clock to $\overline{IORQ}$ = H during I/O cycle		110	ns	
$\overline{RD}$	$t_{DL\phi}(RD)$	Delay from rising edge of clock to $\overline{RD}$ = L during I/O cycle		100	ns	C_L=50pF
	$t_{DL\overline{\phi}}(RD)$	Delay from falling edge of clock to $\overline{RD}$ = L during memory cycle		130	ns	
	$t_{DH\phi}(RD)$	Delay from rising edge of clock to $\overline{RD}$ = H during M_1 cycle		100	ns	
	$t_{DH\overline{\phi}}(RD)$	Delay from falling edge of clock to $\overline{RD}$ = H during M_2 to M_5 cycles.		110	ns	
$\overline{WR}$	$t_{DL\phi}(WR)$	Delay from rising edge of clock to $\overline{WR}$ = L during I/O cycle		80	ns	C_L=50pF
	$t_{DL\overline{\phi}}(WR)$	Delay from falling edge of clock to $\overline{WR}$ = L during memory cycle		90	ns	
	$t_{DH\overline{\phi}}(WR)$	Delay from falling edge of clock to $\overline{WR}$ = H		100	ns	
	$t_w(\overline{WRL})$	$\overline{WR}$ pulse width (L)	[10]			
$\overline{M1}$	$t_{DL}(M1)$	Delay from rising edge of clock to M_1 = L		130	ns	C_L=50pF
	$t_{DH}(M1)$	Delay from rising edge of clock to M_1 = H		130	ns	
$\overline{RFSH}$	$t_{DL}(RF)$	Delay from rising edge of clock to $\overline{RESH}$ = L		180	ns	C_L=50pF
	$t_{DH}(RF)$	Delay from rising edge of clock to $\overline{RESH}$ = H		150	ns	

SHARP

Signal	Symbol		Min.	Max.	Unit	
$\overline{WAIT}$	$t_s(WT)$	Setup time to falling edge of clock	70		ns	
$\overline{HALT}$	$t_D(HT)$	Delay from falling edge of clock		300	ns	C_L=50pF
$\overline{INT}$	$t_s(IT)$	Setup time to rising edge of clock	80		ns	
$\overline{NMI}$	$t_w(\overline{NM_L})$	$\overline{NMI}$ pulse width (L)	80		ns	
$\overline{BUSRQ}$	$t_s(BQ)$	Setup time to rising edge of clock	80		ns	
$\overline{BUSAK}$	$t_{DL}(BA)$	Delay from rising edge of clock to $\overline{BUSAK}$ = L		120	ns	C_L=50pF
	$t_{DH}(BA)$	Delay from falling edge of clock to $\overline{BUSAK}$ = H		110	ns	
$\overline{RESET}$	$t_s(RS)$	Setup time to rising edge of clock	90		ns	
	$t_F(C)$	Delay to float state ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)		100	ns	
	t_{mr}	Stable time of $\overline{M_1}$ output (L) prior to $\overline{IORQ}$ (during INTA cycle)	[11]		ns	

[NOTE]

[1] $t_{acm} = t_w(\Phi_H) + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_w(\Phi_L) + t_r - 40$

[4] $t_{caf} = t_w(\Phi_L) + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_w(\Phi_L) + t_r - 210$

[7] $t_{cdf} = t_w(\Phi_L) + t_r - 80$

[8] $t_w(\overline{MR_L}) = t_c - 40$

[9] $t_w(\overline{MR_H}) = t_w(\Phi_H) + t_f - 30$

[10] $t_w(\overline{WR_L}) = t_c - 40$

[11] $t_{mr} = 2t_c + t_w(\Phi_H) + t_f - 80$

- Data should be transferred to the data bus in synchronization with $\overline{RD}$. During interrupt acknowledge cycle, transfer data in synchronization with both $\overline{M_1}$ and $\overline{IORQ}$.
- All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- Relation between load capacitance and output delay when

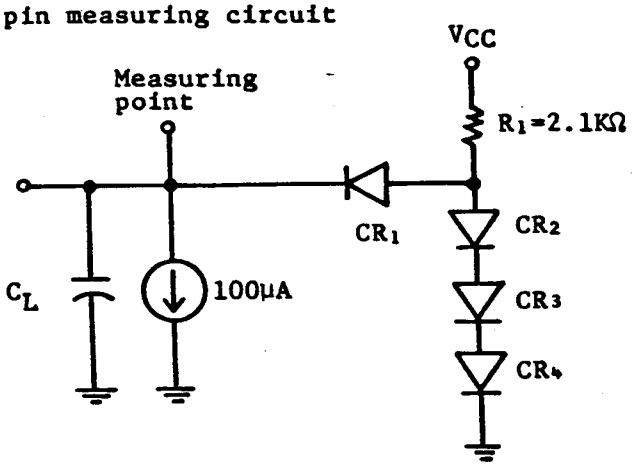
  T_A = +70°C, V_{CC} = +5V ± 5%

  With a 50pF increase in load capacitance, delay increases 10ns. The maximum load capacitance for the data bus is 200pF, and that for the others is 100pF.

SHARP

- The minimum $\overline{\text{RESET}}$ input width requires three clock cycles.

Output pin measuring circuit



CR_{1-4} : 1N914 or equivalent.

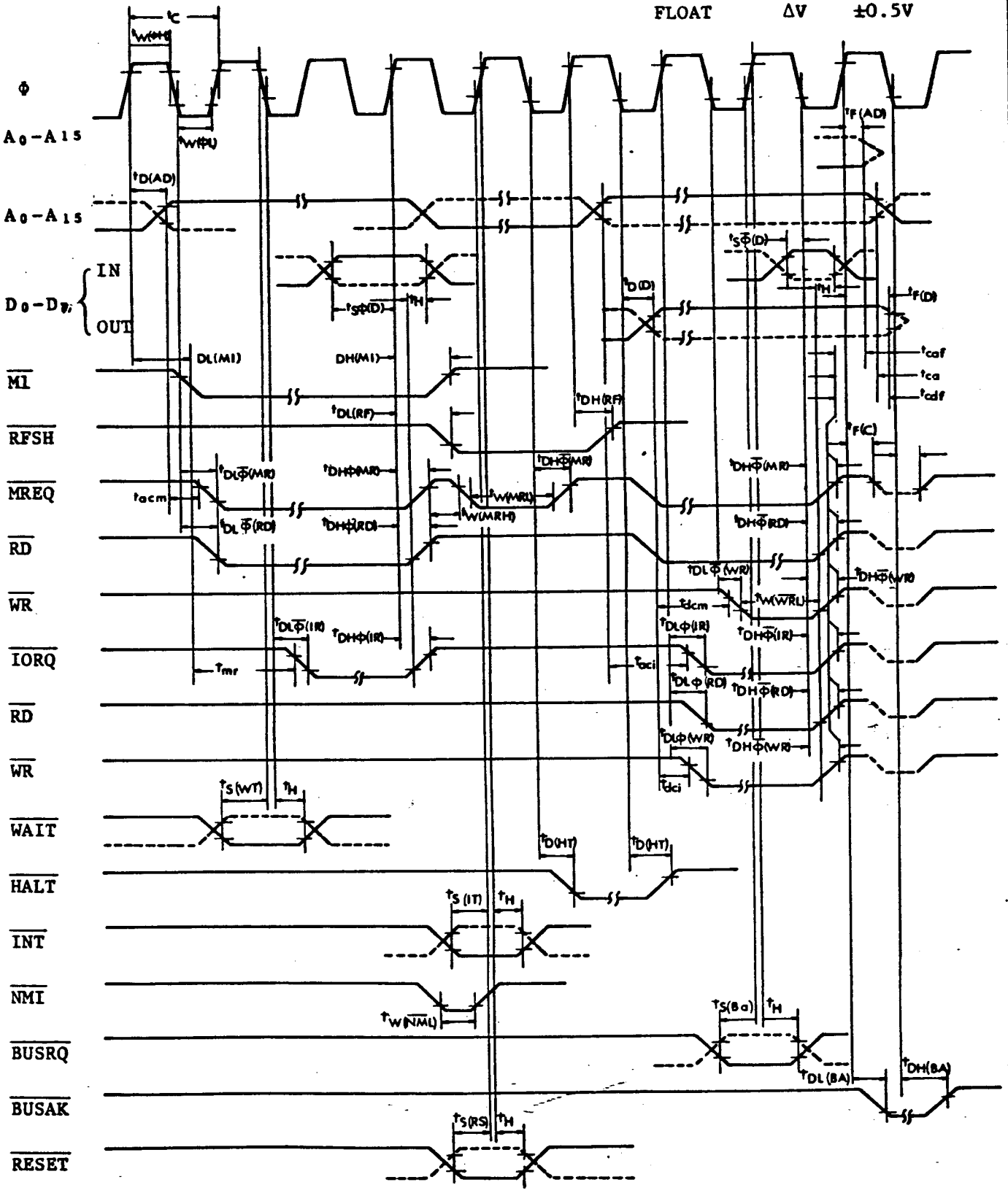
C_L : 50pF for all pins.

SHARP

7-4 A.C. timing chart

Measuring conditions are as follows ;

	"H"	"L"
CLOCK	V_{CC}-.6V	.45V
OUTPUT	2.0V	.8V
INPUT	2.0V	.8V
FLOAT	ΔV	±0.5V



SHARP

6'. LH-0080A (Z80A-CPU) Absolute maximum ratings

Ambient temperature under bias	0°C ∿ + 70°C
Storage temperature	-65°C ∿ +150°C
Input voltage	-0.3V ∿ + 7V
Output voltage	-0.3V ∿ + 7V

7'. LH-0080A (Z80A-CPU) Electrical characteristics

7'-1 D.C. Characteristics

T_A=0°C ∿+70°C, V_{CC}=+5V±5%

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{ILC}	Clock input low voltage	-0.3	0.45	V	
V_{IHC}	Clock input high voltage	V_{CC}-0.6	V_{CC}+0.3	V	
V_{IL}	Input low voltage	-0.3	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}	V	
V_{OL}	Output low voltage		0.4	V	I_{OL}=1.8mA
V_{OH}	Output high voltage	2.4		V	I_{OH}=250μA
I_{CC}	Current consumption		200	mA	
I_{LI}	Input leakage current		10	μA	V_{IN}=0 ∿ V_{CC}
I_{LOH}	Tri-state output leakage current		10	μA	V_{OUT}=2.4 ∿ V_{CC}
I_{LOL}	Tri-state output leakage current		10	μA	V_{OUT}=0.4
I_{LD}	Data bus leakage current in input mode		±10	μA	$0 \leq V_{IN} \leq V_{CC}$

7'- 2 Pin Capacitance

T_A=+25°C, f=1MHz

Symbol		Max.	Unit	Condition
C_Φ	Clock input capacitance	35	pF	Unmeasured pins tied to ground.
C_{IN}	Input capacitance	5	pF	
C_{OUT}	Output capacitance	10	pF	

SHARP

7'-3 A.C. Characteristics

T_A=0°C +70°C, V_{CC}=+5V±5%

Signal	Symbol		Min.	Max.	Unit	
Φ	t_c	Clock period	0.25	200	μs	
	$t_w(\Phi H)$	Clock pulse width (H)	110		ns	
	$t_w(\Phi L)$	Clock pulse width (L)	110	2000	ns	
	t_r, t_f	Clock rise and fall time		30	ns	
A_0-A_{15}	$t_D(AD)$	Output delay from rising edge of clock		110	ns	C_L=50pF
	$t_F(AD)$	Delay to float		90	ns	
	t_{acm}	Output stable time prior to $\overline{MREQ}$ (Memory cycle)	[1]		ns	
	t_{aci}	Output stable time prior to $\overline{IORQ}$, $\overline{RD}$, or $\overline{WR}$ (I/O cycle)	[2]		ns	
	t_{ca}	Output stable time from $\overline{RD}$, $\overline{WR}$, $\overline{IROQ}$, or $\overline{MREQ}$	[3]		ns	
	t_{caf}	Output stable time from $\overline{RD}$ or $\overline{WR}$ (during float)	[4]		ns	
D_0-D_7	t_D (D)	Output delay from falling edge of clock		150	ns	C_L=50pF
	t_F (D)	Delay to float during write cycle		90	ns	
	$t_{s\Phi}$(D)	Data setup time to rising edge of clock during M_1 cycle	35		ns	
	$t_{s\overline{\Phi}}$(D)	Data setup time to falling edge of clock during M_2 to M_5 cycles	50		ns	
	t_{dcm}	Output stable time prior to $\overline{WR}$ (memory cycle)	[5]		ns	
	t_{dci}	Output stable time prior to $\overline{WR}$ (I/O cycle)	[6]		ns	
	t_{cdf}	Output stable time from $\overline{WR}$	[7]		ns	
	t_H	Any hold time for setup time	0		ns	
$\overline{MREQ}$	$t_{DL\overline{\Phi}}(MR)$	Delay from falling edge of clock to $\overline{MREQ}$=L		85	ns	C_L=50pF

SHARP

Signal	Symbol		Mix.	Max.	Unit	
$\overline{MREQ}$	$t_{DH\phi}(MR)$	Delay form rising edge of clock to $\overline{MREQ}$ = H during M_1 cycle		85	ns	C_L=50pF
	$t_{DH\bar{\phi}}(MR)$	Delay from falling edge of clock to $\overline{MREQ}$ = H during M_2 to M_5 cycles		85	ns	
	$t_w(\overline{MR_L})$	$\overline{MREQ}$ pulse width (L)	[8]		ns	
	$t_w(\overline{MR_H})$	$\overline{MREQ}$ pulse width (H)	[9]		ns	
$\overline{IORQ}$	$t_{DL\phi}(IR)$	Delay from rising edge of clock to $\overline{IORQ}$ = L during I/O cycle		75	ns	C_L=50pF
	$t_{DL\bar{\phi}}(IR)$	Delay from falling edge of clock to $\overline{IORQ}$ = L during INTA cycle		85	ns	
	$t_{DH\phi}(IR)$	Delay from rising edge of clock to $\overline{IORQ}$ = H during INTA cycle		85	ns	
	$t_{DH\bar{\phi}}(IR)$	Delay from falling edge of clock to $\overline{IORQ}$ = H during I/O cycle		85	ns	
$\overline{RD}$	$t_{DL\phi}(RD)$	Delay from rising edge of clock to $\overline{RD}$ = L during I/O cycle		85	ns	C_L=50pF
	$t_{DL\bar{\phi}}(RD)$	Delay from falling edge of clock to $\overline{RD}$ = L during memory cycle		95	ns	
	$t_{DH\phi}(RD)$	Delay from rising edge of clock to $\overline{RD}$ = H during M_1 cycle		85	ns	
	$t_{DH\bar{\phi}}(RD)$	Delay from falling edge of clock to $\overline{RD}$ = H during M_2 to M_5 cycles.		85	ns	
$\overline{WR}$	$t_{DL\phi}(WR)$	Delay from rising edge of clock to $\overline{WR}$ = L during I/O cycle		65	ns	C_L=50pF
	$t_{DL\bar{\phi}}(WR)$	Delay from falling edge of clock to $\overline{WR}$ = L during memory cycle		80	ns	
	$t_{DH\bar{\phi}}(WR)$	Delay from falling edge of clock to $\overline{WR}$ = H		80	ns	
	$t_w(\overline{WR_L})$	$\overline{WR}$ pulse width (L)	[10]			
$\overline{M1}$	$t_{DL}(M1)$	Delay from rising edge of clock to $\overline{M_1}$ = L		100	ns	C_L=50pF
	$t_{DH}(M1)$	Delay from rising edge of clock to $\overline{M_1}$ = H		100	ns	
$\overline{RFSH}$	$t_{DL}(RF)$	Delay from rising edge of clock to $\overline{RESH}$ = L		130	ns	C_L=50pF
	$t_{DH}(RF)$	Delay from rising edge of clock to $\overline{RESH}$ = H		120	ns	

SHARP

Signal	Symbol		Min.	Max.	Unit	
$\overline{WAIT}$	$t_s(WT)$	Setup time to falling edge of clock	70		ns	
$\overline{HALT}$	$t_D(HT)$	Delay from falling edge of clock		300	ns	C_L=50pF
$\overline{INT}$	$t_s(IT)$	Setup time to rising edge of clock	80		ns	
$\overline{NMI}$	$t_w(\overline{NM_L})$	$\overline{NMI}$ pulse width (L)	80		ns	
$\overline{BUSRQ}$	$t_s(BQ)$	Setup time to rising edge of clock	50		ns	
$\overline{BUSAK}$	$t_{DL}(BA)$	Delay from rising edge of clock to $\overline{BUSAK}$ = L		100	ns	C_L=50pF
	$t_{DH}(BA)$	Delay from falling edge of clock to $\overline{BUSAK}$ = H		100	ns	
$\overline{RESET}$	$t_s(RS)$	Setup time to rising edge of clock	60		ns	
	$t_F(C)$	Delay to float state ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)		80	ns	
	t_{mr}	Stable time of $\overline{M_1}$ output (L) prior to $\overline{IORQ}$ (during INTA cycle)	[11]		ns	

[NOTE]

[1] $t_{acm} = t_w(\Phi_H) + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_w(\Phi_L) + t_r - 50$

[4] $t_{caf} = t_w(\Phi_L) + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_w(\Phi_L) + t_r - 170$

[7] $t_{cdf} = t_w(\Phi_L) + t_r - 70$

[8] $t_w(\overline{MR_L}) = t_c - 30$

[9] $t_w(\overline{MR_H}) = t_w(\Phi_H) + t_f - 20$

[10] $t_w(\overline{WR_L}) = t_c - 30$

[11] $t_{mr} = 2t_c + t_w(\Phi_H) + t_f - 65$

- Data should be transferred to the data bus in synchronization with $\overline{RD}$. During interrupt acknowledge cycle, transfer data in synchronization with both $\overline{M_1}$ and $\overline{IORQ}$.
- All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- Relation between load capacitance and output delay when
  T_A = +70°C, V_{CC} = +5V ±5%
  With a 50pF increase in load capacitance, delay increases 10ns. The maximum load capacitance for the data bus is 200pF, and that for the others is 100pF.
- The minimum $\overline{RESET}$ input width requires three clock cycles.

SHARP

1. Package specifications
   Refer to Fig. AA176-00.

2. Marking specifications

2-1 Contents
The following items must be marked on each product body.

(1) Product name : LH-0080 Z80-CPU

(2) Company name : SHARP

(3) Date code : (Example)

9 H 2001 (This means Aug. 1979.)

- 2001 — Lot No.
- H — A - L shows month.
- 9 — The last digit of year

2-2 Position and direction
Refer to Fig. AA176-00.

2-3 Marking color
SILVER

3. Crating specifications

3-1 Crating materials

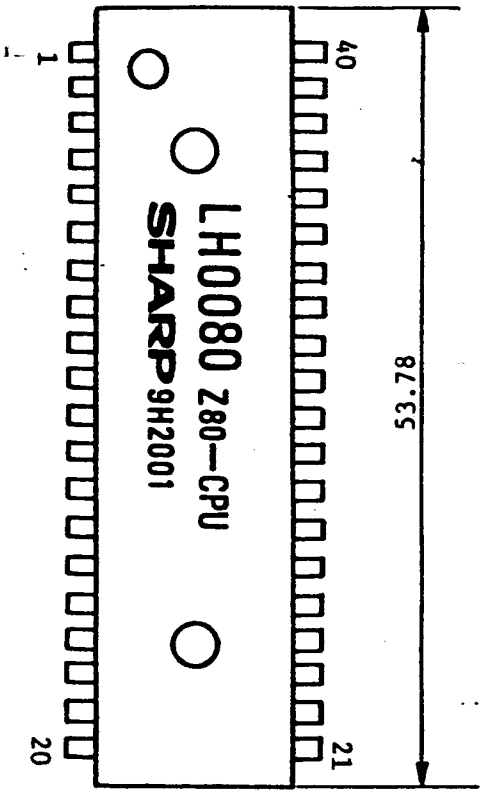
Material Name	Material Specifications	Purpose
Package case	Paper (Includes 60 pcs.)	Package
Cushion-1	Semiconduction moltplane 2pcs.	Package fixing, electrical short
Cushion-2	General moltplane 3 pcs.	Package buffer
Cellophane tape		Package case lid fixing
Crating case	Corrugated paper (Includes 40 package cases.)	Outer package

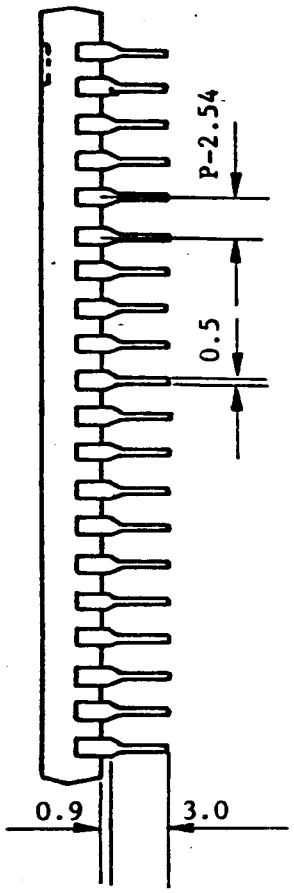
3-2 Crating procedure

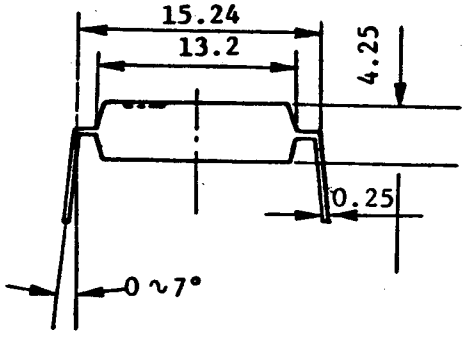
(1) Place cushion-2 in case.
(2) Insert package into cushion-1 and place into package case.
(3) Put cushion-2, after completing above steps, into case.
(4) Attach cover and secure with cellophane tape.
(5) Mark quantity and manufacturing date on the side of the case.
(6) Place cases into a crate. Mark product name and quantity on the crate.

3-3 External view of crate
Refer to Fig. BJ015-00.

SHARP

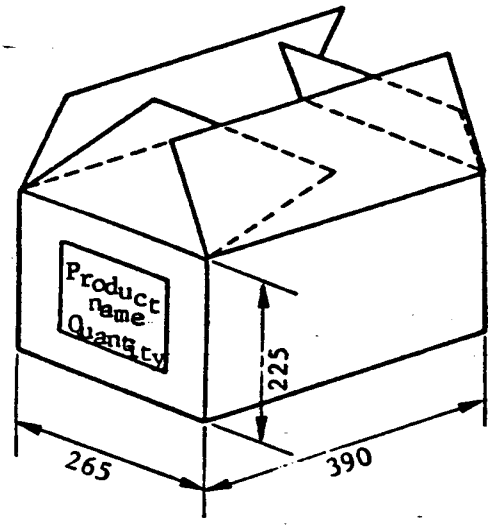


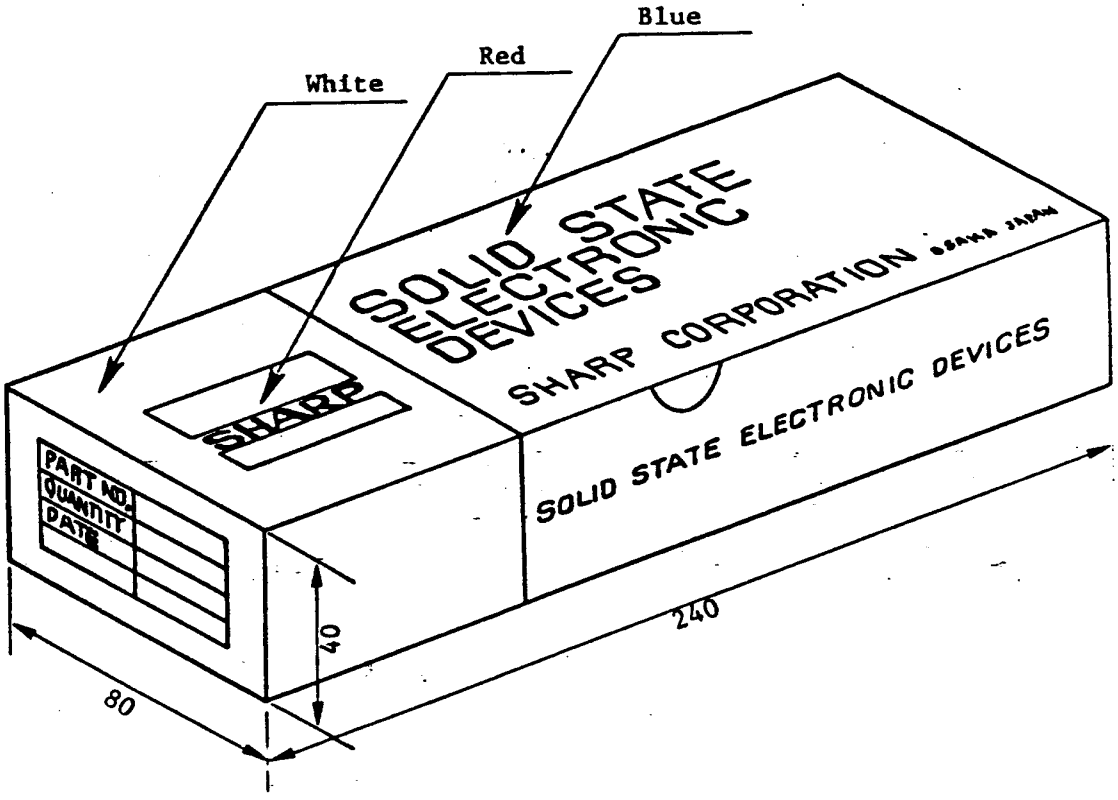




適用機種 APPLICABLE MODEL		尺度 SCALE 2/1	単位 UNIT 1=m/m		
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	DPT40AP
0.25t					
日付 DATE 1979 8. 22				コード CODE	
設計 DESIGN 製図 DRAW 写図 TRACE 検図 CHECK 承認 APPROVE		シャープ株式会社 電子部品事業本部			

27





適用機種 APPLICABLE MODEL: LH-0080 Z80-CPU		SCALE	UNIT: m / m	△ DATE △ REVISE
THICKNESS	PIECES	MATERIAL	FINISH	NAME: Package crating case
DATE: 1979. 8 . 15				CODE
DESIGN DRAW TRACE CHECK APPROVE		シャープ株式会社		

SHARP

1. Package specifications
   Refer to Fig. AA177-00.

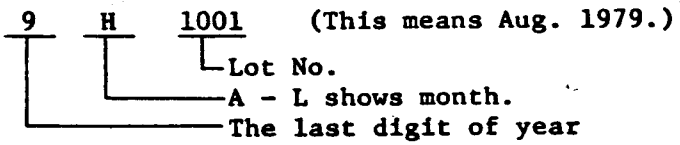
2. Marking specifications

2-1 Contents
The following items must be marked on each product body.

(1) Product name : LH-0080 Z80-CPU

(2) Company name : SHARP

(3) Date code : (Example)



2-2 Position and direction
Refer to Fig. AA177-00.

2-3 Marking color
RED

3. Crating specifications

3-1 Crating materials

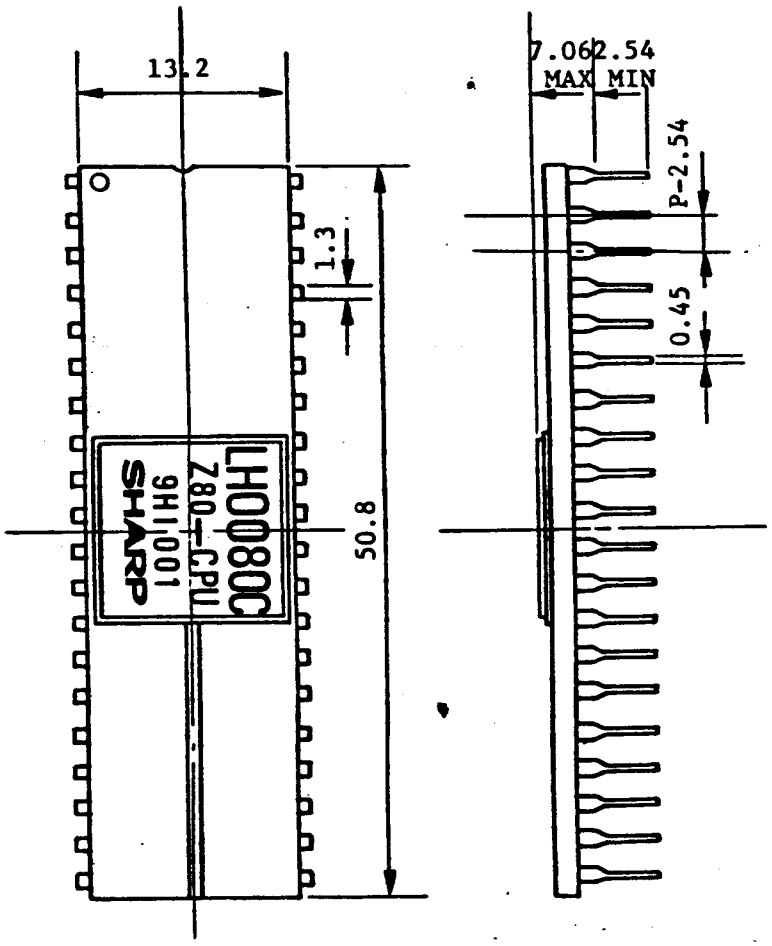
Material Name	Material Specifications	Purpose
Packing case	Plastic (Includes 10 pcs.)	Package
Cushion-1	Semiconducting moltplane	Package fixing
Cushion-2	General moltplane	Buffer
Cellophane tape		Package case lid fixing
Label	Paper	Product name, quantity indication
Crating case	Corrugated paper (Includes 40 package cases.)	Package case crating

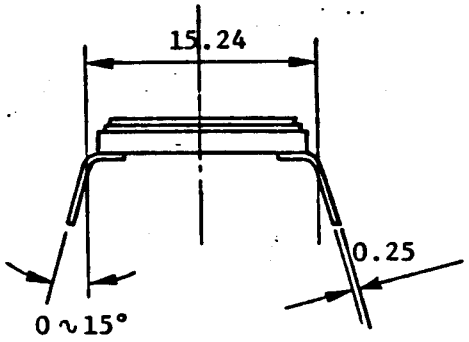
3-2 Crating procedure

(1) Place cushion-2 in case.
(2) Insert package into cushion-1 and place into package case.
(3) Put cushion-2, after completing above steps, into case.
(4) Attach cover and secure with cellophane tape.
(5) Mark quantity and manufacturing date on the side of the case.

3-3 External view of crate
Refer to Fig. BJ014-00.

SHARP

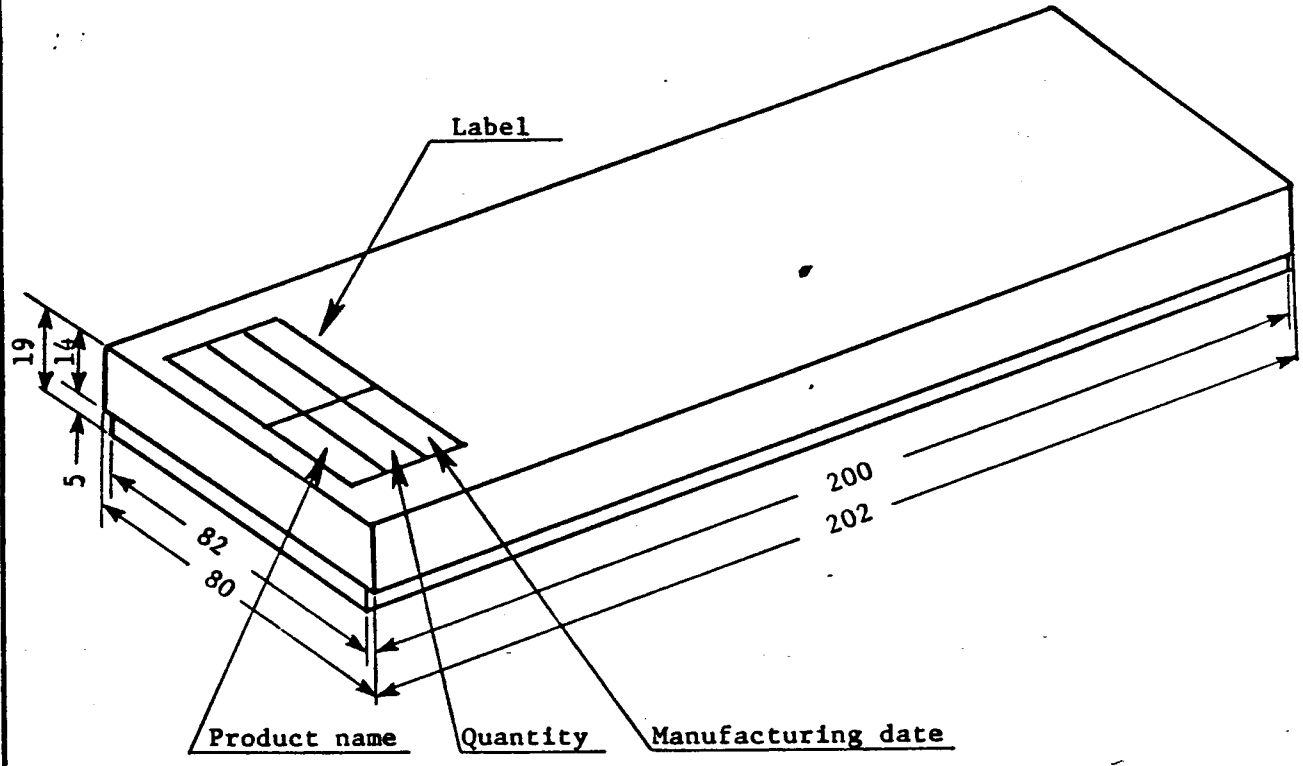




[NOTE]
- Unit : mm
- The body is ceramic finished.
- External leads should be gilded.

適用機種 APPLICABLE MODEL	LH-0080C Z80-CPU	尺度 SCALE 2／1	単位 UNIT 1＝m／m	△ . . △ . .	
				改訂日 DATE	改訂記事 REVISE 担当 CHARGE
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	DP40AK Package
		Ceramic			
日付 DATE	1979. 8. 22			コード CODE	
設計 DESIGN 製図 DRAW 写図 TRACE	検図 CHECK 承認 APPROVE	シャープ株式会社 電子部品事業本部			

SHARP



* 10 pcs.

適用機種 APPLICABLE MODEL	LH-0080C Z80-CPU	尺度 SCALE	単位 UNIT	△ . .		
		/	1 = m/m	△ . .		
				改訂日 DATE	改訂記事 REVISE	担当 CHARGE
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	Z80 series Package crating case	
日付 DATE	1979 8 . 22			コード CODE		
設計 DESIGN / 製図 DRAW / 写図 TRACE / 検図 CHECK / 承認 APPROVE		ザーフ株式会社 電子部品事業本部				

SHARP

1. Package specifications
   Refer to Fig. AA176-01.

2. Marking specifications

   2-1 Contents
   The following items must be marked on each product body.

   (1) Product name : LH-0080A Z80A-CPU

   (2) Company name : SHARP

   (3) Date code : (Example)

   9 H 2001 (This means Aug. 1979.)
   - 2001: Lot No.
   - H: A - L shows month.
   - 9: The last digit of year

   2-2 Position and direction
   Refer to Fig. AA176-01

   2-3 Marking color
   SILVER

3. Crating specifications

   3-1 Crating materials

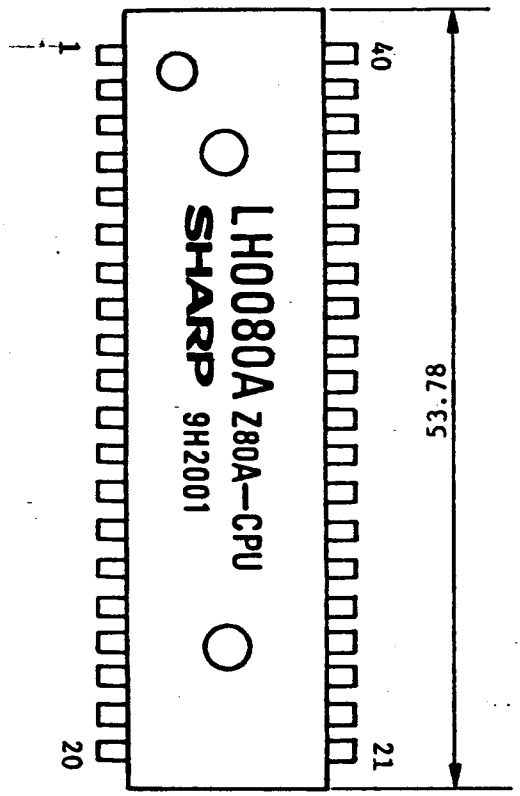
Material Name	Material Specifications	Purpose
Packing case	Plastic (Includes 10 pcs.)	Package
Cushion-1	Semiconducting moltplane	Package fixing
Cushion-2	General moltplant	Buffer
Cellophane tape		Package case lid fixing
Label	Paper	Product name, quantity indication
Crating case	Corrugated paper (Includes 40 package cases.)	Package case crating

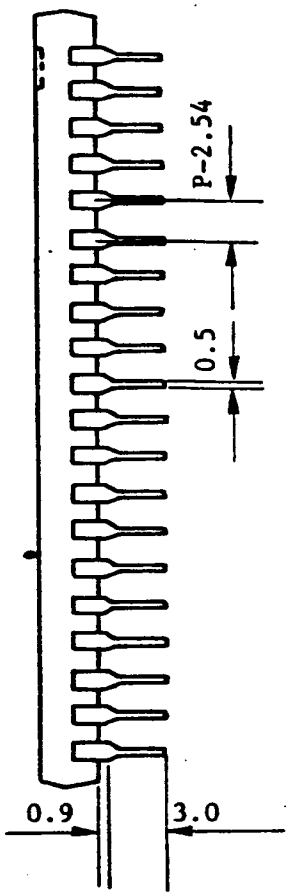
   3-2 Crating procedure

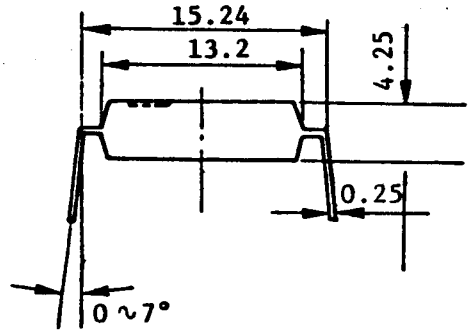
   (1) Place cushion-2 in case.
   (2) Insert package into cushion-1 and place into package case.
   (3) Put cushion-2, after completing above steps, into case.
   (4) Attach cover and secure with cellophane tape.
   (5) Mark quantity and manufacturing date on the side of the case.

   3-3 External view of crate
   Refer to Fig. BJ014-00.

SHARP

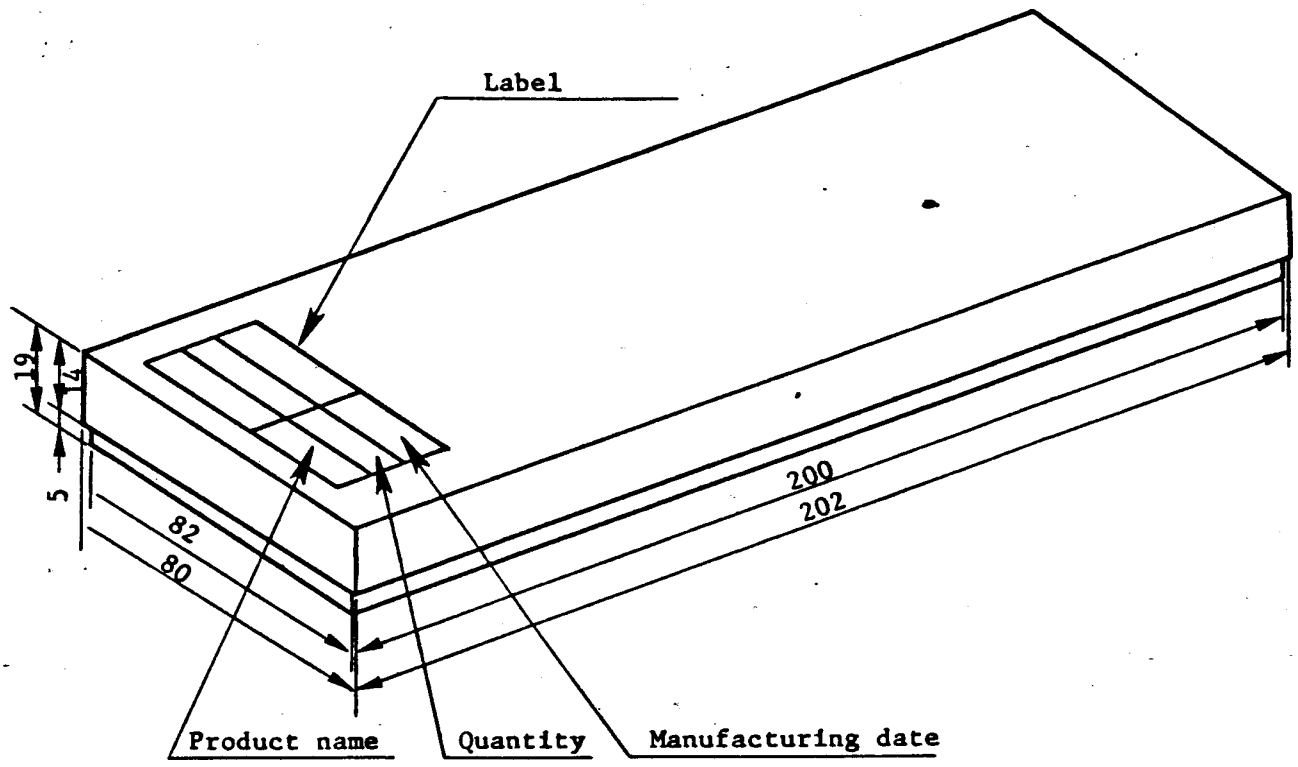






適用機種 APPLICABLE MODEL	LH-0080A Z80A-CPU	尺度 SCALE	2/1	単位 UNIT	1 = m/m	改訂日 DATE	改訂記事 REVISE / 担当 CHARGE
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	DPT40AP		
0.25t							
日付 DATE	1979. 8. 15			コード CODE			
設計 DESIGN / 製図 DRAW / 写図 TRACE / 検図 CHECK / 承認 APPROVE	シャープ株式会社 電子部品事業本部						

SHARP



° 10 pcs.

適用機種 APPLICABLE MODEL	LH-0080A Z80A-CPU	尺度 SCALE	単位 UNIT	△2 . .			
		/	1 = m/m	△1 . .			
				改訂日 DATE	改訂記事 REVISE		担当 CHARGE
板厚 THICKNESS	台数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	Z80 series Package crating case		
日付 DATE 1979 . 8 . 15				コード CODE			
設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	シャープ株式会社 電子部品事業本部		

34

SHARP

1. Package specifications
   Refer to Fig. AA177-01

2. Marking specifications

2-1 Contents
The following items must be marked on each product body.

(1) Product name : LH-0080AC

(2) Company name : SHARP

(3) Date code : (Example)

9 I 1001 (This means Sep. 1979.)

- 1001 — Lot No.
- I — A - L shows month.
- 9 — The last digit of year

2-2 Position and direction
Refer to Fig. AA177-01

2-3 Marking color
RED

3. Crating specifications

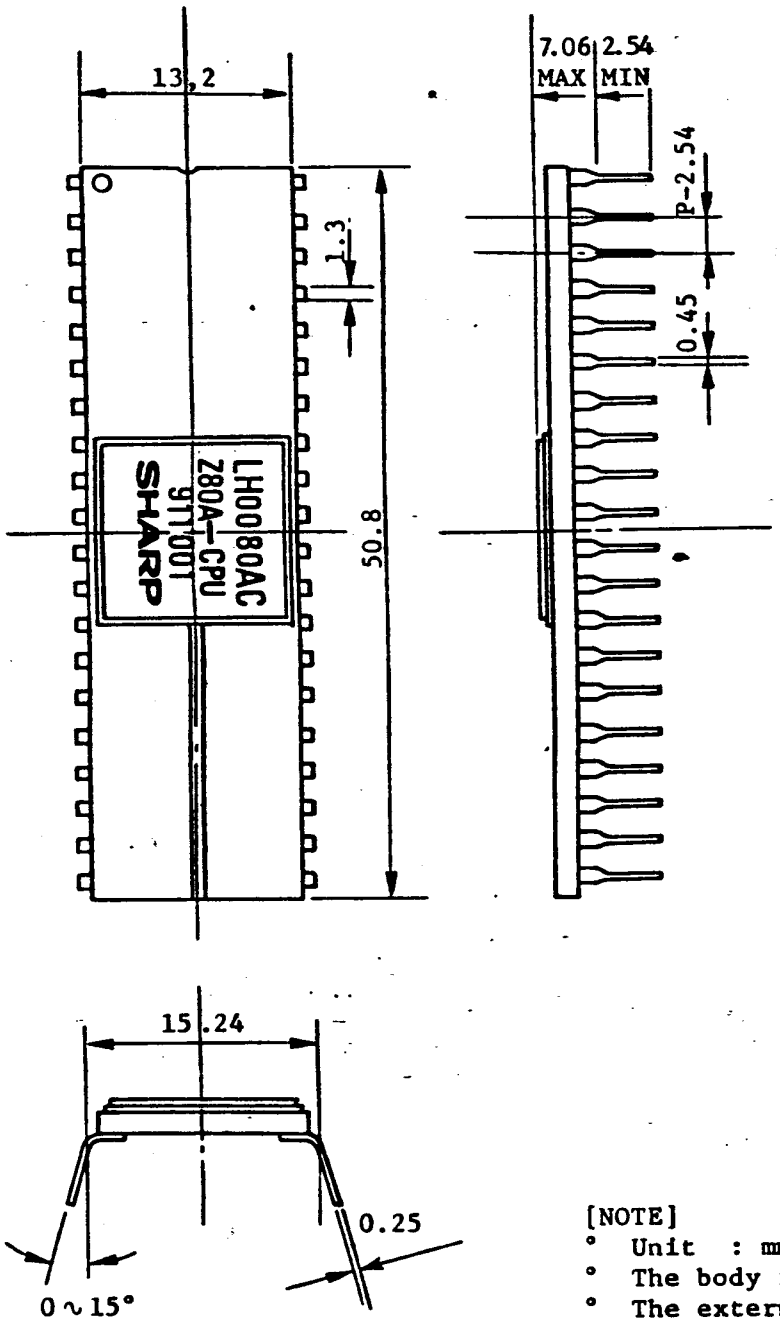
3-1 Crating materials

Material Name	Material Specifications	Purpose
Packing case	Plastic (Includes 10 pcs.)	Package
Cushion-1	Semiconducting moltplane	Package fixing
Cushion-2	General moltplane	Buffer
Cellophane tape		Package case lid fixing
Label	Paper	Product name, quantity indication
Crating case	Corrugated paper (Includes 40 package cases.)	Package case crating

3-2 Crating procedure

(1) Place cushion-2 in case.
(2) Insert package into cushion-1 and place into package case.
(3) Put cushion-2, after completing above steps, into case.
(4) Attach cover and secure with cellophane tape.
(5) Mark quantity and manufacturing date on the side of the case.

3-3 External view of crate
Refer to Fig. BJ014-00.



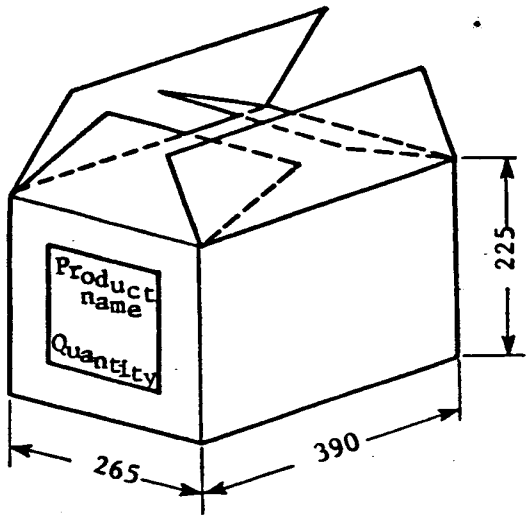
[NOTE]
- Unit : mm
- The body is ceramic finished.
- The external leads should be gilded.

適用機種 APPLICABLE MODEL	LH-0080AC	尺度 SCALE	2/1	単位 UNIT	1 = m/m
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	Ceramic	仕上 FINISH	
日付 DATE	1979. 9. 10				
設計 DESIGN / 製図 DRAW / 写図 TRACE / 検図 CHECK / 承認 APPROVE		シャープ株式会社 電子部品事業本部			

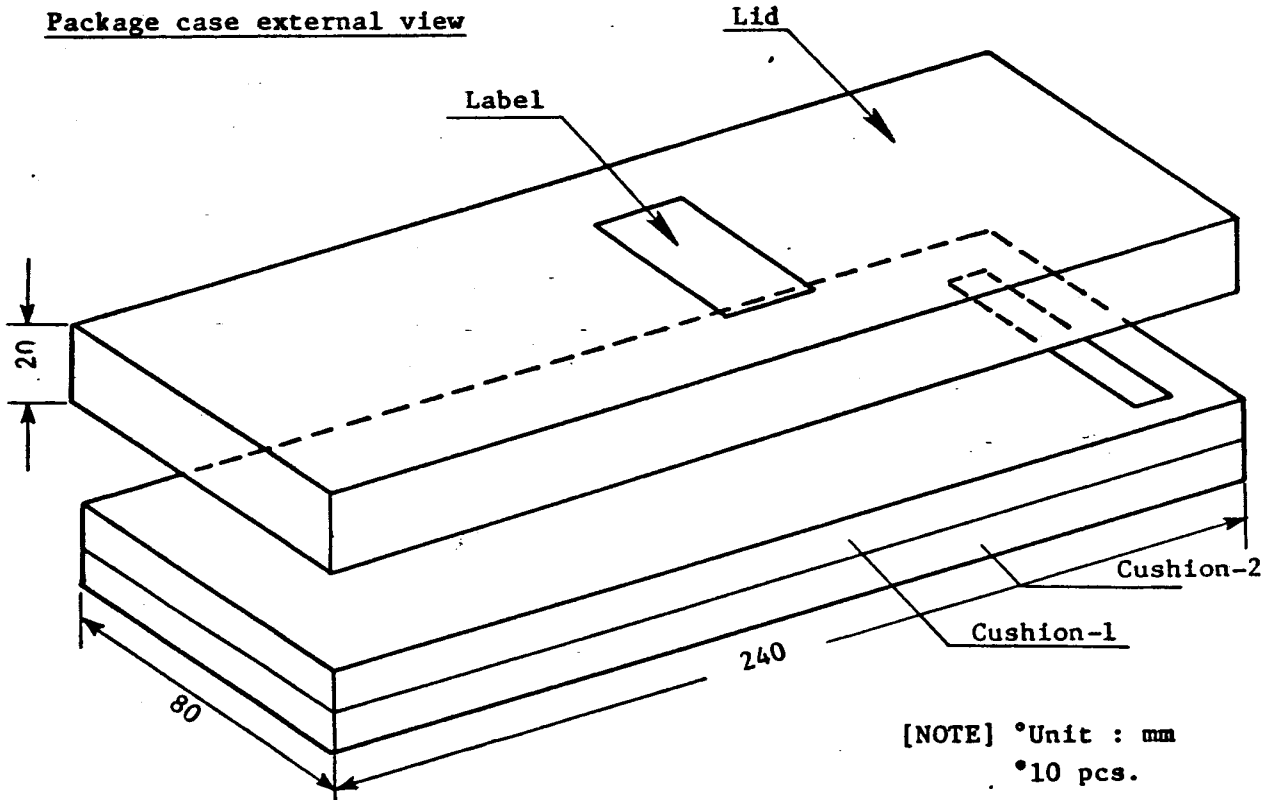
△			
△			
改訂日 DATE	改訂記事 REVISE	担当 CHARGE	
名称 NAME	DP40AK package		
コード CODE			

SHARP

Crating case



Package case external view



[NOTE] •Unit : mm
•10 pcs.

適用機種 APPLICABLE MODEL	LH-0080AC	尺度 SCALE	単位 UNIT	改訂日 DATE	改訂記事 REVISE / 担当 CHARGE
		/	1 = /		
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH	名称 NAME	Package crating case
日付 DATE 1979 . 9 . 10				コード CODE	
設計 DESIGN / 製図 DRAW / 写図 TRACE / 検図 CHECK / 承認 APPROVE		シャープ株式会社 電子部品事業本部			