MOTOROLA

68K and ColdFire®

Product Portfolio

Overview

3Q97

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http://www.mot.com/hpesd/docs_survey.html

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JAPAN, Atsugi	81(0462)23-0761
JAPAN, Kumagaya	81(0485)26-2600
JAPAN, Kyushu	81(092)771-4212
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PREFACE

Introduction

The *68K and ColdFire Product Portfolio Overview (3Q97)* describes current products in these 2 microprocessor families.

Additional 68K and ColdFire Documentation

See the specific section in the 68K and ColdFire Product Portfolio Overview for additional technical information support.

Trademarks

All trademarks mentioned in this document reside with their respective owners.

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Preface

Overview

Introduction   The *68K and ColdFire® Product Portfolio Overview* document provides a quarterly update to all 68K and ColdFire standard products produced by the Imaging and Storage Division.

Website Contents   The latest documentation updates for 68K and ColdFire parts are located at the following URLs:

http://www.motorola.com/isd
http://www.motorola.com/68000
http://www.motorola.com/68300
http://www.motorola.com/ColdFire

Documentation for all other Motorola microprocessors is located at:
http://www.motorola.com/microprocessors

Section 1

The M68000 Family

Overview

Introduction

The M68000 Family continues to be the industry standard in 32-bit embedded applications. The M68000 Family is currently in use in thousands of applications including handheld computing, telecommunications, office automation, network controllers, and consumer products.

M68000 Family Products

The M68000 Family offers a range of upward code-compatible performance unequalled in the industry—from 2 to 100 MIPS—and boasts the industry's largest array of third-party development tools. The following products comprise the M68000 Family:

• MC68EC000/MC68HC000/MC68SEC000
• MC68020/MC68EC020
• MC68030/MC68EC030
• MC68040/MC68EC040
• MC68040V
• MC68060/MC68EC060/MC68LC060

MC68EC000/SEC000

```
PREFETCH/          ┌──────────┐      ──► 24-BIT ADDRESS BUS
DECODE      ──►    │   BUS    │      ──► 16-BIT DATA BUS
            ──►    │CONTROLLER│
EXECUTION   ──►    │          │      ──► CONTROL
UNIT               └──────────┘
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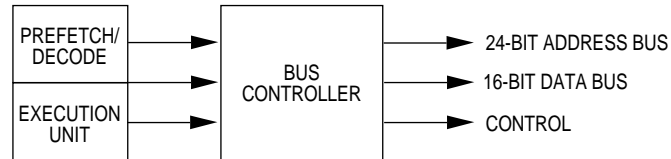
Features

- 24-bit address bus and 8- or 16-bit data bus
- Sixteen 32-bit registers
- Seven Interrupt levels
- 2.7 MIPS performance at 16.67 MHz

The 68SEC000 is a static version of the 68EC000.

Target Markets and Applications

The MC68EC000 represents the most inexpensive entry point to any 32-bit architecture. Upward migration to processors with a higher performance is possible because of the architecture's software compatibility. The CMOS process ensures low power consumption. Target applications are PABX low level, line cards, GSM fax, modems, industrial control, instrumentation, etc. The MC68EC000 is recommended for 8-bit applications that require higher performance and extended addressing range.

Related Microprocessors

For more information, see the MC68306 section later in this book.

Motorola's Competitive Advantage

The Z80 is inexpensive, but it has a limited performance upgrade potential. The 8086/8088 requires external support chips to avoid technical limitations.

Related Documentation

TITLE	ORDER NUMBER
MC68EC000 Product Brief	MC68EC000/D
M68000 User's Manual	M68000UM/AD Rev 8
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D
The High Performance Embedded Systems Source Catalog	BR729/D

MC68EC000, Continued

Support Tools
M68EC000IDP—An integrated development platform and hardware/software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP -40• TO +85• C	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68EC000	68-Lead FN	8-, 10-, 12-, 16-, and 20-MHz	—	—	0	18	1008	SPAKEC000FN*xx*
	64-Lead FU	8-, 10-, 12-, 16-, and 20-MHz	—	CFUxx	0	84	252	SPAKEC000FU*xx*
MC68SEC000	64-Lead FU	10-, 16-, 20 MHz	—	—	0	84	252	SPAKSEC000FUxx
	64-Lead PB	10-, 16-, 20 MHz	—	—	1	1	1	SPAKSEC000PBxx

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
G78K	0	85%	MOS10	0.65m	Introduction	—	In process	Die size 125 x 133
G47B	0	85%	MOS8	0.65m	Introduction	—	In process	
0G74K	0	75%	MOS10	0.8mm	Production	—	Yes	Die size 157.2 x 167.6 (PCN to G78K and G47B)
2F30A	2	78%	MOS8	0.71mm	Production	—	—	Changed poly gate sizing (PCN to G78K and G47B)
1F30A	1	78%	MOS8	0.71mm	Cancelled	—	—	Changed contact sizing
0F30A	0	78%	MOS8	0.71mm	Cancelled	—	—	Die shrink, die size 130 ¥ 143
0F86C	0	63%	Tohoku	1.2m	Production	—	—	Die size = 213.4 ¥ 237.4 (PCN to G78K/G47B)
1F90A	1	75%	MOS8	0.8m	Cancelled	—	—	Changed polymide reticle
0F90A	0	75%	MOS8	.8m	Cancelled	—	—	Die shrink
5C71T	2	70%	MOS8	1.0m	Cancelled	—	—	

Status Information
First Silicon: 3Q91
MC Qualification Date: 4Q91
Die Size: 213 ¥ 237 (F86C), 130 ¥ 143 (F30A),
       157 ¥ 168 (G74K), 125 x 133 (G78K and G47B)
Devices: Sites = 68,000; Active = 37,000
Process: HCMOS

MC68HC000

PREFETCH/ DECODE	BUS CONTROLLER	→ 24-BIT ADDRESS BUS
EXECUTION UNIT		→ 16-BIT DATA BUS
		→ CONTROL
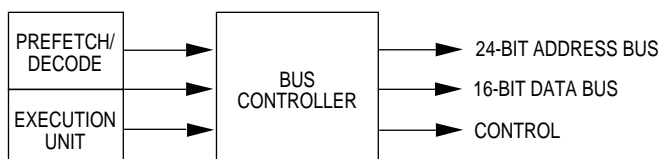
Features

- 24-bit address bus and 16-bit data bus
- Sixteen 32-bit registers
- Seven interrupt levels
- 2.7 MIPS performance at 16 MHz

Target Markets and Applications

The MC68HC000 processor is a low-power dissipation HCMOS version of the MC68000 16/32-bit microprocessor. The pin, timing, parameter, and code are all compatible with the standard (HMOS) MC68000. The MC68HC000 offers a lower power consumption than that of the HMOS MC68000. Worst-case power dissipations are 0.131 watts at 8 MHz, 0.158 watts at 10 MHz, 0.184 watts at 12.5 MHz, and 0.263 watts at 16.67 MHz.

The 64-pin P version is not sold in the United States.

Motorola's Competitive Advantage

The performance of the 8086/8088 is similar but the migration path to high-performance microprocessors is limited.

Competitors

Hitachi and Toshiba

Related Documentation

TITLE	ORDER NUMBER
MC68HC000 Product Brief (Rev 4)	MC68HC000/D
M68000 User's Manual (Rev 9)	M68000UM/AD
The High Performance Embedded Systems Source Catalog	BR729/D

MC68HC000, Continued

Support Tools	M68EC000IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68HC000	64-Lead P	8-, 10-, 12-, and 16-MHz	—	—	5	5	160	SPAKHC000P*xx*
	68-Lead R*, RC*	8-, 10-, 12-, and 16-MHz	—	CRC8,10,12,16	0	21	210	SPAKHC000RC*xx*
	68-Lead FN	8-, 10-, 12-, 16-, and 20-MHz	—	CFN8,10,12,16	0	18	1008	SPAKHC000FN*xx*
	68-Lead FC*	8-, 10-, 12-, and 16-MHz	—	CFC8,10,16	0	78	780	SPAKHC000FC*xx*
* Not recommended for new designs								

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
0G54B	0	75%	MOS11	0.8m	Cancelled	—	—	MOS11 version of E72N - 147.1 x 162.1
2E60R	2	63%	Tohoku	1.2m	PCN	—	In process	
1E60R	1	63%	Tohoku	1.2m	Cancelled	—	—	
0E60R	0	63%	Tohoku	1.2m	Cancelled	—	—	Die shrink, 212.6 ¥ 236.6
1E72N	1	75%	MOS8	0.8m	Cancelled	—	—	Die shrink 147.1 ¥ 163.2
4C71T	4	70%	MOS8	1.0m	Cancelled	—	—	Used on DIP and ext tempo versions
2B89N	2	56%	Tohoku	1.5m	Cancelled	—	—	Utilizes a differentially sized poly mask
1C71T	1	70%	MOS8	1.0m	Cancelled	—	—	Die size = 201 ¥ 220
3C44C	3	0	MOS8	—	Cancelled	—	—	1.2m process in MOS8
1B89N	1	56%	Tohoku	1.5m	Cancelled	—	—	Die size = 242 ¥ 271
1B66R	1	20%	MOS8	—	Cancelled	—	—	Shrink and fix latch up problem
2C44C	2	0	MOS8	—	Cancelled	—	—	Poly sizing change for speed improvement
1C44C	1	0	MOS8	—	Cancelled	—	—	Fix latch up problem
4B12C	3	0	MOS8	—	Cancelled	—	—	Poly sizing change for yield enhancement
3B12C	2	0	MOS8	—	—	—	—	Speed path fix for speed enhancement
1B12C	1	0	MOS8	—	Cancelled	—	—	Poly layer sized for speed enhancement
0B12C	0	0	MOS8	—	Cancelled	—	—	Original Motorola mask set
0G73K	0	75%	MOS10	0.8m	Cancelled	—	—	
1G73K	1	75%	MOS10	0.8m	Cancelled	—	—	MOS10 version of E72N - 149.4 x 165.5
2E72N	2	75%	MOS8	0.8m	PCN	—	In process	Metal 2 change to correct low frequency/high VDD problem (also applies to 1G73K)
G78K	0	85%	MOS10	0.65m	Introduction			
G47B	0	85%	MOS8	0.65m	Introduction			

Status Information   First Silicon: 3Q86
MC Qualification Date: 4Q86
Die Size: 147.1×163.2 (E72N), 213×237 (E60R),
149.4×165.5 (G73K), 125 x 133 (G78K and G47B)
Devices: Sites = 68,000; Active = 42,000
Process: HCMOS

MC68020
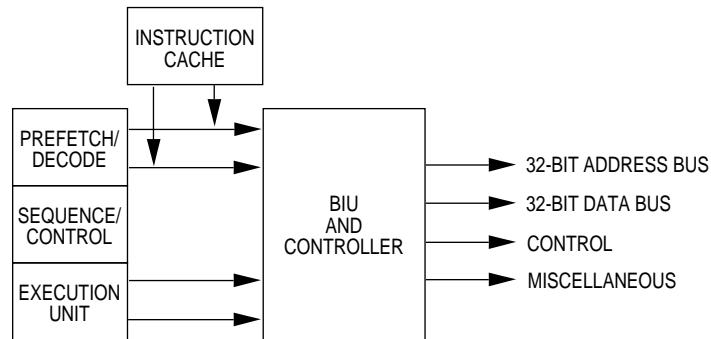
Features

- 32-bit address and data buses
- 256-byte instruction cache
- Coprocessor interface
- 9.8 MIPS/0.25 MFLOPS performance at 33 MHz

Target Markets and Applications

The MC68020 was the first microprocessor to use a full 32-bit internal and external architecture and the first to offer a vast increase in performance over 8- and 16-bit processors. The dynamic bus feature improves system flexibility, which allows use of 8- or 16-bit peripherals. The MC68EC020 should also be considered unless there is a clear need for the full 32-bit address bus.

Competitors

AMD and Intel

Motorola's Competitive Advantage

The Motorola MC68020 has some of the best support tools available.

Related Documentation

TITLE	ORDER NUMBER
MC68020 Product Brief (Rev 4)	MC68020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
The High Performance Embedded Systems Source Catalog	BR729/D

MC68020, Continued

Support Tools	M68EC020IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips	MC68882—Enhanced floating-point coprocessor

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68020	114-Lead RC	12-,16-, 20-, 25-, and 33-MHz	E	CRC16, 20, 25	1	1	14	MC68020RC*xx*E
	114-Lead RP	16-, 20-, and 25-MHz	E	CRP16	1	1	13	MC68020RP*xx*E
	132-Lead FE*	16-, 20-, 25-, and 33-MHz	E	—	0	36	180	SPAK020FE*xx*E
	132-Lead FC	16-, 20-, 25-, and 33-MHz	E	CFC16, 25	0	36	144	SPAK020FC*xx*E

*Not recommended for new designs

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
C10H	A	60%	Tohoku	1.2m	Production	—	—	Extended temperature only
B69R	B	60%	APRDL	1.2m	Cancelled	—	—	33 MHz - 60% shrink only
B49N	B	60%	APRDL	1.2m	Cancelled	—	—	33 MHz - 60% shrink only
B47K	B	50%	MOS8	1.5m	Cancelled	—	—	Same as B87E but for NIKON stepper
B87E	B	50%	MOS8	1.5m	Cancelled	—	—	Internal rev. # change
B40G	A	55%	MOS8	1.35m	Cancelled	—	—	
2A70N	—	40%	MOS8	1.7m	Cancelled	—	—	
1A43S	—	50%	MOS8	1.5m	Cancelled	—	—	Speed enhancement/cost reduction
2A45J	—	40%	MOS8	1.7m	Cancelled	—	—	Phased out - March, 1986
1A45J	L	40%	MOS8	1.7m	Cancelled	—	—	Phased out - March, 1986
A45J	K	40%	MOS8	1.7m	Cancelled	—	—	Virtual bug
A23G	J	40%	MOS8	1.7m	Cancelled	—	—	
A92E	—	40%	APRDL	1.7m	Cancelled	—	—	
E30G	A	67%	TSC	1.0m	Production	—	—	Optical identical to C54S

MC68020, Continued

Status Information   First Silicon: 2Q84
MC Qualification Date: 2Q85
Die Size: 252×244, 282×276
Devices: Sites = 190,000; Active = 103,000
Process: HCMOS

MC68EC020
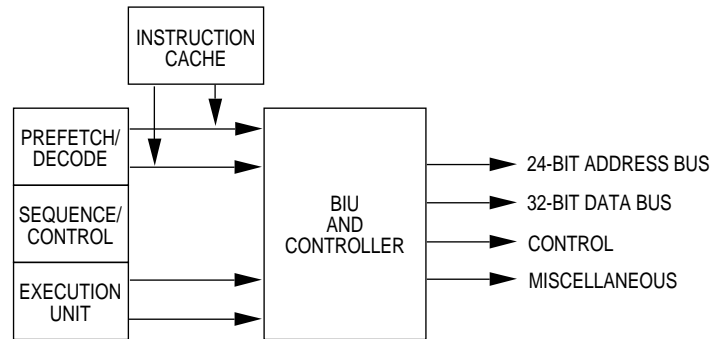
Features

- 24-bit address bus and 32-bit data bus
- 256-byte instruction cache
- Coprocessor interface
- 7.4 MIPS performance at 25 MHz

Target Markets and Applications

The strategy behind the MC68EC020 is to upgrade current MC68000 and MC68HC000 users to a higher performance product with a minimum increase in device or system cost. Key applications are PABX low level, GSM basestations, network controllers, printers, dumb terminals, robotics, VME boards, and instrumentation. The MC68EC020 has a 24-bit address bus and does not support extended temperature.

Competitors

AMD and Intel

Motorola's Competitive Advantage

Even though the Intel 960SA is similar in price to the MC68EC020, the extra logic you need to run the 960SA increases the overall system cost. In addition, the 960SB is an on-chip floating point unit, but it can be attacked by the high-performance MC68EC020/MC68882 combination with an aggressive price structure.

MC68EC020, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68EC020 Product Brief	MC68EC020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC020IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

MC68882—Floating-point coprocessor

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68EC020	100-Lead FG	16- and 25-MHz	—	CFG16	0	66	264	SPAKEC020FG*xx*
	100-Lead RP	16- and 25-MHz	—	CRP25	1	1	13	MC68EC020RP*xx*

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
E13G	A	67%	Tohoku	1.0m	Production	—	—	Optically identical to D76E
D76E	A	67%	MOS8	1.0m	Production	—	—	
C10H	A	60%	Tohoku	1.2m	Production	—	—	On RP package, has been replaced by E13G

Status Information

First Silicon: 2Q91
MC Qualification Date: 2Q91
Die Size: 239×247
Devices: Sites = 190,000; Active = 103,000
Process: HCMOS

MC68030

```
                          ┌──────────────┐
                          │ INSTRUCTION  │
                          │    CACHE     │
                          └──────┬───────┘
         ▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒▒   LINE HOLDING REGISTER
┌──────────────┐          │
│  PREFETCH/   │─────────▶│    ┌───┬──────────────┐
│   DECODE     │          │    │ P │              │────▶ 32-BIT ADDRESS BUS
├──────────────┤─────────▶│    │ M │    BIU       │────▶ 32-BIT DATA BUS
│  SEQUENCE/   │          │    │ M │    AND        │
│   CONTROL    │          │    │ U │  CONTROLLER  │────▶ CONTROL
├──────────────┤          │    │   │              │────▶ MISCELLANEOUS
│  EXECUTION   │─────────▶│    │   │              │
│    UNIT      │─────────▶│    └───┴──────────────┘
└──────────────┘
              │    │
              ▼    ▼
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         │   CACHE      │
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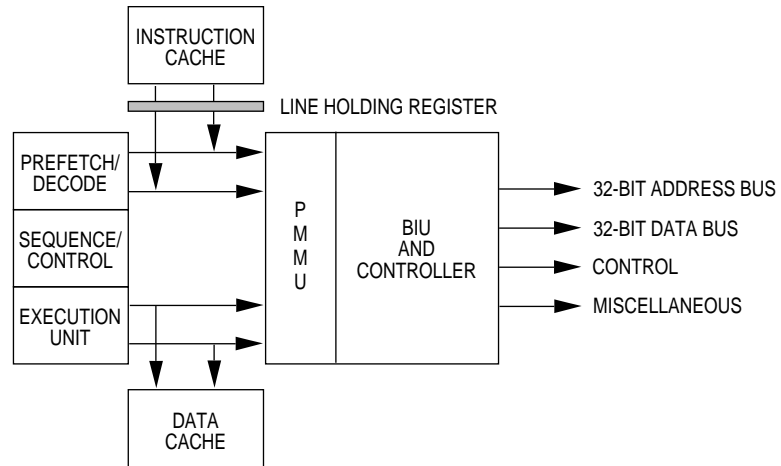
Features

- 32-bit address and data buses
- 256-byte on-chip instruction and data caches
- 17.9 MIPS performance at 50 MHz
- Burst memory interface
- Internal Harvard architecture
- Dynamic bus sizing
- On-chip memory management

Target Markets and

The MC68030 is well-suited for all applications requiring moderate performance and low cost (via dynamic bus sizing and burst memory interface). Memory management support protects users and tasks, allowing controlled execution of programs. Target markets are high-speed LAN controllers, I/O processors, laser printers, X-terminals, low-end PCs, and workstations.

Principle markets include low- to mid-range personal computers as well as embedded applications that require the protection features of a memory management unit.

Competitors

AMD and Intel

MC68030, Continued

<table>
<tr><td>Motorola's Competitive Advantage</td><td>The performance of the Intel 386 is comparable to the MC68EC030, except that it has an awkward register set and poor memory management. The performance and price range of the Intel 960KA is also comparable, but it contains multiplexed address and data buses, has no data cache, its performance is susceptible to wait states, and it has poor interrupt latency (Intel typically quotes 1 ms at 33 MHz).</td></tr>
</table>

Related Documentation

TITLE	ORDER NUMBER
MC68030 Product Brief	MC68030/D
MC68030 User's Manual	MC68030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC030IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- MC68882—Floating-point coprocessor
- MC88915/MC88916—Clock driver
- Crystals—Champion, Kyocera, and ACT
- FSRAMS—MCM6226

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68030	128-Lead RC	16-, 20-, 25, 33-, 40-, and 50-MHz	B, C	CRC16, 20, 25, 33	1	1	14	Call factory
	124-Lead RP	16-, 20-, 25-, and 33-MHz	B, C	CRP16, 20, 25, 33	1	1	14	
	132-Lead FE	16-, 20-, 25-, and 33-MHz	B, C	—	0	36	180	SPAK030FE*xx*C

MC68030, Continued

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
C74N	B	67%	MOS8	1.0m		No	Yes	
D62C	B	60%	Tohoku	1.2m	Cancelled	No	Yes	Tohoku die
D66C	B	67%	Tohoku	1.0m		No	Yes	Tohoku die
F91C	C	73%	Tohoku	0.8m	Production	No	Yes	Tohoku die
C48A	G	60/67%	APRDL	1.2m	Cancelled	—	—	33-MHz evaluation & bug fixer
C43C	B	60%	MOS8	1.2m	Cancelled	No	—	
B67R	I	60%	MOS8	1.2m	Cancelled	—	—	33-MHz MOS8 process certification-C48A
1B56P	D	55%	APRDL	1.35m	Cancelled	Yes	—	25 MHz, 1 errata
3B47B	C	55%	APRDL	1.35m	Cancelled	Yes	—	2 Errata
B47B	0	55%	APRDL	1.35m	Cancelled	—	—	Internal evaluation

Status Information

First Silicon: 2Q87
MC Qualification Date: 4Q87
Die Size: 256 x 238 (F91C) and G40W
Devices: Sites = 273,000; Active = 186,000
Process: HCMOS

MC68EC030
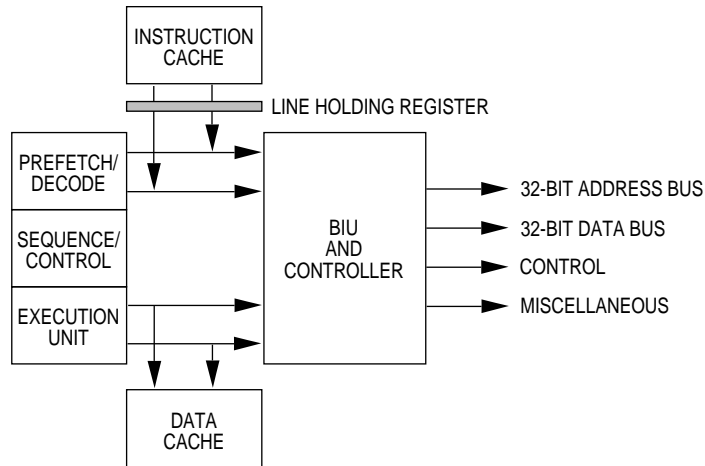
Features	• 32-bit address and data buses • 256-byte on-chip instruction and data caches • 14.3 MIPS performance at 40 MHz • Burst memory interface • Internal Harvard architecture • Bus sizing
Target Markets and Applications	The MC68EC030 is well-suited for all mid-range embedded control applications that require moderate performance, low price, and surface-mount capability. Target markets are high-speed LAN controllers, I/O processors, laser printers, and X-terminals.
Competitors	AMD and Intel
Motorola's Competitive Advantage	The performance and price range of the Intel 960KA is comparable, but it contains multiplexed address and data buses, has no data cache, its performance is susceptible to wait states, and it has poor interrupt latency (Intel typically quotes 1 ms at 33 MHz). Likewise, the performance level of the AMD29000 lies somewhere between that of the MC68EC030 and MC68EC040, but its performance is lower with DRAMs in burst mode. It is also susceptible to wait states and contains large register sets that are not well-suited to multitasking.

MC68EC030, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68EC030 Product Brief	MC68EC030/D
MC68EC030 User's Manual	MC68EC030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC030IDP—An integrated development platform and hardware/software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- MC68882—Floating-point coprocessor
- MC88915/MC88916—Clock driver
- FSRAMS—MCM6706BJ and MCM6246AWT
- Crystals—Champion, Kyocera, and ACT

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68EC030	124-Lead RP	25- and 40-MHz	C	CRP25	1	1	14	
	132-Lead FE	25- and 40-MHz	C	—	0	36	180	SPAKEC030FE*xx*C
	144-Lead PV	25-MHz	C	—	—	60	240	SPAKEC030PVxxC

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
C74N	B	67%	MOS8	1.0m		No	Yes	
D66C	B	67%	Tohoku	1.0m	Cancelled	No	Yes	Tohoku die
D62C	B	60%	Tohoku	1.2m	Cancelled	No	Yes	Tohoku die
F91C	C	73%	Tohoku	0.8m	Production	No	Yes	Tohoku die

MC68EC030, Continued

Status Information   First Silicon: 1Q91
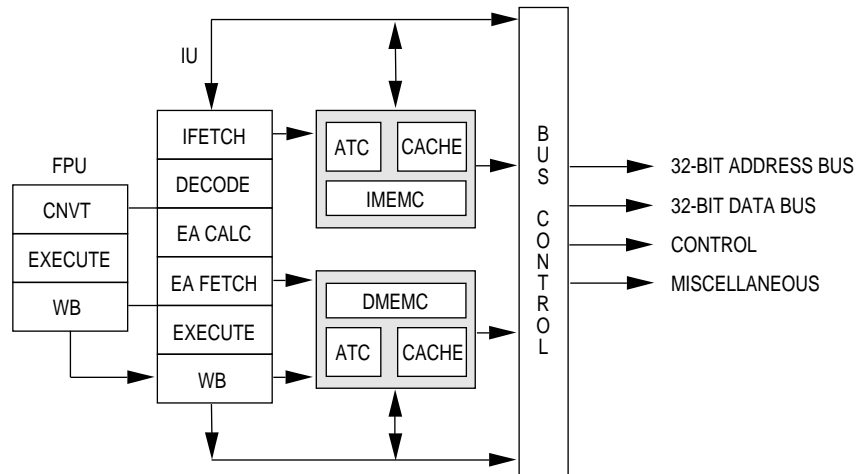MC Qualification Date: 1Q91
Die Size: 256×238 (F91C) and G40W
Devices: Sites = 251,000; Active = 183,000
Process: HCMOS

MC68040

Features

- 32-bit address and data buses
- 4-Kbyte on-chip instruction and data caches
- On-chip floating point support
- 43.8 MIPS performance at 40 MHz
- 5.3 MFLOPS performance at 40 MHz
- Burst memory interface
- On-chip memory management

Target Markets and Applications

The MC68040 is well-suited for all applications that require high-integer and floating-point performance and compatibility with the 68K architecture. Target markets include mid-performance embedded applications.

Competitors

AMD, IBM, IDT, Intel, and MIPs

Motorola's Competitive Advantage

The IDT 3051/52 has a competitive pricing structure, high performance, and surface mount capability, but unfortunately the multiplexed bus requires external components and the RISC machine is intolerant of wait states. Only a limited range of development tools is available compared to those for the 68K.

MC68040, Continued

Motorola's Competitive Advantage (continued)

The AMD 29030/35 has a competitive pricing structure and a 4K/8K instruction cache, but there is no data cache. In addition, bus usage is high and there is no support for multiprocessor systems.

Related Documentation

TITLE	ORDER NUMBER
MC68040 Product Brief	MC68040/D
M68040 User's Manual (Rev 1)	M68040UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC040IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- MC68150—Dynamic bus sizer
- MC88915/MC88916—Clock driver
- Crystals—Champion, Kyocera, and ACT
- FSRAMS—MCM62940 and MCM69P818ZP burst-mode SRAMs

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68040	179-Lead RC	25-, 33-, 40-MHz	—	—	1	1	10	
	184-Lead FE	25-, 33-, 40-MHz	—	—	0	24	96	SPAK040FExx

MC68040, Continued

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
2E42K	—	80%	MOS11	0.65m	Production	No	Yes	See addendum to user's manual on website
2E31F	M	80%	MOS11	0.65m	Cancelled	Yes	Yes	
OE31F	M	80%	MOS11	0.65m	Cancelled	Yes	Yes	
7D98D	E	75%	MOS8	0.8m	Cancelled	Yes	—	
D43B	B	75%	MOS8	0.8m	Cancelled	Yes	—	
4D50D	A	75%	MOS8	0.8m	Cancelled	Yes	—	
5D98D	E	75%	MOS8	0.8m	Cancelled	Yes	Yes	100 C test temperature only at this time
9D50D	B	75%	MOS8	0.8m	Cancelled	Yes	—	

Status Information

MC Qualification Date: 2Q95
Die Size: 473×500
Devices: Sites = 1,170,000; Active = 844,000
Process: HCMOS

MC68040V
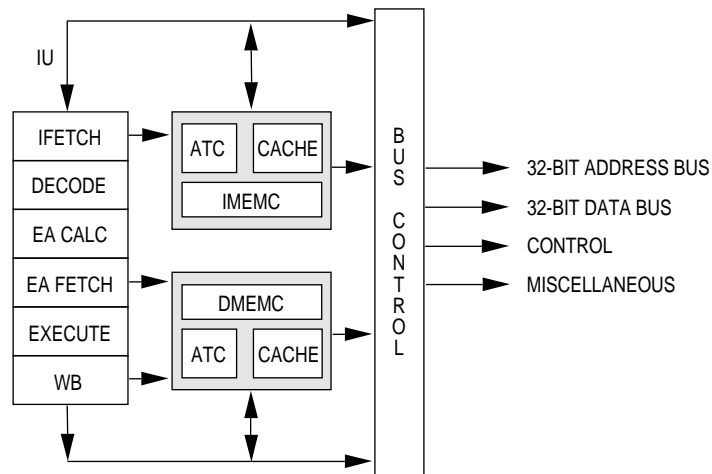
Features	• Low voltage (3.3 V) and low power (1.5 W at 33 MHz) version of the MC68LC040
	• Low-power mode for full power-down capability
	• Full static design
	• Dual input voltage compatibility (3.3 and 5 V TTL)
	• Identical code to the MC68LC040 plus LPSTOP command for power-down
	• Nonmultiplexed 32-bit address and data buses
	• 4-Kbyte on-chip instruction and data caches
	• 37 MIPS performance at 33 MHz
	• Burst memory interface
	• On-chip memory management
	• Upward pin compatibility with the MC68040 and MC68EC/LC040

Target Markets and Applications

The principle targets for the XC68040V are all high-performance, power-sensitive, general computing, and embedded processing applications.

Competitors

AMD, Hitachi, IBM, IDT, Intel, LSI, MIPs, and NEC

Motorola's Competitive Advantage

The Intel 960CA/F is marketed as a RISC high-end solution, but it consumes more power. The low-performance RISC machine is intolerant of wait states and requires expensive high-speed SRAM.

MC68040V, Continued

Motorola's Competitive Advantage (continued)

The IDT 3051/3052 and 3081/3082 all have a competitive pricing structure, high performance, and surface mount capability, but the multiplexed bus always requires external components. In addition, the RISC machine is intolerant of wait states, requires expensive high-speed SRAM, and consumes a lot of power.

The AMD 29030/35 has a competitive pricing structure and a 4K/8K instruction cache. Unfortunately, it has no data cache, bus usage is high, and there is no support for multiprocessor systems. Also, the RISC machine is intolerant of wait states, requires expensive high-speed SRAM, and consumes a lot of power.

Related Documentation

TITLE	ORDER NUMBER
MC68040 VT Product Brief	MC68040V/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
3.3 Volt Logic and Interface Circuits	BR1407/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC040IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

• MC68150—Dynamic bus sizer
• MC88915/MC88916/MC8892—Clock driver
• Crystals—Champion, Kyocera, and ACT
• National NM27C6841 burst EPROM
• FSRAMS—MCM62940 and MCM69P818ZP burst-mode SRAMs

MC68040V, Continued

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68040V	179-Lead RC	25-, 33-, 40-MHz		Max operation $T_J = 110° C$ Min operation $T_A = 0° C$	1	1	10	
	184-Lead FE	25- and 33-MHz			0	24	96	SPAK040FE*xx*V

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
3F54F	J	85%	MOS11	0.5 TLM	Sampling	Yes	No	
2F54F	I	85%	MOS11	0.5 TLM	Cancelled	Yes	No	
1F54F	H	85%	MOS11	0.5 TLM	Cancelled	Yes	No	
0F54F	G	85%	MOS11	0.5 TLM	Cancelled	Yes	No	
6D33T	F	85%	MOS11	0.5 TLM	Cancelled	Yes	No	

Status Information
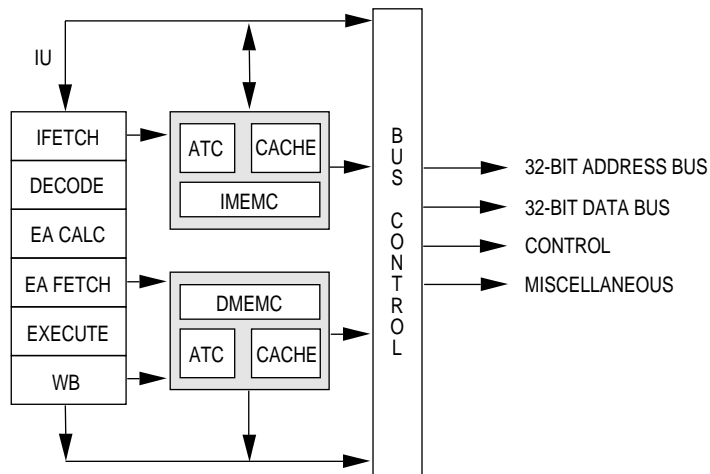
MC Qualification Date: 3Q96
Die Size: 357.8 x 321.7
Devices: Sites = 1,170,000; Active = 844,000
Process: 0.5μ TLM

MC68EC/LC040

Features

- 32-bit address and data buses
- 4-Kbyte on-chip instruction and data caches
- 44 MIPS performance at 40 MHz
- Burst memory interface
- On-chip memory management (LC040 only)

Target Markets and Applications

The MC68EC/LC040 is well suited for all high-end embedded control applications that require high performance, low cost, and memory management.

Competitors

AMD, IBM, IDT, Intel, and MIPs

Motorola's Competitive Advantage

The Intel 486SX is a low-cost 486, but it is not accepted outside the DOS-compatible market. The IDT 3051/3052 has a competitive pricing structure, high performance, and surface mount capability, but the multiplexed bus requires external components to run. Also, the RISC machine is intolerant of wait states and there is a limited range of development tools compared to those available for the 68K.

The AMD 29030/29035 has a competitive pricing structure and a 4K/8K instruction cache, but there is no data cache, bus usage is high, and no support for multiprocessor systems.

MC68EC/LC040, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68LC040 Product Brief	MC68LC040/D
MC68EC040 Product Brief	MC68EC040/D
M68040 User's Manual (Rev 1)	M68040UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC040IDP—An integrated development platform and hardware/ software evaluation module. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- 68150—Dynamic bus sizer
- MC68360—Integrated communication controller
- MC88915/MC88916—Clock driver
- Crystals—Champion, Kyocera, and ACT
- FSRAMS—MCM62940 and MCM69P818ZP burst-mode SRAMs

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68EC040	179-Lead RC	20-, 25-, 33-, and 40-MHz	—	—	1	1	10	SPAKEC040FE*xx*
MC68LC040	184-Lead FE	20-, 25-, 33-, and 40-MHz	—	—	0	24	96	SPAKLC040FE*xx*

Product History

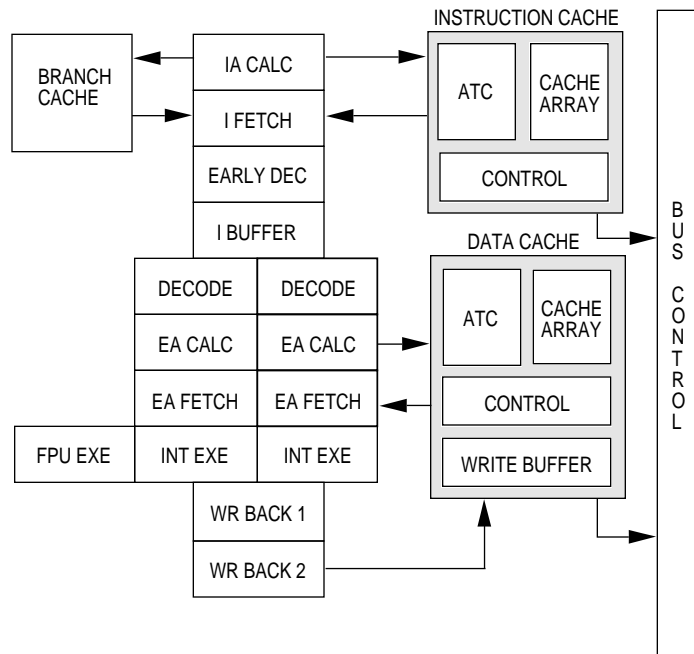| MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
2E71M	—	80%	MOS11	0.65m	Production	No	Yes	See Addendum User's Manual on web
2E23G	B	80%	MOS11	0.65m	Cancelled	Yes	—	XC orders supplied in 2E23G
D39H	A	75%	MOS8	0.8m	Cancelled	Yes	No	

MC68EC/LC040, Continued

Status Information

MC Qualification Date: 4Q95
Die Size: 461.4×431.6
Devices: Sites = 777,092
Process: HCMOS

XC68060

INSTRUCTION CACHE

| BRANCH CACHE | IA CALC | | ATC | CACHE ARRAY |
| I FETCH |

EARLY DEC

I BUFFER

DATA CACHE

DECODE	DECODE		ATC	CACHE ARRAY
EA CALC	EA CALC
EA FETCH	EA FETCH		CONTROL
FPU EXE	INT EXE	INT EXE		WRITE BUFFER

WR BACK 1

WR BACK 2

CONTROL

BUS CONTROL

Features

- 112.5 MIPS at 66 MHz
- Dual-issue execution pipeline
- 32-bit address and data buses
- 8-Kbyte on-chip instruction and data caches
- 256-entry branch cache
- On-chip floating-point support
- On-chip memory management
- Burst memory interface
- Low-power design
- 3.3 V operation

Target Markets and Applications

The XC68060 is well-suited for all applications that require high-integer and floating-point performance and compatibility with the 68K architecture.

Competitors

AMD, IBM, IDT, Intel, and MIPs

XC68060, Continued

Motorola's Competitive Advantage

The Intel Pentium dominates the PC-DOS market and requires a 64-bit bus to run, whereas the XC68060 has superior integer performance combined with a low-cost memory system.

Related Documentation

TITLE	ORDER NUMBER
MC68060 Product Brief	MC68060/D
M68060 User's Manual (Rev 1)	M68060UM/AD
M68000 Family Brochure (Rev 1)	BR1115/D
M68060 Family Brochure	BR1153/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC060IDP—An integrated development platform and hardware/software evaluation module that will be available soon. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- MC68150—Dynamic bus sizer
- MC88926—Clock driver
- Crystals—Champion, Kyocera, and ACT
- FSRAMS—MCM62940 and MCM69P818ZP burst-mode SRAMs

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XC68060	206-Lead RC	50 MHz	—	—	1	1	10	

Product History

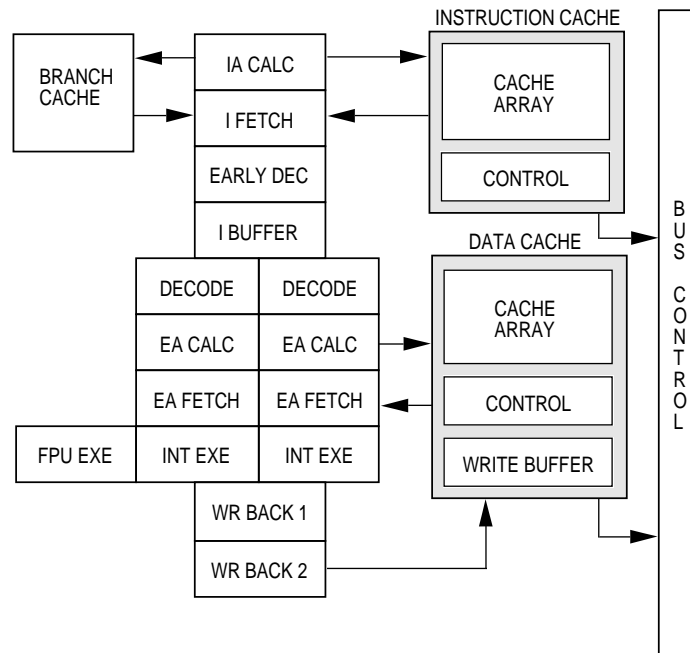| MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
1F43G	C	85%	MOS11	0.5m	Production	Yes	—	
0F43G	B	85%	MOS11	0.5m	Cancelled	Yes	—	
D11W	A	85%	APRDL	0.5m	Cancelled	Yes	—	

XC68060, Continued

Status Information   First Silicon: 4Q93
XC Qualification Date: 1Q95
Die Size: 582×579
Devices: Active = 2,530,000
Process: HCMOS

XC68EC060

Features	• 100 MIPS at 66 MHz
	• Dual-issue execution pipeline
	• 32-bit address and data buses
	• 8-Kbyte on-chip instruction and data caches
	• 256-entry branch cache
	• Burst memory interface
	• Low-power design
	• 3.3 V operation

Target Markets and Applications

The XC68EC060 is well-suited for high-end embedded control applications that require high performance at a low price.

Competitors

AMD, IBM, IDT, Intel, and MIPs

Motorola's Competitive Advantage

The Intel Pentium dominates the PC-DOS market and requires a 64-bit bus to run, whereas the XC68EC060 has a superior integer performance combined with a low-cost memory system.

XC68EC060, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68060 Product Brief	MC68060/D
M68060 User's Manual (Rev 1)	M68060UM/AD
M68060 Family Brochure	BR1153/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68060IDP—An integrated development platform and hardware/ software evaluation module available. Refer to *The High Performance Embedded Systems Source Catalog* for information on third-party support tools.

Support Chips

- MC68150—Dynamic bus size
- MC88926—Clock driver
- Crystals—Champion, Kyocera, and ACT
- FSRAMS—MCM62940 and MCM69P818ZP burst-mode SRAMs

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XC68EC060	206-Lead RC	50- and 66-MHz	E	—	0	1	10	

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
1F43G	C	85%	MOS11	0.5m	Production	Yes	—	
0F43G	B	85%	MOS11	0.5m	Cancelled	Yes	—	
D11W	A	85%	APRDL	0.5m	Cancelled	Yes	—	EC060s temp. sourced from full ' 060 mask

Status Information

First Silicon: 4Q93
XC Qualification Date: 1Q95
Die Size: 103.2 mm^2
Devices: Active = 2,130,000
Process:.42μ HCMOS

XC68LC060
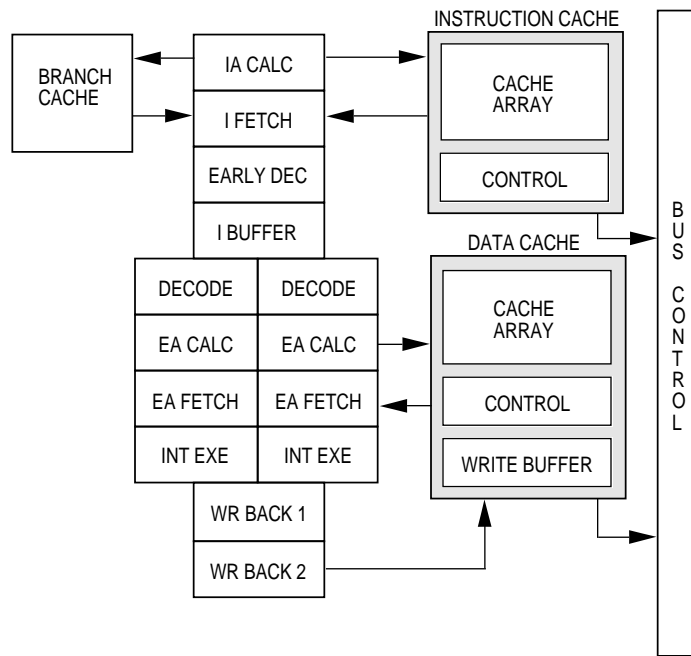
Features

- 100 MIPS at 66 MHz
- Dual-issue execution pipeline
- 32-bit address and data buses
- 8-Kbyte on-chip instruction and data caches
- 256-entry branch cache
- Burst memory interface
- On-chip memory management
- Low-power design
- 3.3 V operation

Target Markets and Applications

The 68LC060 is well-suited for high-end embedded control applications that require high performance, low cost, and memory management.

Competitors

AMD, IBM, IDT, Intel, and MIPs

Motorola's Competitive Advantage

The Intel Pentium dominates the PC-DOS market and requires a 64-bit bus to run, whereas the XC68LC060 has a superior integer performance combined with a low-cost memory system.

XC68LC060, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68060 Product Brief	MC68060/D
M68060 User's Manual (Rev 1)	M68060UM/AD
M68060 Family Brochure	BR1153/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68EC060IDP–An integrated development platform and hardware/ software evaluation module that will be available soon. Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

Support Chips

- MC68150–Dynamic bus sizer
- MC88926–Clock driver
- Crystals–Champion, Kyocera, and ACT
- FSRAMS–MCM62940 and MCM69P818ZP burst-mode SRAMs

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XC68LC060	206-Lead RC	50-MHz	—	—	0	1	10	

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
1F43G	C	85%	MOS11	0.5m	Production	Yes	—	
0F43G	B	85%	MOS11	0.5m	Cancelled	Yes	—	
D11W	A	85%	APRDL	0.5m	Cancelled	Yes	—	LC060s temp. sourced from full 060 mask

Status Information

First Silicon: 4Q93
XC Qualification Date: 1Q95
Die Size: 103.2 mm^2
Devices: Active = 2,130,000
Process:.42m HCMOS

68K and ColdFire Product Portfolio Overview MOTOROLA

Section 2

The M68100 Family

Overview

Introduction   The wireless messaging revolution continues with Motorola defining the next *de facto* paging protocol standard called FLEX. FLEX is an Open Standard protocol that will allow new markets and high-performance applications to be developed for a global community. One clear advantage of the FLEX protocol is that it allows increased system capacity through multispeed communication.

FLEX Family   The Motorola FLEX IC MC68175 is the first member of this FLEX family. The FLEX IC greatly simplifies the design of a paging device. The system designer will no longer have to spend valuable time writing and rewriting the protocol.

Two related paging protocols, ReFLEX, which allows two-way messaging capabilities, and InFLEXion, a high-speed voice and data protocol, could join the FLEX IC Family in the very near future.

MC68175 Flex™ IC
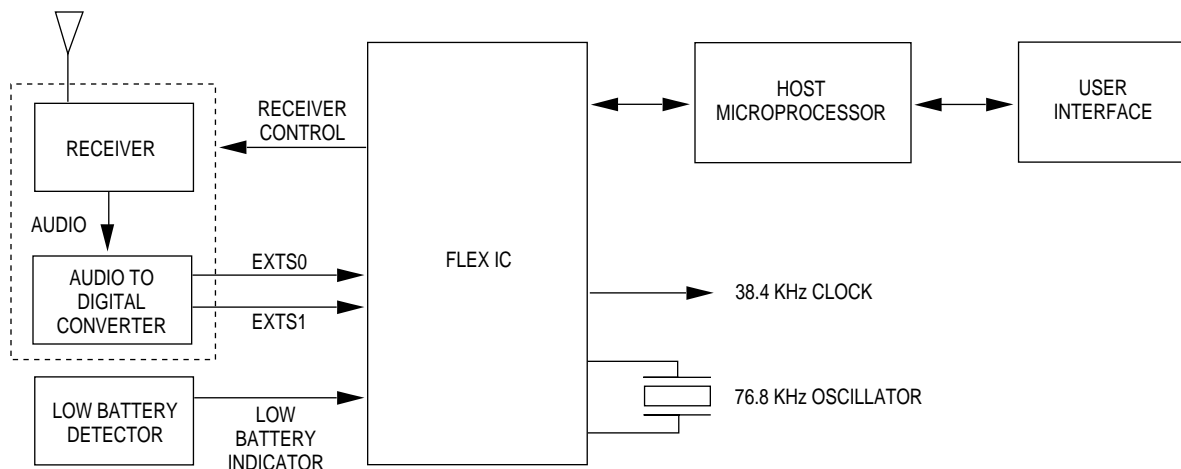
Features

- FLEX™ paging protocol signal processor
- 16 programmable user address words
- 16 fixed temporary addresses
- 1600, 3200, and 6400 bits per second decoding
- Any-phase decoding
- Uses standard Serial Peripheral Interface (SPI) in slave mode
- Allows low current STOP mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX roaming, fragmentation, and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- 24 pins

Target Markets and Applications

Initially, the FLEX IC will be used primarily in the paging market to support the FLEX multispeed, high-performance paging protocol adopted by leading service providers worldwide as a de facto standard. The FLEX IC simplifies implementation of a Flex paging device by interfacing with any of several off-the-shelf paging receivers and any of several off-the-shelf host microcontrollers/microprocessors. Future FLEX IC applications will include a wide range of possibilities, any of which involve consumers' interaction with electronic devices, such as personal digital assistants, laptop computers, home electronics, or automobiles. The FLEX IC will allow users to communicate with these devices and many others from remote locations.

MC68175 Flex™ IC, Continued

Competitors

The Texas Instruments TLV5591 is a FLEX signal processor (pin-for-pin compatible, authorized device).

Motorola's Competitive Advantage

FLEX protocol gives service providers the increased capacity, added reliability, and enhanced pager battery performance they need today. It also provides an upward migration path to the service provider that is completely transparent to the end user.

FLEX Protocol vs. POCSAG

- FLEX protocol can give the service provider a potential increase of more than 10 times over a POCSAG 512 bps system
- FLEX protocol can operate at three different speeds, allowing a system to initially run more slowly, and then increase speed as system demands increase, while still using the same pager units
- FLEX protocol provides accurate message delivery by offering protection from fading conditions, such as bridges or overpasses It provides 12 times the fading protection of PCOSAG 1200 and 24 times the fading protection of POCSAG 2400

FLEX protocol is a synchronous time slot scheme designed to increase the battery life of pagers. Instead of sending out messages at random, all paging data intended for a particular pager is scheduled into a predefined time slot. This allows a FLEX pager to selectively decode one or more frames over each four-minute FLEX cycle, so that the pager does not waste its battery life decoding data intended for other pagers.

Related Documentation

TITLE	ORDER NUMBER
MC68175 Product Brief	MC68175/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

Software Developers Kit (SDK)–ANSI C Interpreter that generates code for the host MCU/MPU communicating to the FLEX IC via the SPI interface.

MC68175 Flex™ IC, Continued

Support Tools
(Continued)

FLEXstack–Software that runs on Host MCU/MPU and handles the interpretation of raw code words that pass between the FLEX IC and host.

Support Chips

Texas Instruments DART–Converts an audio signal from an off-the-shelf receiver IC to a two-bit digital output for processing by the FLEX IC.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
---	---	---	---	---	SOQ	MPQ	POQ	
XC68175	32-Lead EA	76.4-KHz	—	0 to 70∞ C	—	—	—	

Status Information

First Silicon: 2Q96
XC Qualification Date: 3Q96
Die Size: TBD
Devices: 80K
Process:.65m TLM

Section 3

The ColdFire® Family

Overview

Introduction   ColdFire® represents a revolutionary microprocessor architecture that has
been optimized for embedded processing applications. It brings new
levels of price and performance to cost-sensitive, high-volume markets.
Based on the concept of variable-length RISC technology, ColdFire
combines the architectural simplicity of conventional 32-bit fixed-length
RISC with a memory-saving, variable-length instruction set.

By employing a variable-length instruction set architecture, ColdFire
RISC processors are tuned to offer embedded processor designers
significant system-level advantages over conventional fixed-length RISC
architectures. Binary code for ColdFire processors is denser and therefore
takes up less program memory than conventional 32-bit fixed-length
machines. This improved code density results in systems that require less
memory for a given application and also allows the use of slower and less
costly memory to achieve a given performance level.

The Advantage of   Not only is the ColdFire architecture optimized for performance, its small
ColdFire Architecture   die size and competitive process technology yield low unit cost for the
customer. ColdFire's creation comes from the 68K architecture. Thus
each ColdFire design includes 17 years of 68K technical support and
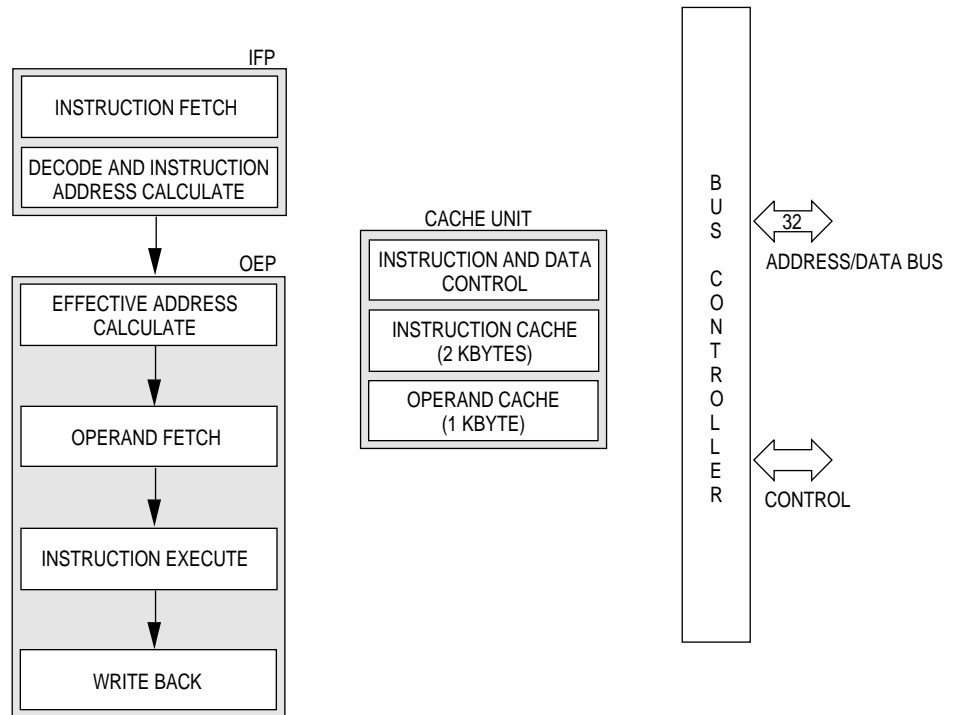evaluation tools for customer support.

The ColdFire Product   The ColdFire Family consists of the following devices:
Family

• XCF5102
• XCF5202/03
• XCF5204
• XCF5206

XCF5102

Diagram labels:

IFP
- INSTRUCTION FETCH
- DECODE AND INSTRUCTION ADDRESS CALCULATE

OEP
- EFFECTIVE ADDRESS CALCULATE
- OPERAND FETCH
- INSTRUCTION EXECUTE
- WRITE BACK

CACHE UNIT
- INSTRUCTION AND DATA CONTROL
- INSTRUCTION CACHE (2 KBYTES)
- OPERAND CACHE (1 KBYTE)

BUS CONTROLLER
- 32 ADDRESS/DATA BUS
- CONTROL

Features

- High integer performance
  - One instruction per clock peak performance
- Full static design allows operation down to DC to minimize power consumption
- On-chip caches
  - 2 Kbyte instruction cache
  - 1 Kbyte data cache
- Four separate access control registers
- Simple instruction set architecture
  - Sixteen user-visible 32-bit wide registers
  - User-mode compatible with M68000 instruction set
  - Supervisor/user modes for system protection
  - Vector base register to relocate exception vector table
  - Optimized for high-level language constructs
- Low interrupt latency
- Fully code-compatible with the M68EC030

XCF5102, Continued

Features (Continued) • Multiplexed 32-bit address and data buses to minimize board space and interconnections
• 3.3 V operation
• 5 V TTL-compatible and 5 V CMOS-tolerant
• Three-state pin
• Snoop capability
• JTAG IEEE 1149.1
• Single bus clock input
• Fast-locking PLL

Target Markets and Applications The XCF5102 is fully compatible with ColdFire code. As the first chip in the ColdFire Family, it has been specially designed to allow it to execute the M68000 code that exists today. These extensions to the ColdFire instruction set allow Motorola customers to use the XCF5102 as a bridge to future ColdFire processors for applications requiring the advantages of a variable-length RISC architecture. Compatibility with existing development tools such as compilers, debuggers, real-time operating systems, and adapted hardware tools offers XCF5102 developers access to a broad range of mature support tools. Such a compatibility with existing development tools enables accelerated product development cycles, lowers development costs, and decreases critical time-to-market advantages for Motorola customers.

Competitors ARM and Hitachi

Motorola's Competitive Advantage The XCF5102 runs existing 68K code.

Related Documentation

TITLE	ORDER NUMBER
MCF5102 User's Manual	MCF5102UM/AD
M68000 Family Programmer's Reference Manual	M68000PM/AD
The High Performance Embedded System Source Catalog	BR729/D

Support Tools M5102EVM: Refer to *The High Performance Embedded Systems Source Catalog* for third-party support tools.

XCF5102, Continued

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XCF5102	144-Lead PV	16-, 20-, 25-, and 33-MHz	A	—	0	60	240	SPAK5102PV*xx*A

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS

MCF5202

```
┌─────────────┐  ┌─────────────────────────┐ ┌───┐
│             │  │ ┌─────────────────────┐ │ │ B │
│             │  │ │ INSTRUCTION ADDRESS │ │ │ U │
│             │  │ │     GENERATION      │ │ │ S │
│             │  │ └─────────────────────┘ │ │   │
│             │  │ ┌─────────────────────┐ │ │ C │
│             │  │ │  INSTRUCTION FETCH  │ │ │ O │
│  2 K-BYTE   │  │ └─────────────────────┘ │ │ N │
│  UNIFIED    │  │ ┌─────────────────────┐ │ │ T │
│  CACHE      │  │ │ INSTRUCTION BUFFER  │ │ │ R │
│             │  │ └─────────────────────┘ │ │ O │
│             │  │ ┌─────────────────────┐ │ │ L │
│             │  │ │ DECODE AND SELECT   │ │ │ L │
│             │  │ │     OPERANDS        │ │ │ E │
│             │  │ └─────────────────────┘ │ │ R │
│             │  │ ┌─────────────────────┐ │ │   │
│             │  │ │ ADDRESS GENERATION  │ │ │   │
│             │  │ │    AND EXECUTE      │ │ │   │
│             │  │ └─────────────────────┘ │ │   │
└─────────────┘  └─────────────────────────┘ └───┘
┌──────────────────────┐  ┌──────────────────────┐
│    DEBUG MODULE      │  │    JTAG INTERFACE    │
└──────────────────────┘  └──────────────────────┘
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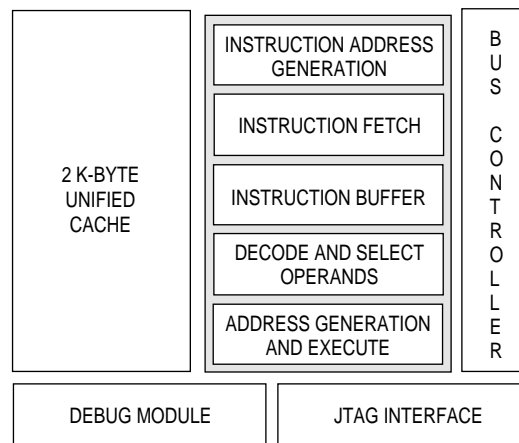
Features

- Variable-length RISC code density
  - Requires less memory than fixed-length RISC equivalents
  - Uses slower memory for a given performance level rather than fixed-length RISC
  - Improves effectiveness of cache memory
- Simple instruction set architecture
  - Sixteen user-visible 32-bit wide registers
  - Designed to minimize die size
- Supervisor/user modes for system protection
- Vector base register to relocate exception vector table
- Optimized for high-level language constructs
  - 2-Kbyte on-chip unified cache
- High-performance nonblocking cache implementation
- Four-way set associative
- Dynamic bus sizing
- 32-, 16-, and 8-bit bus support on MCF5202 processor
- 16- and 8-bit bus support on MCF5203 processor
- Debug module with background debug (BDM) and real-time debug support
- Low interrupt latency accelerates responsiveness in real-time applications
- Full static design allows operation down to DC to minimize power consumption
- Three-state pin
- JTAG IEEE 1149.1
- Single bus clock input
  - Low-cost 100-pin thin quad flat packaging
- Fully supported by the leading industry third-party tools developers

MCF5202, Continued

Target Markets and Applications

The MCF5202 was developed to meet the needs of an emerging class of advanced consumer embedded solutions, such as imaging products, data storage devices, and television set tops.

Key Design Considerations

The key product design considerations for this market include:

- System performance
- Overall system cost
- Ease of application development

The MCF5202 addresses these requirements by providing a "68K-like architecture," 32-bit, variable-length instruction, RISC processor core bundled with a 2K unified cache and debug module in an economical 100-pin, plastic TQFP package. The MCF5202 leverages the many years of 68K application engineering experience combined with excellent code density and 25 MIPS performance.

Motorola's Competitive Advantage

ColdFire has many advantages over the ARM6, ARM7, and ARM7 configured with the Thumb™ preprocessor, including a lower system cost, better performance, and superior tools support.

A lower system cost is achieved by low-cost parts and better code density. ColdFire's better code density means less system memory required, which translates to reduced system cost.

Support by leading third-party tool vendors and the unique feature of the debug module gives ColdFire customers a development environment that is superior to the ARM development environment.

Related Documentation

TITLE	ORDER NUMBER
MCF5202 User's Manual	MCF5202/03UM/D
MCF5202 Product Brief	MCF5202/D
HPESD Embedded Solutions Brochure	EMBSOLUTIONS/D
Coldfire Family Brochure	COLDFIREFAM/D
The High Performance Embedded Systems Source Catalog	BR729/D

MCF5202, Continued

Support Tools   M5202EVM: A hardware/software evaluation module available
                           (requires the M68EC040IDP). Refer to *The High Performance
                           Embedded Systems Division Source Catalog* for third-party support
                           tools.

**Package and Speed
Options**

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XCF5202	100-lead PU	16-, 25-, and 33-MHz	A	—	0	84	420	SPAK5202FUxx

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS

XCF5202/03

```
┌──────────────┐  ┌─────────────────────────┐ ┌───┐
│              │  │  INSTRUCTION ADDRESS    │ │ B │
│              │  │      GENERATION         │ │ U │
│              │  ├─────────────────────────┤ │ S │
│              │  │   INSTRUCTION FETCH     │ │   │
│  2 K-BYTE    │  ├─────────────────────────┤ │ C │
│  UNIFIED     │  │  INSTRUCTION BUFFER     │ │ O │
│  CACHE       │  ├─────────────────────────┤ │ N │
│              │  │  DECODE AND SELECT      │ │ T │
│              │  │      OPERANDS           │ │ R │
│              │  ├─────────────────────────┤ │ O │
│              │  │  ADDRESS GENERATION     │ │ L │
│              │  │    AND EXECUTE          │ │ L │
│              │  └─────────────────────────┘ │ E │
│              │                              │ R │
└──────────────┘                              └───┘
┌──────────────────┐  ┌──────────────────────┐
│  DEBUG MODULE    │  │   JTAG INTERFACE     │
└──────────────────┘  └──────────────────────┘
```
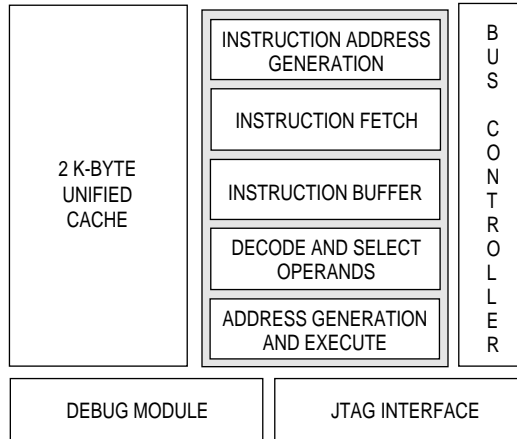
Features

- Fully ColdFire compliant
- Includes ISA extensions to support 680x0 binaries
  - —Bridges 040 legacy to ColdFire
  - —Software reuse
  - —Established tools
  - —Time to market
- 2 Kbyte instruction cache
- 1 Kbyte data cache
- Muxed address/data bus
  - —Low-cost 144-pin TQFP package
- Low power (typically < 1w)

Performance

- 44 Dhrystone 1.1 MIPS @ 40MHz

Power Management

- 3.3v static design
- —I/O to 3v or 5v logic
- Variable frequency operation
- Software powerdown

Technology

- 0.6μm TLM CMOS

XCF5202/03, Continued

**Related
Documentation**

TITLE	ORDER NUMBER
MCF5202 Product Brief	MCF5202/D
MCF5202 Users Manual	MCF5202UM/AD
MCF5203 Product Brief	MCF5203/D

**Target Markets and
Applications**

ColdFire represents a revolutionary microprocessor architecture that has been optimized for embedded processing applications. It brings new levels of price and performance to cost-sensitive, high-volume markets.

**Package and Speed
Options**

DEVICE	PACKAGE	SPEED	RW	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XCF5203PV	TQFP	16, 25	A		—	84	420	SPAK5203PVXX
XCF5202PU	TQFP	16, 25	A		—	84	420	SPAK5203PUXX

XCF5204
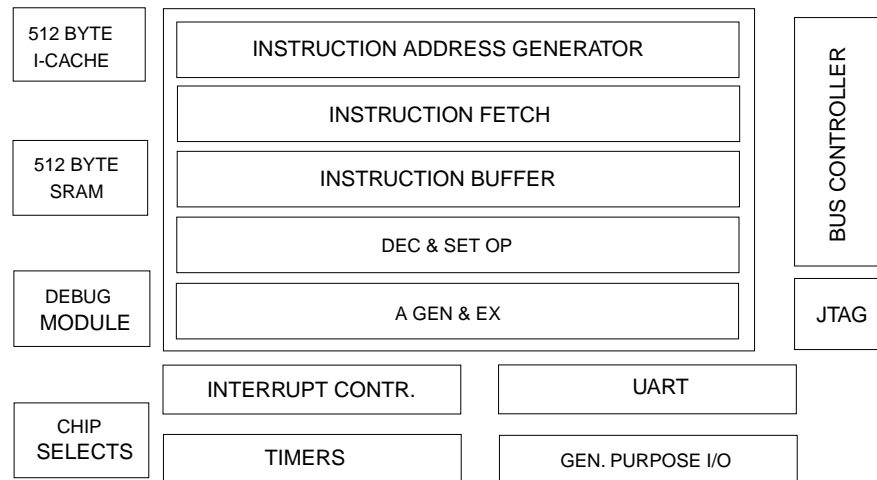
Features	• Fully ColdFire compatible
	• Integrated processor
	—Two 16-bit timers
	—UART
	—General-purpose I/O
	—System integration including chip-selects and interrupt controller
	—Debug Module
	• Asynchronous pseudo-burst bus write static bus sizing
	—16-bit nonmultiplexed data bus
	• 512 byte I-cache and 512 byte I/D SRAM
Performance	13.5 MIPS @ 33 MHz
Power Management	• Variable frequency of operation
	• Software powerdown
Technology	• 0.65μm TLM CMOS
	• 100-pin QFP package
	• Samples available now
	• XC production now

XCF5204, Continued

Target Markets/ Applications   Same as the XCF5202/03

Related Documentation

TITLE	ORDER NUMBER
MCF5204 Product Brief	MCF5204/D
MCF5204 Users Manual	MCF5204UM/AD

Support Tools   M5204AN—a low-cost complete evaluation system. Refer to the *High Performance Embedded Systems Source Catalog* for third-party support tools.

Package and Speed Options

DEVICE	PACKAGE	SPEED	RW	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XCF5204PV	TQFP	16, 25, 33	A		—	84	420	SPAK5204PUXX

XCF5206
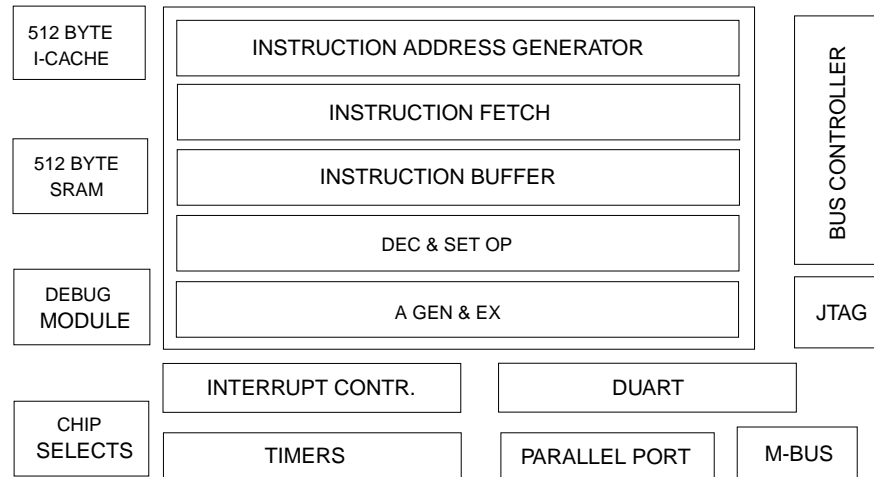
Features

- Fully ColdFire compatible
- Integrated processor
  - DRAM controller (glueless interface)
  - Supports page mode and EDO RAM
  - DUART
  - Chip-selects
  - 8-bit general-purpose I/O
  - M-Bus interface (I^2C compatible)
  - Two 16-bit timers
  - System integration
- 32-bit nonmultiplexed data bus with bus sizing
- 512 byte I-cache and 512 byte I/D SRAM

Performance

17 MIPS @ 33 MHz

Power Management

- Variable frequency of operation
- Software powerdown

Technology

- 0.65 mm TLM CMOS
- 160-pin QFP package
- Samples available now

XCF5206, Continued

Related Documentation

TITLE	ORDER NUMBER
MCF5206 Product Brief	MCF5206/D
MCF5206 Users Manual	MCF5206UM/AD

Support Tools

M5206AN—a low-cost complete evaluation system. Refer to the *High Performance Embedded Systems Source Catalog* for third-party support tools.

Packages and Speed Options

DEVICE	PACKAGE	SPEED	RW	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XCF5206FT	QFP	16, 25, 33	A		0	24	120	SPAK5206FTXX

68K and ColdFire Product Portfolio Overview MOTOROLA

Section 4

The M68300 Family

Overview

Introduction	The M68300 Family consists of highly integrated processors aimed at the embedded computing and control market.

M68300 Product Family	• MC68302* • XC68EN302* • XC68LC302* • XC68PM302* • MC68306 • XC68322 • MC68330/MC68330V • MC68340/MC68340V • XC68356** • XC68360* • XC68376*** * Updated manual on WWW applies to new mask.

Markets Ideally Suited for M68300 Family Products	The M68300 Family continues to dominate the 32-bit architecture industry in the area of integrated processors by focusing on customer needs in the following markets: • **Consumer**—Information terminals, CD-I, global positioning (navigation aids), and personal computing • **Communications**—Network control and telecom applications • **Office Equipment**—Copiers, network interfaces, portable computers, and personal information computers • **Automotive**—Engine and transmission management and navigation systems • **Portable Instruments**—Measuring, monitoring, medical, inventory control, and computers

Overview, Continued

Intermodule Bus

Much of the M68300 Family is centered around the intermodule bus, which allows the device to be assembled from a library of peripheral modules, as shown in the next illustration.

PERIPHERAL LIBRARY

CPU16 · CPU32 · DUART · TIMER · TIME PROCESSOR · DMA (x2) · A/D 10b · GEN. PURPOSE TIMER · SIM A24, D16 · SCIM A24, D16 · SRAM .5, 2, 3.5K · SIM A32, D16 · EEPROM 16, 48K · QUEUED SERIAL

68300

CORE PROCESSOR

PERIPHERALS

MC68306

```
                          ↕ 8

   ┌──────────────┬────────┬──────────────────┐
   │    DRAM      │        │                  │
   │  CONTROLLER  │ PORT A │                  │
   ├──────────────┤        │                  │──→ 24
   │    CHIP      │        │      EC000        │
   │   SELECTS    │        │      CORE         │
   ├──────────────┤   M    │    PROCESSOR      │←─ 16
   │  INTERRUPT   │   C     │                  │
   │  CONTROLLER  │   6     │                  │
   ├──────────────┤   8     │                  │
   │    CLOCK     │   3     │                  │
   ├──────────────┤   0     ├──────┬───────────┤
   │    MODE      │   6     │      │   TWO-     │
   │  CONTROLLER  │        │16-BIT│  CHANNEL   │
   ├──────────────┤ PORT B │TIMER │  SERIAL    │
   │    JTAG      │        │      │   I/O      │
   │    PORT      │        │      │           │
   └──────────────┴────────┴──────┴───────────┘

                          ↕ 8
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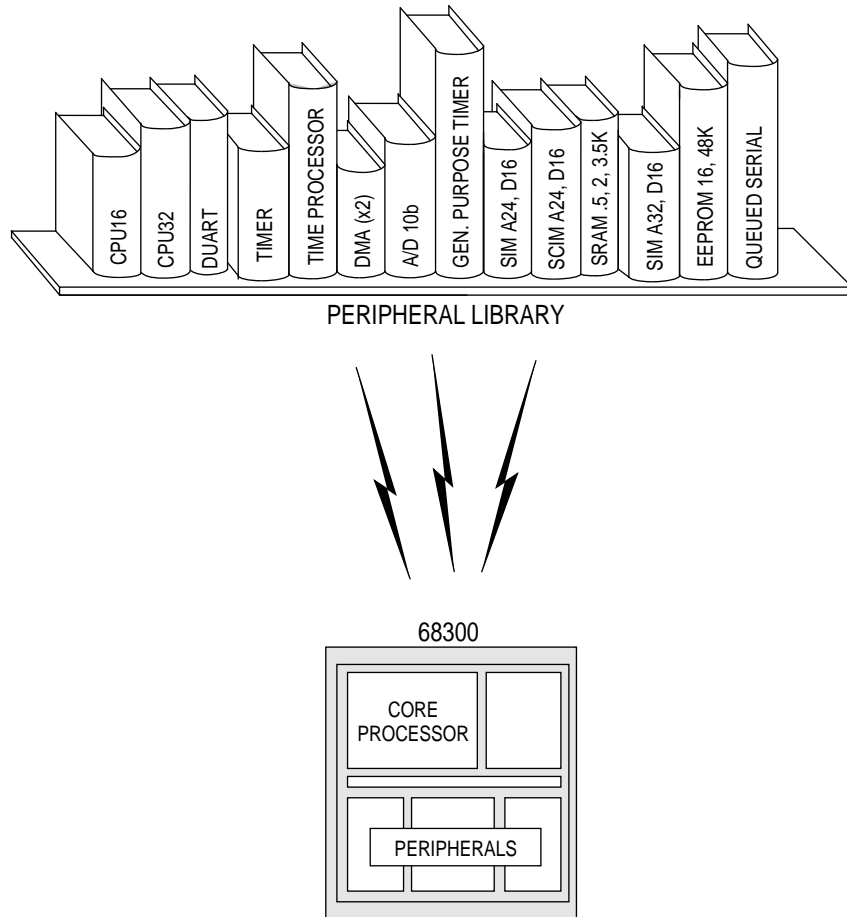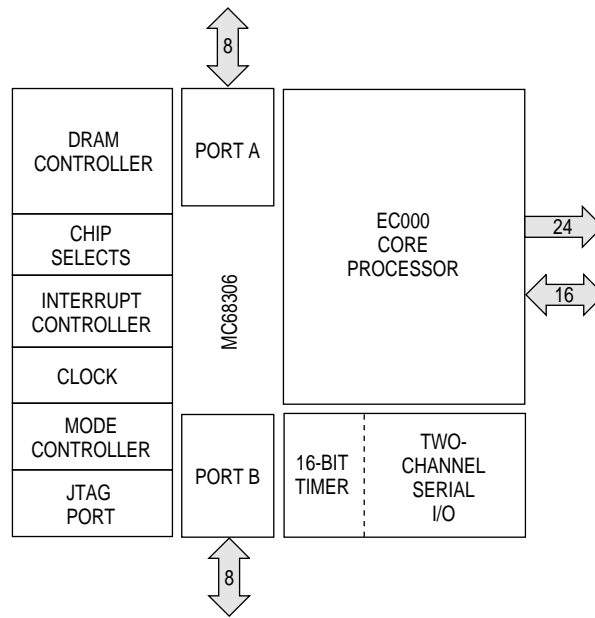
Features

- EC000 core CPU
- MC68681 two-channel serial UART
- DRAM controller
- Sixteen parallel I/O
- 3.3 MIPS performance at 20 MHz
- Internal 32-bit address
- Supports up to 4G of DRAM

Target Markets and Applications

The MC68306 is a highly integrated device with a DRAM controller priced under ten dollars. As such, it holds broad appeal to designers of MC68000-based systems. The integrated features—particularly the DRAM controller—simplify system design and speed time-to-market.

Motorola's Competitive Advantage

Motorola's MC68306 processor is unique in that it offers a glueless interface to DRAM. Competitors like the Intel 80186 and the Toshiba 68301 and 68308 all lack DRAM control. And even though the Intel 80186 is priced low and has a similar performance to the MC68306, its multiplexed address and data bus lower the processor's efficiency.

MC68306, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68306 Product Brief	MC68306/D
MC68306 User's Manual	MC68306UM/AD*
M68000 Programmer's Reference Manual	M68000PM/AD
68300 Family Brochure (Rev 3)	BR1114/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68306AN: Refer to *The High Performance Embedded Systems Source Catalog* for information on third-party support.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68306	132-Lead FC	16/20 MHz	A	0 to 70∞ C	0	36	144	SPAK306AFC*xx*
	144-Lead PV	16/20 MHz	A	0 to 70∞ C	0	60	600	SPAK306APV*xx*
	132-Lead CFC	16/20 MHz	A	-40∞ to +85∞ C	0	36	144	

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
E94M	4		MOS8	0.8m	Production	Yes	—	Fab process improvements "MC" rev
E94M	3		MOS8	0.8m	Discontinued	Yes	—	
E94M	2		MOS8	0.8m	Cancelled	Yes	—	
E94M	1		MOS8	0.8m	Cancelled	Yes	—	
G71K	2		MOS8	0.65m	Production	Yes	Yes	Fixed DUART errata. Requires hardware capacitor changes.

Status Information

First Silicon: 1Q93
MC Qual Date: 4Q94
Die Size: 293×225
Device: 11,000
Process: HCMOS

XC68322
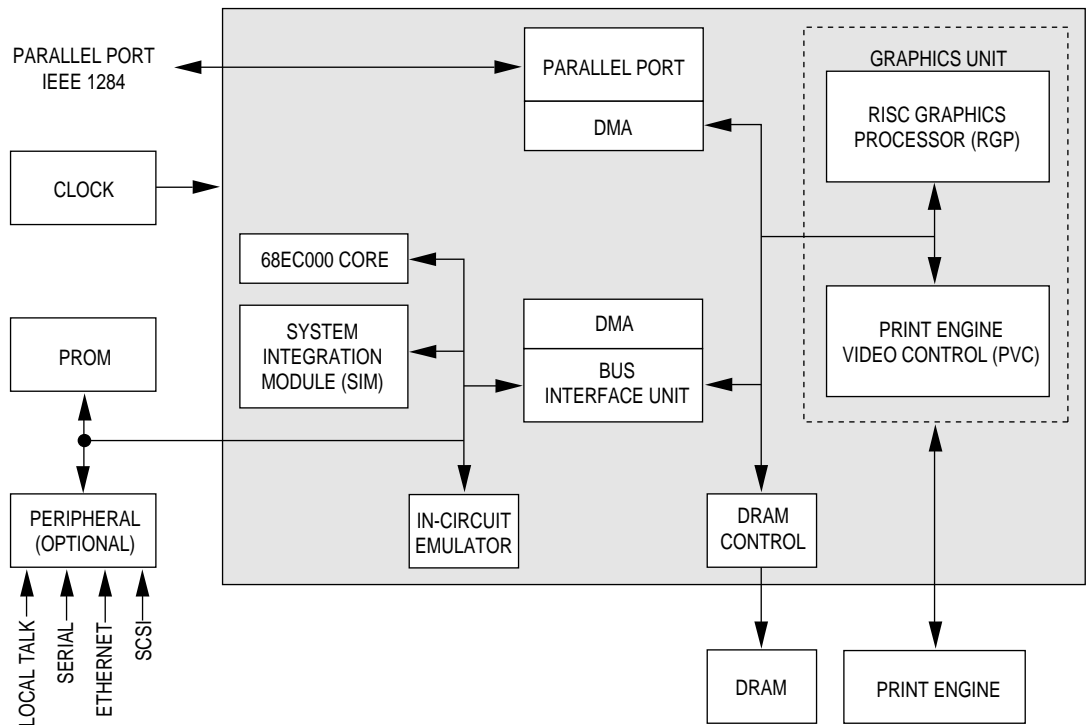
Features

- Static EC000 core processor
- RISC graphic coprocessor
- Print engine video controller
- General-purpose DMA unit
- System integration module
- Parallel communication port (IEEE 1284)
- Low-power device
- Dual-bus architecture
- Distributed processing
- 16 and 20 MHz

Target Markets and Applications

The XC68322 is optimized for the low-end (up to 8 ppm @ 600 dpi) laser printer market. This highly integrated, low-power, single-chip printer solution can also be targeted at

- Inkjet printers
- Multifunction peripherals (fax/modem/printer)
- Bar code printers
- Other portable printing applications

XC68322, Continued

Target Markets and Applications
(Continued)

The XC68322 finds ready applications to other embedded control applications that require very fast bit manipulations.

Motorola's Competitive Advantage

The Intel 960SA is a low-cost RISC processor, but when applied to the printer market, requires ASIC.

Related Documentation

TITLE	ORDER NUMBER
MC68322 Product Brief	MC68322/D
MC68322 User's Manual	MC68322UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
M68300 Brochure (Rev 3)	BR1114/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

- M68322 ICE (In-Circuit Emulation Adaptor Board)
- M68322 EVS (Evaluation System)

Refer to *The High Performance Embedded Systems Source Catalog* for information on third-party support.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
XC68322	160-Lead FT	16- and 20-MHz	—	—	0	24	96	SPAK322FT*xx*

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
F65E	2	75%	MOS8	0.8m	XC	—	—	Fixed bus contention problem
F65E	1	75%	—	—	—	—	—	Fixed assorted design anomalies
F65E	0	75%	MOS8	0.8m	Cancelled	—	—	Original silicon

XC68322, Continued

Status Information   First Silicon: 1Q94
Production Date: 3Q95
Die Size: 331×389
Device: 120,000 (74,000 Active)
Process: CMOS

MC68330/MC68330V
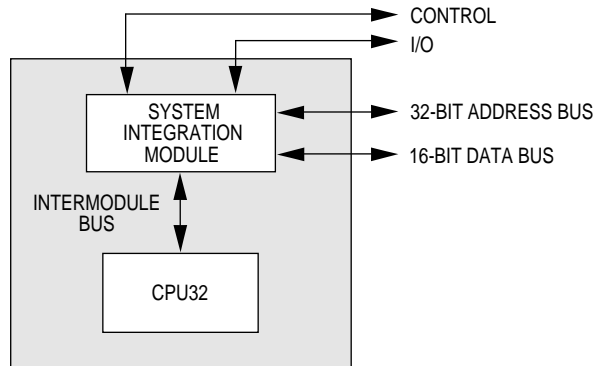
Features	• CPU32 processor • System Integration Module (SIM40) • 3.3 V operation available (68330V only) • 8.3 MIPS performance at 25 MHz
Target Markets and Applications	Applications that require a MC68020 performance from a 16-bit memory system, minimal glue logic (SIM40 contains most of it), static design/low power modes, 5.0 and 3.3 V parts, and a MC68000 upgrade solution for CPU32 performance without any on-chip peripherals. Also, the ability to operate at 3.3 V makes the MC68330V an ideal solution for portable applications.
Motorola's Competitive Advantage	The MC68330 is a low-cost general-purpose part of the CPU32.

Related Documentation

TITLE	ORDER NUMBER
MC68330 Product Brief	MC68330/D
MC68330 User's Manual	MC68330UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
M68300 Family Brochure (Rev 3)	BR1114/D
The High Performance Embedded Systems Source Catalog	BR729/D

MC68330, Continued

Support Tools   Refer to *The High Performance Embedded Systems Source Catalog* for information on third-party support.

Support Chips   M68340EST—Low-cost evaluation system

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68330PV	144-Lead PV	16- and 25-MHz	A	CPV16	0	60	240	SPAK330PV*xx*A
MC68330V	144-Lead PV	16-MHz	A	CPV25	0	60	240	SPAK330PV*xx*VA

* Not recommended for new designs.
V = Suffix for 3.3 V

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
1E84J	C	75%	MOS8	0.8m	Production	Yes	—	Reduced errata
1D81H	B	75%	MOS8	0.8m	Cancelled	Yes	—	
D81H	A	75%	MOS8	0.8m	Cancelled	Yes	—	
D37E	0	67%	MOS8	1.0m	Cancelled	Yes	—	

Status Information   First Silicon: 2Q91
MC Qualification Date: 2Q95
Die Size: 268 ¥ 230
Devices: Sites = 235,000; Active = 130,000
Process: HCMOS

MC68340/MC68340V
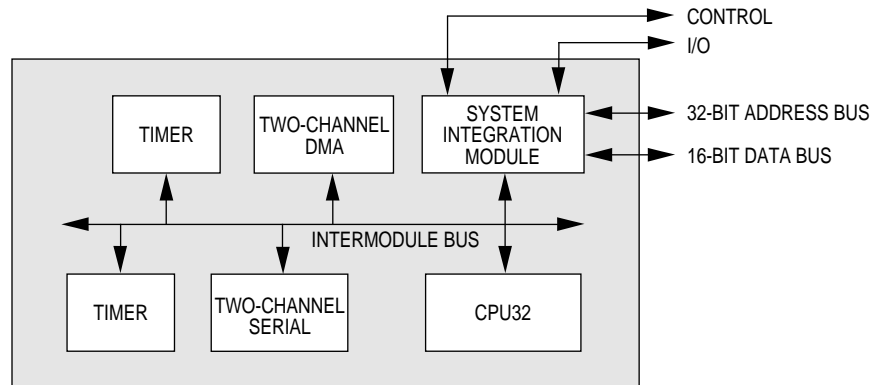
Features

- CPU32 processor
- System Integration Module (SIM40)
- Two-channel DMA controller
- Two-channel serial UART
- Two timer modules
- 3.3 V operation available (MC68340V only)
- 8.3 MIPS performance at 25 MHz

Target Markets and Applications

The MC68340 is targeted toward high-speed data movement products, such as terminals, disk controllers, printers, copiers, CD-I, audio/video processing, and global positioning systems (navigation aids). Another market to tap into is mobile/portable applications, which includes products like pen-based and portable computers, portable phones, and medical instruments.

The ability to operate at 3.3 V makes the MC68340V ideal for portable applications.

Motorola's Competitive Advantage

The MC68340 has a DMA, which makes for fast data transfer. This quality is lacking in its competitor, the ARM Butterfly®. Unlike the MC68340, the Butterfly's interface to SRAM demands expensive 40 ns memory and without it, performance is cut in half. The MC68340 allows SRAM to be used at varying speeds. The Butterfly's advantage, however, is its low cost and conservative power consumption.

Because of its high integration and the availability of low voltage parts, the MC68340 has a definite advantage over the Intel 960SA/B whose big selling point is that it offers a wide variety of speeds.

MC68340/MC68340V, Continued

Related Documentation

TITLE	ORDER NUMBER
MC68340 User's Manual (Rev 1)	MC68340UM/AD
MC68340 Product Brief	MC68340/D
MC68340 User Manual Addendum	MC68340UMAD/AD
M68300 Family Brochure (Rev 3)	BR1114/D
The High Performance Embedded Systems Source Catalog	BR729/D

Support Tools

M68340EST—Low-cost evaluation system. Refer to *The High Performance Embedded Systems Source Catalog* for information on third-party support.

Package and Speed Options

DEVICE	PACKAGE	SPEED	REV	TEMP	ORDER QUANTITY			FOR SAMPLE ORDER
					SOQ	MPQ	POQ	
MC68340	144-Lead FE	16-** and 25-MHz	E	CFE16, CFE25	0	24	96	SPAK340FE*xx*E
	144-Lead PV	16-** and 25-MHz	E	CPV16, CPV25	0	60	60	SPAK340PV*xx*E
	144-Lead FT	16- and 25-MHz	E	—	0	24	96	SPAK340FT*xx*E

*Not recommended for new designs.
**Available in 3.3 V.

Product History

MASK	REV	SHRINK	FAB	GEO	STATUS	ERRATA	PCN	COMMENTS
0G67F	P	80%	MOS11	.65m	Production	Yes	Yes	MC orders
2F77J	N	75%	MOS8	.8m	Production	Yes	Yes	
2E16G	K	75%	MOS8	.8m	Cancelled	Yes	Yes	
2D75M	G	70%	MOS8	1.0m	Cancelled	Yes	—	
D97R	H	70%	MOS8	.8m	Cancelled	Yes	—	Was shipped only as XC
1D75M	F	70%	MOS8	1.0m	Cancelled	Yes	—	
D75M	E	70%	MOS8	1.0m	Cancelled	Yes	—	Few shipped. Max 40
1D76F	D	70%	MOS8	1.0m	Cancelled	Yes	—	
D45C	B	70%	MOS8	1.0m	Cancelled	Yes	—	
1C67H	A	70%	MOS8	1.0m	Cancelled	Yes	—	Released Sept 1990

MC68340/MC68340V, Continued

Status Information   First Silicon: 2Q90
MC Qualification Date: 1Q92
Die Size: 331×316
Devices: Sites = 350,000; Active = 245,000
Process: HCMOS

Section 5

Competitive Analysis

Overview

This section contains information on competitive products and the Motorola solution.

Advanced Micro Devices (AMD)

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
2903X	• RISC core • Surface mount capability • 4-Kbyte on-chip instruction cache	• Poor DRAM performance • Lacks on-chip data cache • Lacks competitive pricing structure • 29035 only in 16 MHz	68EC030/040
29005/050	• RISC core • 17–32 MIPS at 40 MHz • Floating point support	• MIPS rating is less than an 040 at same clock frequency • Poor DRAM performance	68040V and LC040
29030	• 8-Kbyte I-cache; 4-way set-associative; 4-word block size • Salable clocking technology • Programmable bus sizing (16- or 32-bit DRAM interface) • Pin-compatible with other 29K family processors		
29035	• 4-Kbyte direct-mapped I-cache • 16 MHz operating frequency		
29040	• Bus and ASIC compatible with AM29030 processor • On-chip 8 Kbyte I-cache • On-chip 4 Kbyte data cache with control of cache capability • Hardware integer multiplier • 3.3V power supply with 5V-tolerant I/O • Flexible on-chip MMU • Scalable clocking technology • Support for simple page-mode and inter-leaved memories		
29200	• Performance (RISC vs. CISC)	• Lacks competitive pricing structure • Limited integration • Lacks a low power mode	68340

	• Integrated device for laser printers	• Available only at 16 MHz • Performance-to-cost ratio is lower than a 25-MHz EC020 • Lacks general-purpose functionality	EC020
286	• Intel architecture	• Register set is not 32 bit, dedicated registers • Segmented addressing range • Available only with a 16-bit data bus • Lacks CMOS technology	EC020
	• Intel architecture • Performance comparable to a CPU32	• Lacks integration • High system cost	CPU32
386	• Intel 32-bit architecture • CMOS implementation	• Compatibility/performance issues with 286 • Low-performance architecture • Lacks on-chip caches and a burst mode	EC030/030

ARM

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
Spider	• Low power consumption • PCMCIA interface	• No parallel I/O • Demands expensive high speed memory and without it performance is low	68340
610/710	• Competitive pricing structure • Small core • Second sources through Sharp VLSI, GPS • Low power • Fully static design clock		ColdFire 2 core
810	• Five-stage pipeline (fetch, decode, execute, memory, and write) • On-chip PLL; full MMU • 8 Kbyte unified writeback cache • High performance DSP multiplier • Uses branch prediction • 80 MIPS @ 3.3V (Dhrystone 2.1) • 500 mW power consumption • $55mm^2$ core area, 0.5m technology • Many under license by VLSI • May also be offered by other ARM partners		
Strong ARM	• Jointly developed with Digital Equipment		

SA110	• Available in 100, 160, 166, 200, and 233 MHz internal clock speeds • 115 MIPS (Dhrystone 2.1) @ 100 MHz, 1.65V; < 300 mw power • 185 MIPS (Dhrystone 2.1) @ 160 MHz; 450 mw • 270 MIPS (Dhrystone 2.1) @ 233 MHz; < 1w power • Five stage pipeline • 16 Kbyte I-cache • 16 Kbyte writeback data cache • Write buffer • Full MMU support for internal memory systems • Power-down modes • Fast interrupt response; <1µs real-time applications • 144-pin TQFP • Most power-efficient (MIPS/watt) processor available		
Thumb	• 32-bit performance at 8/16-bit system costs • Excellent code density for minimal system memory size at cost • 32-bit performance from 8- or 16-bit memory or 8- or 16-bit bus for low system cost • Industry-leading MIPS/watt for longer battery life • Small die size for integration and minimum chip cost • Global multipartner sourcing for secure supply		
ARM7/IDMI	• Full 32-bit ARM architecture		
	• Supports both full ARM and Thumb instruction sets • 3V and 5V operation • 26 MIPS (Dhrystone 2.1) in 16-bit system @ 40 MHz • 31 MIPS (Dhrystone 2.1) in 32-bit system @ 40 MHz • 322 MIPS/watt • Embedded ICE macrocell • 64-bit DSP multiplier Thumb is an extension to the 32-bit ARM architecture. The Thumb instruction set features a subset of the most commonly used 32-bit ARM instructions, which have been compressed into 16-bit wide operators. At execution, these 16-bit instructions are decompressed transparently to full 32-bit ARM instruction in real-time without performance loss		

Hitachi

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
HC000	• Competitive pricing structure	• Lacks the proprietary Hitachi architecture • Lacks second-source support network	HC000
H8/500	• Analog-to-digital on chip • Favorable timer performance • Convenient packaging	• Poor CPU performance • Low serial channel performance • Lacks flexibility of time processor unit	68331/332
7604	• 32-bit MAC • Full 32-bit architecture • Direct interface to synchronous DRAMs	• Lacks support tools	5206
7702	• Up to 45 MHz • 40 MIPS @ 45 MHz/3/3V • 32-bit MAC • Supports PSRAM, PCMCIA (1 slot), DRAM • Three 32-bit timers • 120-lead TQFP		
7708	• Up to 60 MHz • 60 MIPS @ 60 MHz/3.3V • 32-bit MAC • Supports PCMCIA (2 slots), SDRAM, DRAM, SRAM • Three 32-bit timers • 144-lead QFP		

IBM

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
401 GF	• 401 core • Compatible with PowerPC User Instruction Set Architecture • 32-bit x 32 general-purpose registers • Low power; operating voltage between 2.5V and 3.3V • Active power consumption, 40mw @ 25MHz/2.5V • Sleep mode power is as low as 0.015 mw • 0.5mm CMOS, TLM • Operates in 1:1, 2:1, 3:1, and 4:1 (100 MHz, 75 MHz, 50 MHz, 25 MHz) • 80-pin TQFP		
403GA/B	• Hardware multiplier/divider • DMA controller	• Lacks a competitive pricing structure	5206, MPC860
403 GCX	• Pin-compatible upgrade to 403GC • 16K I-cache • 8K I-cache • Dynamic power management • 0.45mm CMOS TLM		

IDT

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
3051/2	• R3000 core • Competitive pricing structure	• Poor DRAM performance • Contains a multiplexed bus • Inferior development tools	68040V and EC040
3040	• Competitive pricing structure	• Poor DRAM performance • Contains a multiplexed bus • Inferior development tools	EC030
3041	• Low cost • 16 — 33MHz		
3051/2	• (E) version has MMU and 10 Kbyte cache		
3081(E)	• RISC controller with FPU • 20—50 MHz • 20 Kbyte cache • (E) version has MMU • 3.3V version available (79RV3081)		
36100	• Highly integrated CPU • 20 - 33MHz • 5 Kbyte cache		

Intel

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
960SA/B	• Available at fast speeds	• Lacks integration • Poor performance-to-cost ratio • Lacks low-voltage parts	68340 (25 MHz)/68360
	• Floating-point support on 960SB • Limited burst mode	• Contains a multiplexed bus • Requires expensive memory for performance • RISC uses memory inefficiently	EC020
960KA/B	• RISC core (microcoded)	• Poor DRAM performance • Inferior development tools • Not x86 code compatible • Lacks competitive pricing structure • Contains a multiplexed bus • Lacks a data cache	EC030
196		• Lacks competitive pricing structure • Lacks an upgrade path • Poor architecture • Contains an 8-bit bus	EC000
	• Analog-to-digital on chip • Cost-effective 16-bit microcontroller unit	• Lacks integration • Poor performance	68331/332/334
186	• Solid software base • Competitive pricing structure	• Lacks 32-bit architecture • Nonorthogonal architecture • Lacks good migration path with integration	EC000

	Features	Limitations	Replacement
	• Eight additional chip selects • On-board memory refresh • Runs DOS	• Poor CPU performance (0.5 ¥ CPU32) • Low addressing range • Lacks JTAG support • Poor DMA performance • Lacks communications support	68340
	• Two DMA channels	• Low addressing range • Lacks DRAM controller • Lacks JTAG support • Lacks communications support	68306
386SX/SXSA	• 16-bit bus creates smaller packaging	• Performance is limited by 16-bit bus • Compatibility/performance issues with 286 • Low-performance architecture • Lacks on-chip caches and burst mode	EC030
386CXSA	• Static design with System Management mode • 64M address space • TTL I/O		
386CXSB	• Static design • 64M address space • CMOS (3.3V) input levels		
386DX	• Intel 32-bit architecture • CMOS implementation	• Compatibility/performance issues with 286 • Low-performance architecture • Lacks on-chip caches and burst mode	EC030
386EX/TB	• 24 I/O pins • 3 serial ports • 3 timers/counters • Static design • 64M address space • 2 DMA channels • 8 chip-selects • Interrupt controller • TTL • Power saving modes • 3V input levels		
386EX/TC	• 24 I/O pins • 3 serial ports • 3 timers/counters • Static design • 64M address space • 2 DMA channels • 8 chip-selects • Interrupt controller • TTL • Power saving modes • 5V input levels		
386EX/SA	• 24 I/O pins • 3 serial ports • 3 timers/counters • Static design • 64M address space • 2 DMA channels • 8 chip-selects • Interrupt controller • CMOS • Power saving modes • 5V - 3V input levels		

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
486(G)XSF	(G) 16-bit bus • Embedded 486 • Ultra low power (typically 20-50% less than 486SX) • Provides all of the features of the 486SX processor except for the external data-bus parity logic and the processor-up-grade pin		
486SX	• Entry point to 486 architecture • Surface mount capability	• Involved in a confusing marketing strategy with the 487SX • Architecture less powerful than the 040 • Unified cache creates a bottleneck	EC030/EC040/ LC040/040V
486D	• Tailored for PCs	• Lower performance than an 040 at same clock (50-MHz 486 = 33-MHz 040) • Unified cache creates a bottleneck • Lacks copy back cache due to a poor multiprocessor	68040
8051	• Inexpensive	None	EC000
	• Competitive pricing structure	• Poor performance-to-cost ratio	68330
368EX	• Upward compatible with x86 code • Low power • Supports inexpensive memory	• Lacks on-chip cache	

LSI Logic

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
LR33020	• Targeted at X-terminals • Cut-down R3000 core	• Poor DRAM performance • Not general purpose • Inferior development tools	68040V and EC040
33000	• Cut-down R3000 core • Integrated peripherals • Surface mount capabilities	• Poor DRAM performance • Poor performance-to-cost ratio • Inferior development tools	EC030

National Semiconductor

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
NS32FX16	• On-board DSP • Convenient packaging	• Limited installed software base • Lacks configurable timing capabilities	68331/332

NEC

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
V25/25+ V35/V35+	• Competitive pricing structure • Single-chip versions available • Runs DOS	• Limited communications capability • Low addressing range • Low performance	68340

78kVII	• Competitive pricing structure	• Only half the performance of a 302 • Lacks timer/flash/microcode capabilities • Lacks low-power capabilities • Limited installed software base	68331/332/333/340
V850OE/MS1 μPD70F3102	• 52 MIPS @ 40 MHz • Flash: 128 Kbyte • RAM: 4 Kbyte • 16-bit data bus with 8-bit bus sizing function • Memory controller supports EDO DRAM, direct connection function with fast-page DRAM, page DRAM, synchronous FLASH, SRAM • 32-bit MAC • CSI/UARTx2ch; CSIx2ch; dedicated baud-rate generator x3ch • 10-bit resolution A-D x8ch • HALT/IDLE/STOP modes • Power supply/internal unit: 3.3V; external: 5V; A/D converter: 3.3V • Power consumption 160mW (3.3v and 5V, 40 MHz Target) • 144-pin LQFP (20 x 20mm) Applications: printers, video printers, digital still cameras, fax machines, DVDs, etc.		
V850E/MS1 μPD703101	· Mask ROM: 96 Kbyte · RAM: 4 Kbyte • 16-bit data bus with 8-bit bus sizing function • 32-bit MAC • 10-bit resolution A-D x8ch • HALT/IDLE/STOP modes		
V850E/MS1 μPD203100	• RAM: 4 Kbyte • 16-bit data bus with 8-bit bus sizing function • 32-bit MAC • 10-bit resolution A-D x8ch • HALT/IDLE/STOP modes		
V853 μPD70F3003	• 38 MIPS @ 33 MHz • Flash • FEPROM: 128 Kbyte • RAM: 4 Kbyte • UART • A to D and D to A converters • 100-pin 14 x 14 mm QFP • PWM • 32-bit MAC • HALT/IDLE/STOP modes • 32-bit MAC • 0.6mm DLM		

V853 µPD703003	• 38 MIPS @ 33MHz • Mask ROM: 128 Kbyte • RAM: 4 Kbyte • UART • A to D and D to A converters • PWM • 32-bit MAC • HALT/IDLE/STOP modes • 0.6mm DLM		
V851 µPD703001	• 3V to 5.5V • 28 MIPS (25 MHz) • ROM: Less • RAM: 1 Kbyte • Dual 16-bit timers • 32-bit MAC • UART, CSI, dedicated baud-rate generator • HALT/IDLE/STOP modes • 270 mW (5V, 33 MHz) • 100-pin QFP (14 x 14 mm)		
V851 µPD703000	• 3V to 5.5V • 38 MIPS (33 MHz) • Mask ROM: 32 Kbyte • Mask RAM: 1 Kbyte • Dual 16-bit timers • 32-bit MAC • UART, CSI, dedicated baud-rate generator • 270 mW (5V, 33 MHz) • 100-pin QFP (14 x 14 mm)		
V851 µPD70P3000	• 3V to 5.5V • 38 MIPS @ 33 MHz • PROM: 32 Kbyte • RAM: 1 Kbyte • Dual 16-bit timers • 32-bit MAC • UART, CSI, dedicated baud-rate generator • 330 mW (5V, 33 MHz) • 100-pin QFP (14 x 14 mm)		
V852 µPD703002	• 29 MIPS @ 25MHz • Mask ROM: 90 Kbyte • Mask RAM: 3 Kbyte • 32-bit MAC • Dual 16-bit timers • UART; 3-channel CSI; dedicated dual channel baud-rate generator • HALT/IDLE/STOP modes • 217 mW (5V, 25MHz) • 100-pin QFP (14 x 14 mm) Applications: HDDs, PPCs, VTRs, motor controls, robots, camcorders, LBRs, mobile terminals, digital telephone technology		

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
V852 μPD70P3002	• 29 MIPS (25 MHz) • PROM: 90 Kbytes • RAM: 3 Kbyte • 32-bit MAC • Dual 16-bit timers • HALT/IDLE/STOP modes • 320 mW (5V, 25MHz)		
V854 μPD70F3008 μPD70F3008Y	• 38 MIPS (33 MHz) • Flash: FEPROM: 128 Kbyte; RAM: 4 Kbyte • 32-bit MAC • Dual 24-bit timers: 6-channel 16-bit timer; 8-channel realtime output port • CSI/UART, CSI/I^{2}C*, CSIx2ch; 4 ch dedicated baud-rate generator • 16-channel 8-bit resolution A-D converter • HALT/IDLE/STOP modes • 2.7V to 3.6V supply voltage • Typical power consumption: 118 mW (3V, 33MHz target) • 144-lead LQFP (20x20mm) * I^{2}C is incorporated in MPD70F3008Y and MPD703008Y		
V854 μPD703008 μPD703008Y	• 38 MIPS @ 33MHz • MASKROM: 128 Kbyte; RAM:4 Kbyte • 32-bit MAC • Dual 24-bit timers: 6-channel 16-bit timer; 8-channel realtime output port		

SGS-Thomson

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
ST10F166	• Solid interrupt handler	• Limited flash EEPROM • A third of available RAM size • No silicon yet	68F333

Siemens

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
80C166	• Solid interrupt handler	• Limited installed software base • Architecture not widely accepted • Lacks user-configurable timers	68331/332

Toshiba

DEVICE	PRODUCT QUALITIES	PRODUCT LIMITATIONS	THE MOTOROLA SOLUTION
HC000	• Competitive pricing structure	• Lacks proprietary Toshiba architecture • Lacks second-source support network	HC000
	• Competitive pricing structure	• Low performance • Lacks integration	68330
	• Built-in Centronics • Additional serial channel	• Lacks DRAM controller • Limited address space	68306
	• Built-in Centronics	• Lacks DMA • Low CPU performance • Lacks low power mode option	68340
68303	• Superior timer • Dedicated motor control • Robust DRAM controller	• Only three DMA channels • Low CPU performance	68340
	• Superior timer • Dedicated motor control • Solid DMA	• Limited address space • Weak DRAM controller	68306
68301AF/AFR	• 12, 16 MHz • 3 UARTs • 3 timers • 100-pin QFP • 100-pin RFP		
68305F	• 2-channel UARTs • 2 DMA channels • Address decoder • 100--pin QFP		

68K and ColdFire Product Portfolio Overview

Section 5

Product Routing Information

DEVICE NAME AND PACKAGING CODES	FAB SITE	PROBE	ASSEMBLY SITE	FINAL TEST SITE
68EC000FN	MOS8/MOS10/TSC	OHT/MOS10/TSC	KLM/ASTRA	KLM
68EC000FU	MOS8/MOS10/TSC	OHT/MOS10/TSC	SHC	SHC
68HC000RC,FN,FC	MOS8/MOS10/TSC	OHT/MOS10/TSC	KLM/ASTRA	OHT/KLM/(FN)
68HC000P	MOS8/MOS10/TSC	OHT/MOS10/TSC	CARSEM/KLM	OHT/KLM(RC)
68HC001RC,FN	MOS8/MOS10/TSC	OHT/MOS10/TSC	KLM	KLM
68HC001FC	MOS8/TSC	OHT/TSC	KLM	OHT
68020RC	TSC	TSC	KLM	KLM
68020FE	TSC	TSC	KLM	KLM
68020RP	TSC	TSC	CITIZEN	NML
68020FC	TSC	TSC	KLM	KLM
68EC020RP	TSC	TSC	CITIZEN	NML
68EC020FG	TSC	TSC	ASTRA	SHC
68030RC	MOS8/TSC	MOS8/TSC	KLM	KLM
68030FE	MOS8/TSC	MOS8/TSC	KLM	KLM
68030RP	MOS8/TSC	MOS8/TSC	CITIZEN	KLM
68EC030RP	MOS8/TSC	MOS8/TSC	CITIZEN	KLM
68040RC, FE	MOS11	MOS11	KLM	KLM
68040RCV	MOS11	MOS11	KLM	OHT
68040FEV	MOS11	MOS11	KLM	OHT
68060RC/68LC060RCE	MOS11	MOS11	KLM	OHT
68306FC	MOS8	OHT	KLM	OHT/KLM
68306PV	MOS8	OHT	SHC	SHC
68307FG	MOS8	OHT	ANAM	SHC
68307PU	MOS8	OHT	SHC	SHC
68322FT	MOS8	OHT	SHC	OHT/SHC

DEVICE NAME AND PACKAGING CODES	FAB SITE	PROBE	ASSEMBLY SITE	FINAL TEST SITE
68330PV	MOS8	MOS8	ANAM	OHT
68340FE	MOS11	MOS11	KLM	KLM
68340PV	MOS11	MOS11	ANAM/SHC/KLM	KLM
68340FT	MOS11	MOS11	ANAM	KLM
68341FT	MOS8	MOS8	ANAM	OHT/KLM
68349FT	MOS8	MOS8	ANAM	OHT
68882RC,FN	MOS8	MOS8	KLM	OHT/KLM
XCF5202PU	MOS8	MOS8	SHC	OHT
XCF5102PV	MOS11	MOS11	SHC	SHC
XCF5204PU	MOS8	MOS8	SHC	OHT
XCF5206FT	MOS8	MOS8	KLM (4Q97)	OHT
GXCV38499FY01	MOS8	MOS8	ASE	SHC

SITE CODE	SITE LOCATION
AIZU	AIZU, JAPAN
ANAM	KOREA
ATX	AUSTIN, TEXAS
CARSEM	MALAYSIA
CHNDLR	CHANDLER, ARIZONA
CITIZEN	CITIZEN, JAPAN
EKB	EAST KILBRIDE, SCOTLAND
KLM	KUALA LUMPUR, MALAYSIA
MESA	MESA, ARIZONA
OHT	OAK HILL, TEXAS
SHC	SILICON HARBOR, HONG KONG
SND	SENDAI, JAPAN
SWIRE	HONG KONG
TSC	TOHOKU, JAPAN

WAFER FAB	FAB LOCATION	WAFER SIZE (INCHES)	PROCESS TECHNOLOGY
MOS1	EKB	4	>1.2 MICRON
MOS2	ATX	4	LOGIC PRODUCT
MOS3	ATX	4	>1.2 MICRON
MOS5	MESA	5	>1.2 MICRON
MOS6	MESA	6	ASIC PRODUCT
MOS7	AIZU	4	>1.5 MICRON
MOS8	ATX	5	0.65–1.5 MICRON
MOS9	EKB	6	0.8–1.5 MICRON
MOS10		6	0.8–0.65 MICRON
MOS11	OHT	8	0.5–0.8 MICRON
MOS12	CHD	8	<0.8 MICRON
MOS13	ATX	8	0.5–0.8 MICRON
TOHOKU	TSC	6	0.5–1.5 MICRON

68K and ColdFire Product Portfolio Overview MOTOROLA

Section 6

DSP Development Tools

ADS Complete Systems

DEVICE	DESCRIPTION	REVISION
DSP56002ADSA	Application Development Systems for IBM PC	6.0.18
DSP56002ADSF	Application Development System for SUN	6.0.18
DSP56002ADSH	Application Development System for HP700	6.0.18
DSP56005ADSA	Application Development Systems for IBM PC	6.0.18
DSP56005ADSF	Application Development System for SUN	6.0.18
DSP56005ADSH	Application Development System for HP700	6.0.18
DSP56156ADSA	Application Development Systems for IBM PC	6.0.18
DSP56156ADSF	Application Development System for SUN	6.0.18
DSP56156ADSH	Application Development System for HP700	6.0.18
DSP56166ADSA	Application Development Systems for IBM PC	6.0.18
DSP56166ADSF	Application Development System for SUN	6.0.18
DSP56156ADSH	Application Development System for HP700	6.0.18
DSP96000ADSA	Application Development Systems for IBM PC	6.0.18
DSP96000ADSB	Application Development System for MAC	6.0.18
DSP96000ADSF	Application Development System for SUN	6.0.18
DSP96000ADSH	Application Development System for HP700	6.0.18
DSP56301ADSA	Application Development Systems for IBM PC	6.0.18
DSP56301ADSF	Application Development System for SUN	6.0.18
DSP56301ADSH	Application Development System for HP700	6.0.18

Evaluation Modules

DEVICE	DESCRIPTION	REVISION
DSP56002EVM	Evaluation Module for IBM PC	2.2
DSP56007EVM	Evaluation Module for IBM PC	1.0x
DSP56302EVM	Evaluation Module for IBM PC	1.0x
DSP56303EVM	Evaluation Module for IBM PC	1.0x
DSP56811EVM	Evaluation Module for IBM PC	1.0x

DSP Development Tools, Continued

**Assemblers/
Simulators**

DEVICE	DESCRIPTION	REVISION
DSP56000CLASA	Assembler/Linker/Simulator SW for IBM PC	6.0.18
DSP56000CLASF	Assembler/Linker/Simulator for SUN	6.0.18
DSP56000CLASH	Assembler/Linker/Simulator for HP700	6.0.18
DSP56100CLASA	Assembler/Linker/Simulator SW for IBM PC	6.0.18
DSP56100CLASF	Assembler/Linker/Simulator for SUN	6.0.18
DSP56100CLASH	Assembler/Linker/Simulator for HP700	6.0.18
DSP56300CLASA	Assembler/Linker/Simulator SW for IBM PC	6.0.18
DSP56300CLASF	Assembler/Linker/Simulator for SUN	6.0.18
DSP56300CLASH	Assembler/Linker/Simulator for HP700	6.0.18
DSP96000CLASA	Assembler/Linker/Simulator SW for IBM PC	6.0.18
DSP96000CLASF	Assembler/Linker/Simulator for SUN	6.0.18
DSP96000CLASH	Assembler/Linker/Simulator for HP700	6.0.18

C Compilers

DEVICE	DESCRIPTION	REVISION
DSP56KCCA	560xx C Compiler SW for IBM PC	G1.11
DSP56KCCF	560xx C Compiler SW for SUN	G1.11
DSP56KCCH	560xx C Compiler SW for HP700	G1.11
DSP561CCCA	561xx C Compiler SW for IBM PC	G1.11
DSP561CCCF	561xx C Compiler SW for SUN	G1.11
DSP561CCCH	561xx C Compiler SW for HP700	G1.11
DSP563CCA	563xx C Compiler SW for IBM PC	G1.24
DSP563CCF	563xx C Compiler SW for SUN	G1.24
DSP563CCH	563xx C Compiler SW for HP700	G1.24
DSP96KCCA	96000 C Compiler SW for IBM PC	G1.03
DSP96KCCF	96000 C Compiler SW for SUN	G1.03
DSP96KCCH	96000 C Compiler SW for HP700	G1.03

ADS Components

DEVICE	DESCRIPTION	REVISION
DSP56002ADM	Application Development Module	2.0
DSP56004ADM	Application Development Module	1.0
DSP56156ADM	Application Development Module	2.0
DSP56166ADM	Application Development Module	2.0
DSP56301ADM	Application Development Module	1.0
DSP96000ADM	Application Development Module	1.0
DSPPCHOST	Host, Board, Cable, and Debug SW for IBM PC	1.0
DSPSUNHOST	Host, Board, Cable, and Debug SW for SUN	1.0
DSPHPHOST	Host, Board, Cable, and Debug SW for HP700	1.0
DSP56005ADPTR	Adaptor plugs onto DSP56002ADSx	1.0
DSPCOMMAND	Command Converter Board and OnCE Cable	5.0
DSP56004AIB	Analog Interface Board for DSP56004ADSx	1.0

NOTES