

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM TC5563APL-10, TC5563APL-12
SILICON GATE CMOS TC5563APL-15

PRELIMINARY

DESCRIPTION

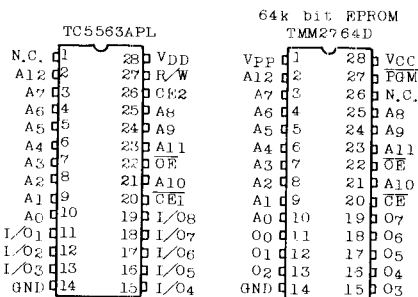
The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE₂ is a logical low or CE₁ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables (CE₁, CE₂) allow for device selection and data retention control, and an output enable input

FEATURES

- Low Power Dissipation
27.5mW/MHz (Max.) Operating
- Standby Current : 100μA (Max.) Ta = 70°C
- Access Time
TC5563APL-10 : 100ns (Max.)
TC5563APL-12 : 120ns (Max.)
TC5563APL-15 : 150ns (Max.)
- 5V Single Power Supply

PIN CONNECTION (TOP VIEW)



PIN NAMES

A ₀ ~A ₁₂	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
CE ₁ , CE ₂	Chip Enable Inputs
I/O ₁ ~I/O ₈	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

(OE) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

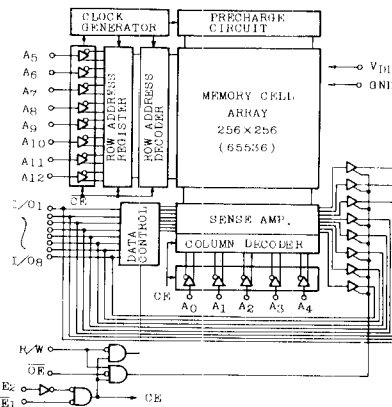
The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

- Power Down Features : CE₂, CE₁
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

*) See TC5565APL Technical Data.

BLOCK DIAGRAM



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OPERATION MODE

OPERATION MODE	CE ₁	CE ₂	OE	R/W	I/O ₁ ~I/O ₈	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDO}
	*	L	*	*	High-Z	I _{DDO}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3*~7.0	V
V _{I/O}	Input and Output Voltage	-0.5~V _{DD} +0.5	V
P _D	Power Dissipation	0.8	W
T _{solder}	Soldering Temperature	260·10	°C·Sec
T _{stg}	Storage Temperature	-55~150	°C
T _{opr}	Operating Temperature	0~70	°C

* : -3.0V at pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3*	—	0.8	V
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : -3.0V at pulse width 50ns

D. C. and OPERATING CHARACTERISTICS (T_a=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
I _{IL}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	—	—	±10	μA		
I _{OH}	Output High Current	V _{OH} = 2.4V	-10	—	—	mA		
I _{OL}	Output Low Current	V _{OL} = 0.4V	4.0	—	—	mA		
I _{LO}	Output Leakage Current	CE ₁ = V _{IH} or CE ₂ = V _{IL} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 ~ V _{DD}	—	—	±1.0	μA		
I _{DD1}	Operating Current	V _{DD} = 5.5V CE ₁ = V _{IL} CE ₂ = V _{IH} Other input = V _{IH} /V _{IL} I _{OUT} = 0mA	t _{cycle} = 1.0μs	—	—	10	mA	
			t _{cycle} = 100ns	TC5563APL-10	—	—	45	mA
				TC5563AFL-10	—	—	—	—
			t _{cycle} = 120ns	TC5563APL-12	—	—	40	mA
				TC5563AFL-12	—	—	—	—
t _{cycle} = 150ns	TC5563APL-15	—	—	35	mA			
	TC5563AFL-15	—	—	—	—			
I _{DD2}	Operating Current	V _{DD} = 5.5V CE ₁ = 0.2V CE ₂ = V _{DD} -0.2V Other input = V _{DD} -0.2V/0.2V I _{OUT} = 0mA	t _{cycle} = 1.0μs	—	—	5	mA	
			t _{cycle} = 100ns	TC5563APL-10	—	—	40	mA
				TC5563AFL-10	—	—	—	—
			t _{cycle} = 120ns	TC5563APL-12	—	—	35	mA
				TC5563AFL-12	—	—	—	—
t _{cycle} = 150ns	TC5563APL-15	—	—	30	mA			
	TC5563AFL-15	—	—	—	—			
I _{DDO1}	Standby Current	CE ₁ = V _{IH} or CE ₂ = V _{IL}	—	—	3	mA		
*I _{DDO2}	Standby Current	CE ₁ = V _{DD} -0.2V or CE ₂ = 0.2V	V _{DD} = 5.5V	—	2	100	μA	
			V _{DD} = 3.0V	—	1	50		

* : In standby mode with CE₁ ≥ V_{DD}-0.2V, these specification limits are guaranteed under the condition of CE₂ ≥ V_{DD}-0.2V or CE₂ ≤ 0.2V.

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CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =GND	10	pF
C _{OUT}	Output Capacitance	V _{OLT} =GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t _{ACC}	Address Access Time	—	100	—	120	—	150	ns
t _{CO1}	CE1 Access Time	—	100	—	120	—	150	ns
t _{CO2}	CE2 Access Time	—	100	—	120	—	150	ns
t _{OE}	Output Enable to Output Valid	—	50	—	60	—	70	ns
t _{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	10	—	10	—	15	—	ns
t _{OEL}	Output Enable to Output in Low-Z	5	—	5	—	5	—	ns
t _{OD}	Chip Enable (CE1, CE2) to Output in High-Z	—	35	—	40	—	50	ns
t _{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	ns
t _{OH}	Output Data Hold Time	20	—	20	—	20	—	ns

Write Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	90	—	ns
t _{CW}	Chip Selection to End of Write	80	—	85	—	100	—	ns
t _{AS}	Address Set up Time	0	—	0	—	0	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	ns
t _{OFW}	R/W to Output in Low-Z	5	—	5	—	10	—	ns
t _{DS}	Data Set up Time	40	—	50	—	60	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	ns

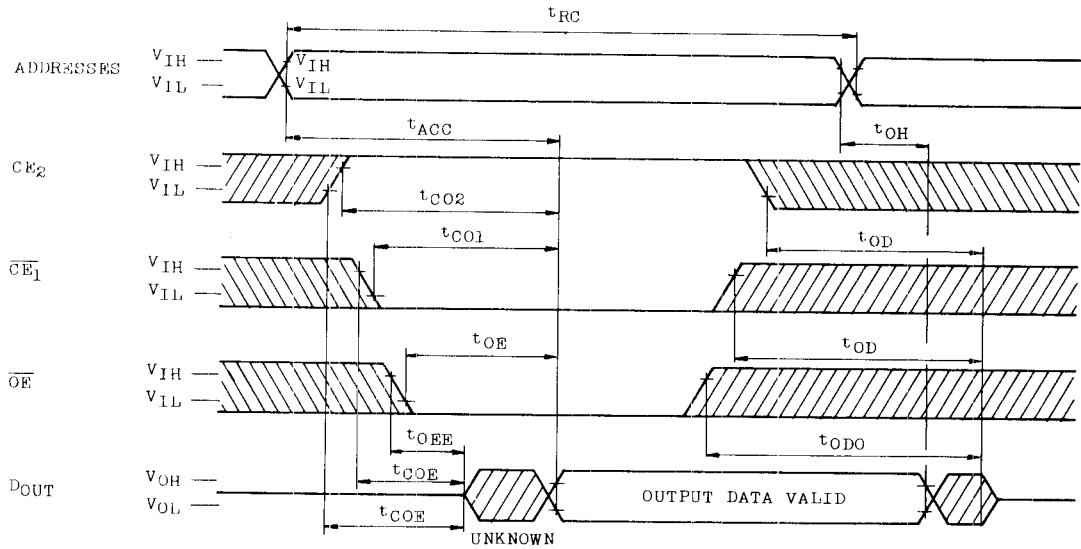
A. C. TEST CONDITIONS

Output Load : 100pF + 1 TTL Gate
 Input Pulse Level : 0.6V, 2.4V
 Timing Measurement V_{IN} : 0.8V, 2.2V
 Reference Level V_{OUT} : 0.8V, 2.2V
 t_r, t_f : 5ns

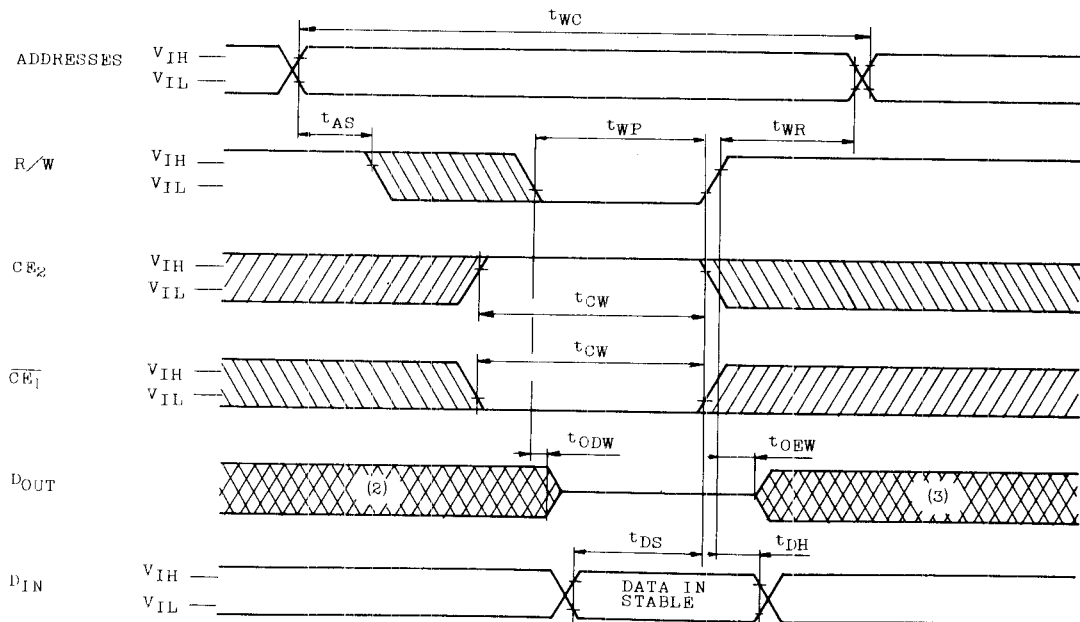
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TIMING WAVEFORMS

● READ CYCLE (1)

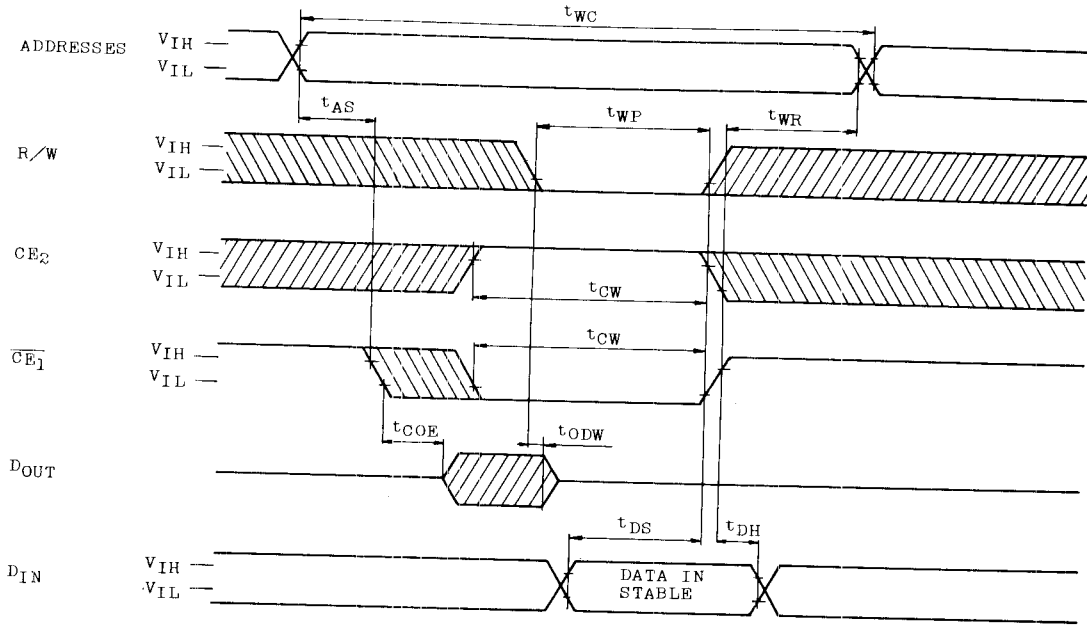


● WRITE CYCLE 1 (4) (R/W Controlled Write)

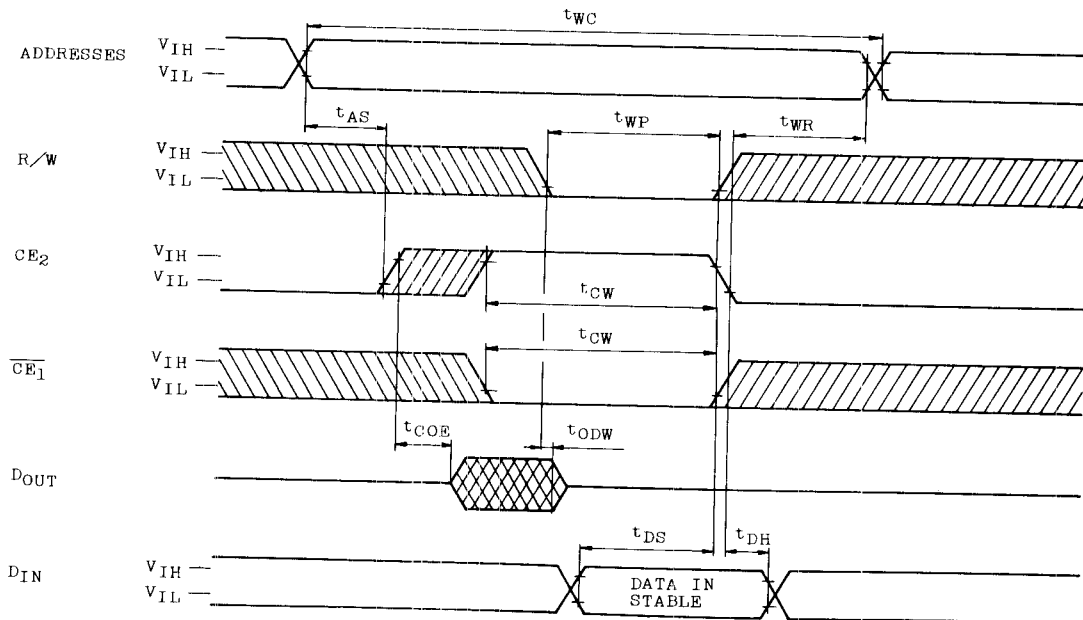


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● WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



● WRITE CYCLE 3 (4) ($CE2$ Controlled Write)



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Note :

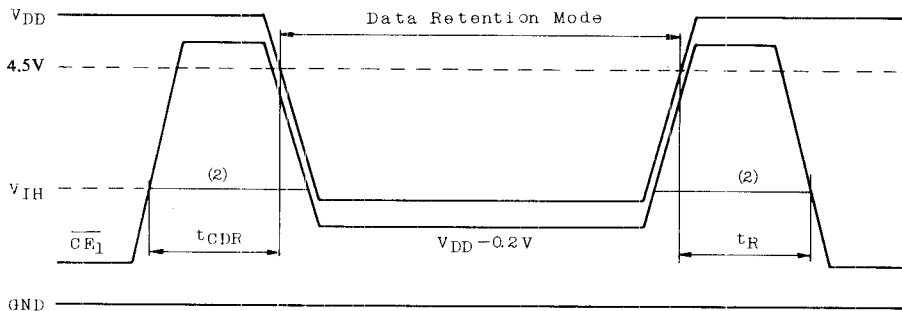
1. R/W is High for Read cycle.
2. Assuming that \overline{CE}_1 Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE}_1 High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

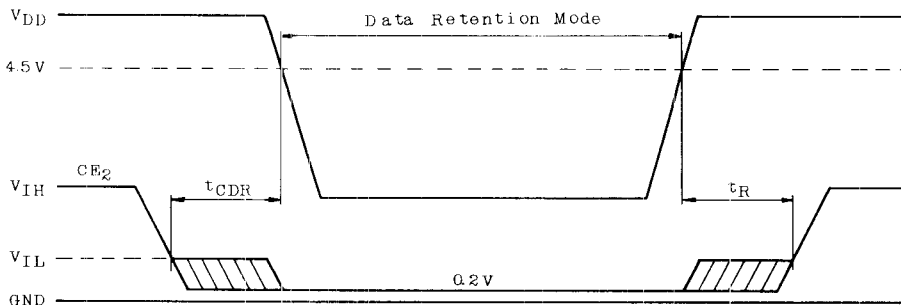
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V	
I_{DPS2}	Standby Supply Current	$V_{DD}=3.0V$	—	—	50	μA
		$V_{DD}=5.5V$	—	—	100	μA
t_{CDR}	Chip Deselection to Data Retention Mode	0	—	—	μs	
t_R	Recovery Time	t_{RC}^*	—	—	μs	

* : Read cycle time.

● \overline{CE}_1 Controlled Data Retention Mode (1)



● CE_2 Controlled Data Retention Mode (3)



Note:

1. In \overline{CE}_1 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of \overline{CE}_1 is 2.2V in operation, I_{DSD1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about $0.1\mu F$. decoupling capacitor for every device is recommended to eliminate such noise.

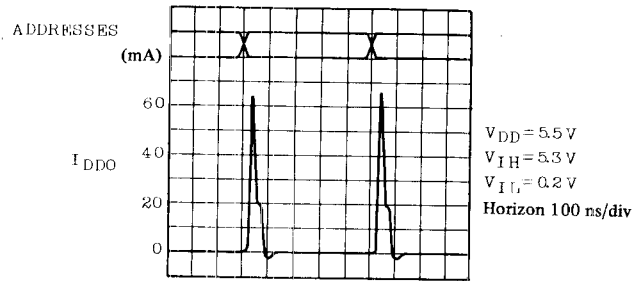
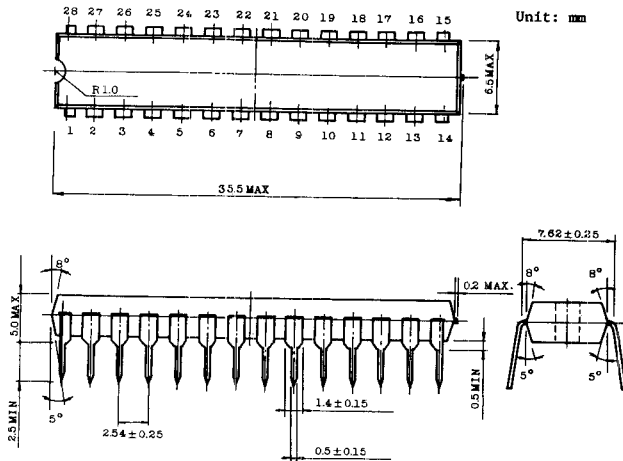


Fig. TYPICAL CURRENT WAVEFORMS

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OUTLINE DRAWINGS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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