7c198: 10/25/89
Revision: February 29, 1996

CY7C198

32K x 8 Static RAM

Features

- **High speed**
  — 15 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 990 mW
- **Low standby power**
  — 195 mW
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

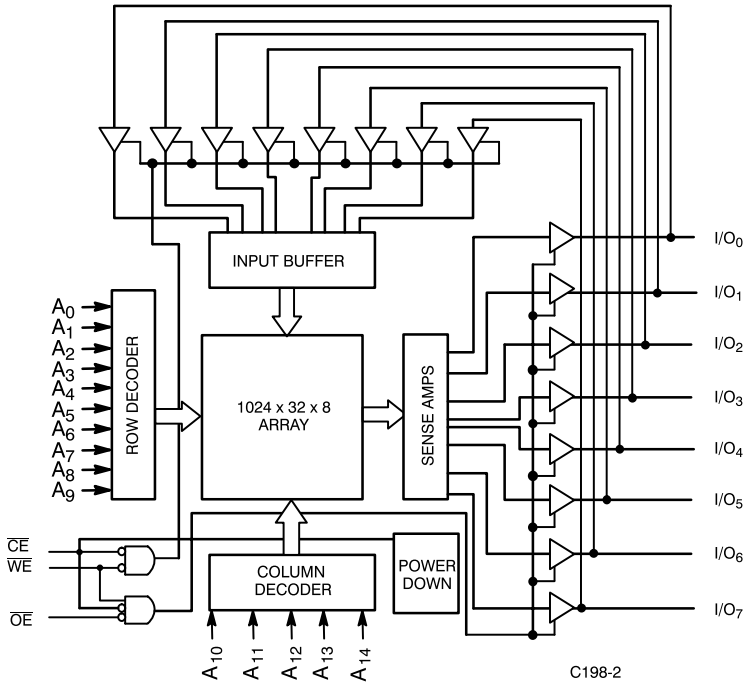
The CY7C198 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 80% when deselected. The CY7C198 is available in a 600-mil-wide cerDIP and LCC package and a 32-lead TSOP package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs areboth LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

A die coat is used to ensure alpha immunity.

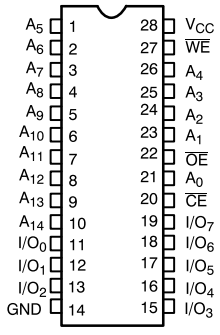
Logic Block Diagram



C198-2

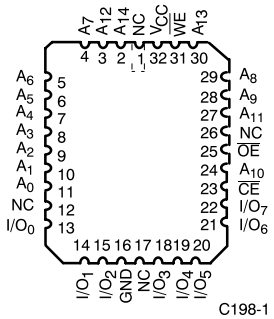
Pin Configurations

CerDIP
Top View



C198-3

LCC
Top View



C198-1

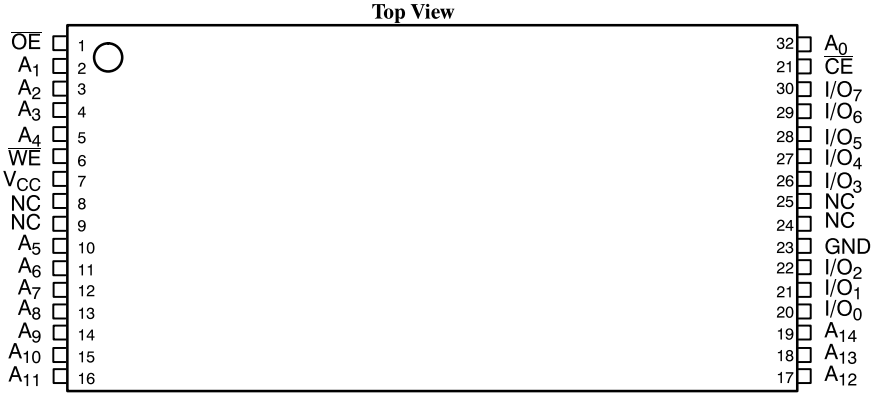
Selection Guide

		7C198−15	7C198−20	7C198−25	7C198−35	7C198−45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial		150			
	Military	180	170	150	150	150
Maximum Standby Current (mA)		30	30	30	25	25

Shaded area contains preliminary information.

Pin Configurations (continued)

TSOP
Top View



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[15] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[15] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[16]	−55°C to +125°C	5V ± 10%

Notes:
15. V_{IL} (min.) = −2.0V for pulse durations less than 20 ns.
16. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[17]

Parameter	Description	Test Conditions		7C198−15		7C198−20		7C198−25		7C198−35, 45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[15]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[18]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l				150					mA
			Mil		180		170		150		150	
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30		30		25	mA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15		15		15	mA

Shaded area contains preliminary information

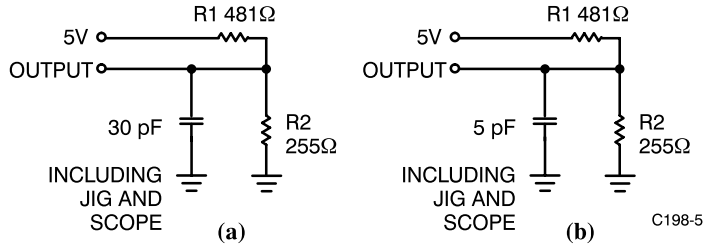
Capacitance[19]

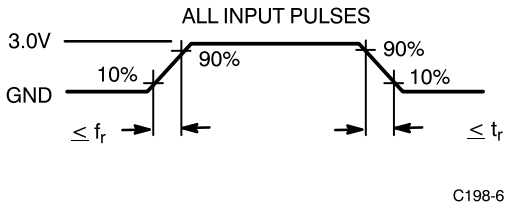
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

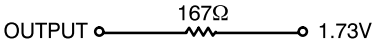
17. See the last page of this specification for Group A subgroup testing information.
18. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
19. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[20]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[17, 21]

Parameter	Description	7C198−15		7C198−20		7C198−25		7C198−35		7C198−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		9		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[22]	0		0		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[22, 23]		7		9		11		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[22]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[22, 23]		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[24, 25]												
t_{WC}	Write Cycle Time	15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		22		22		ns
t_{AW}	Address Set-Up to Write End	10		15		20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	9		15		20		22		22		ns
t_{SD}	Data Set-Up to Write End	9		10		15		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[23]		7		10		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[22]	3		3		3		3		3		ns

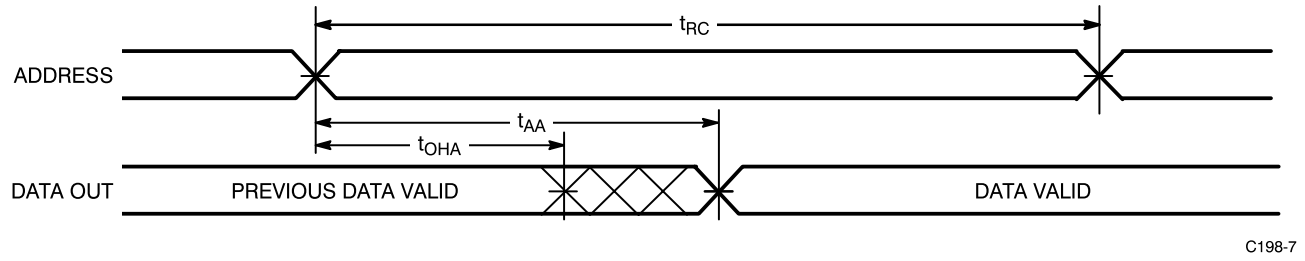
Shaded area contains preliminary information.

Notes:

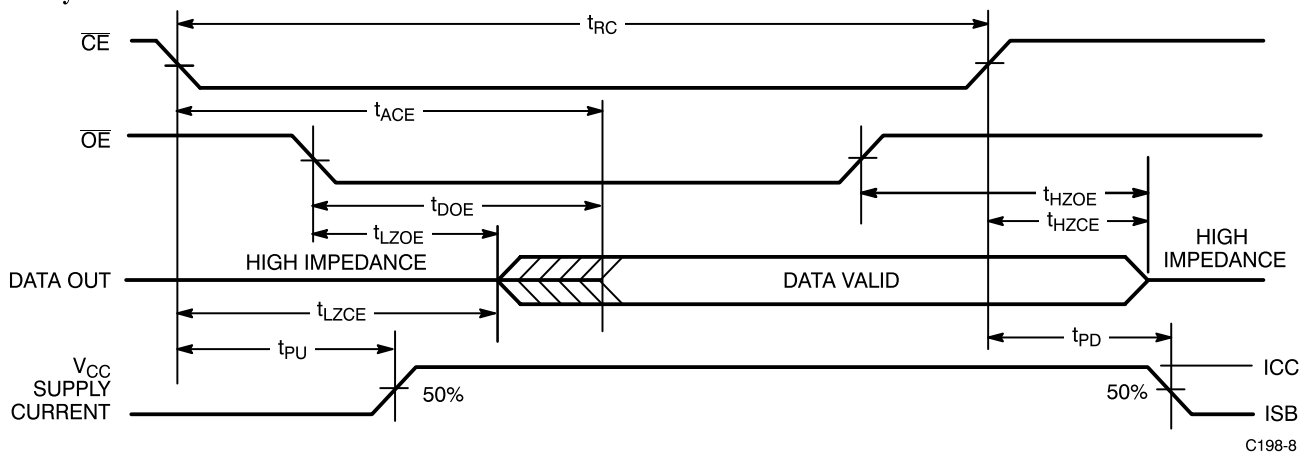
20. $t_r \geq 3$ ns for the 15-ns and 20-ns speeds, $t_r \geq 5$ ns for the 20-ns and slower speeds.
21. Test conditions assume signal transition time of 3 ns or less for the 12-ns and15-ns speeds and 5 ns for the 20-ns and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
22. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
23. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
24. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
25. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

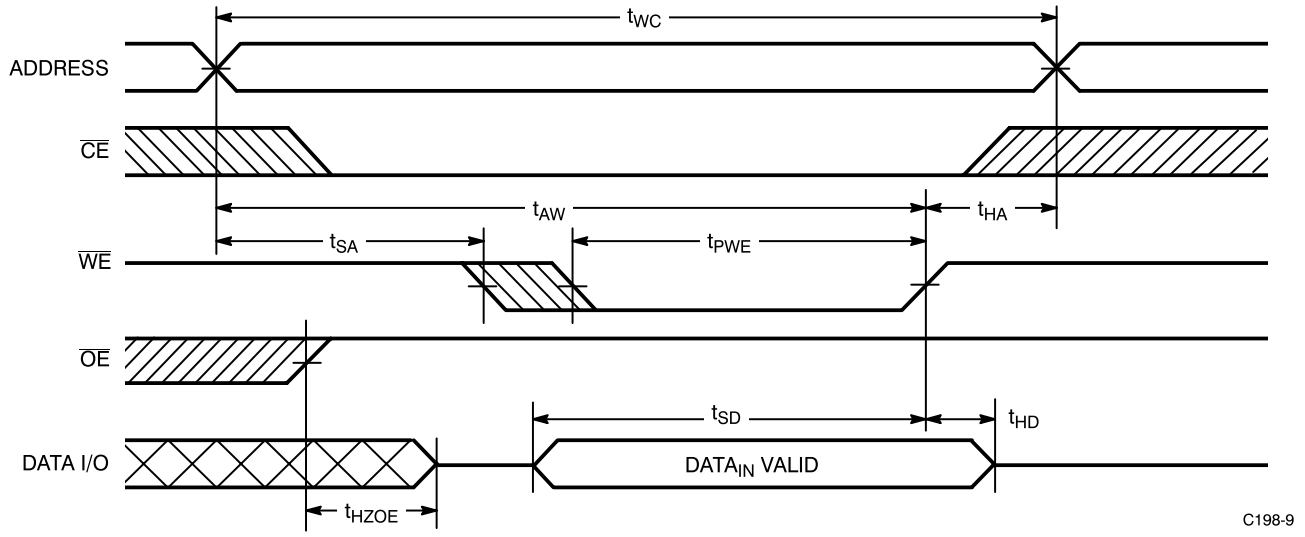
Read Cycle No. 1[26, 27]



Read Cycle No. 2[27, 28]



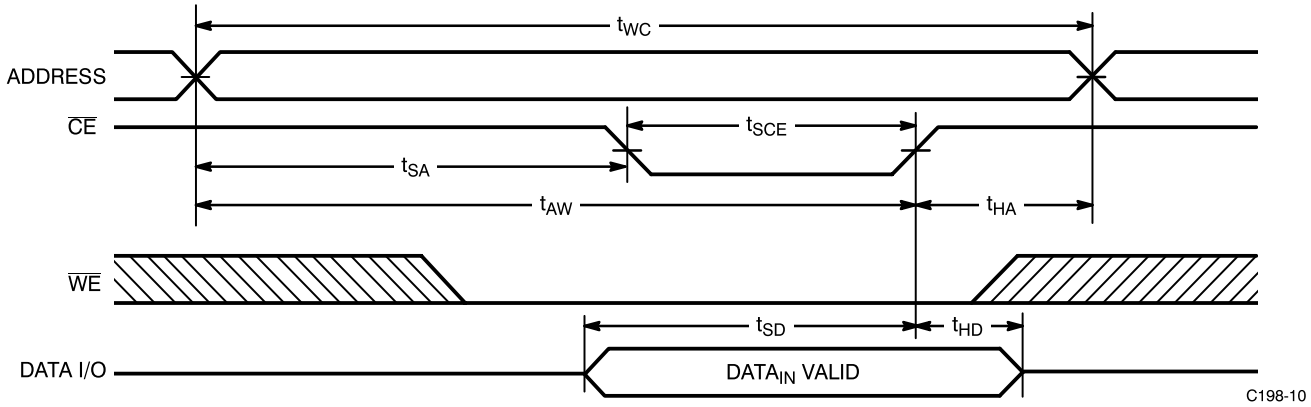
Write Cycle No. 1 ($\overline{WE}$ Controlled)[24, 29, 30]



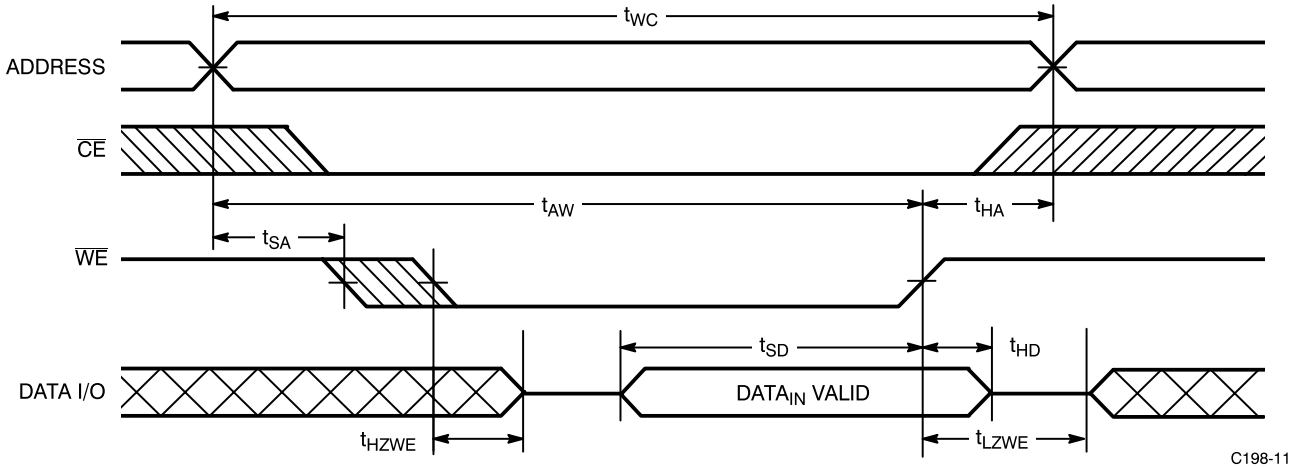
Notes:
26. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
27. $\overline{WE}$ is HIGH for read cycle.
28. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
29. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
30. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[24, 29, 30]

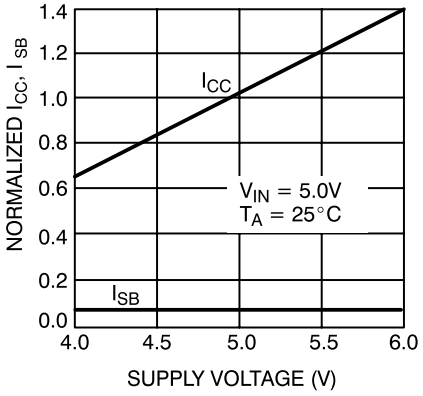


Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[25, 30]

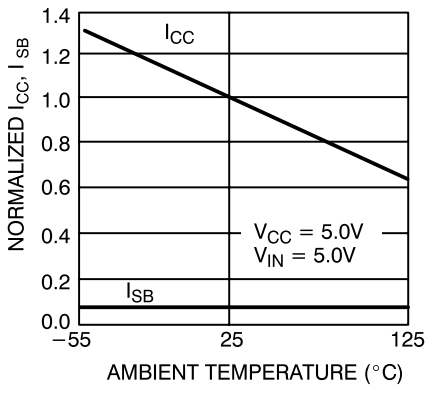


Typical DC and AC Characteristics

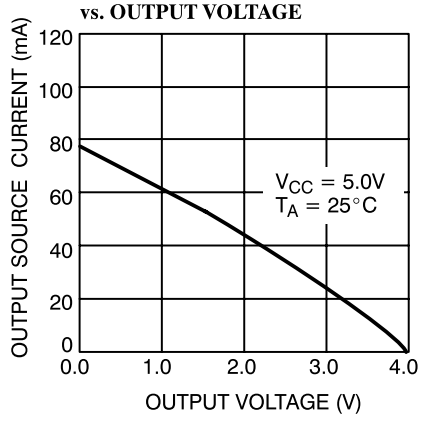
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



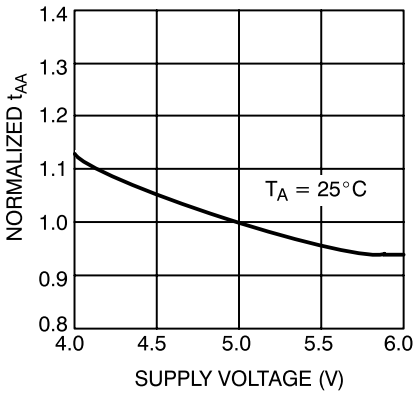
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



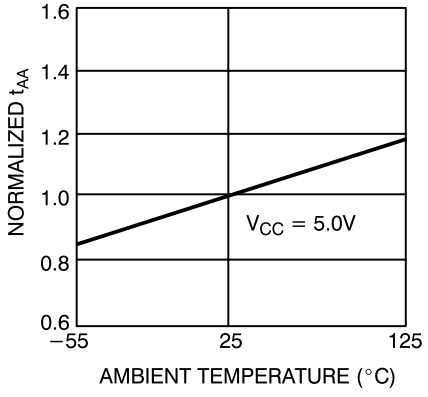
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



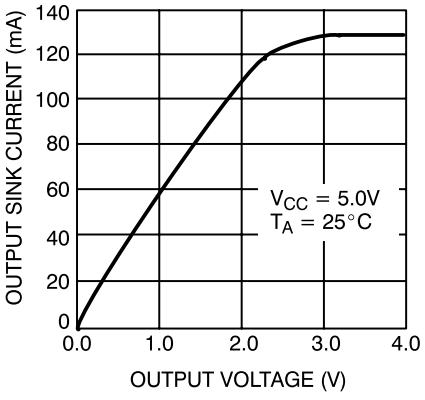
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



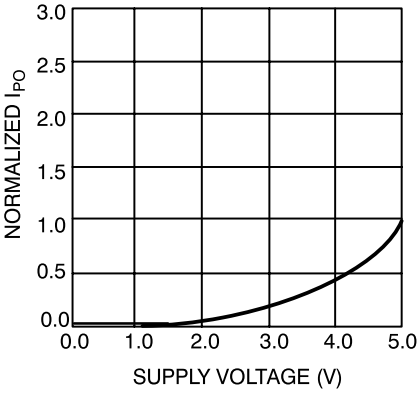
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



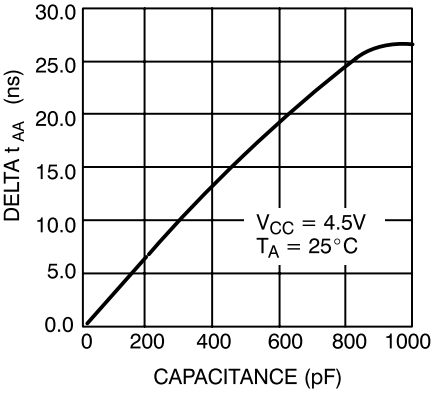
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



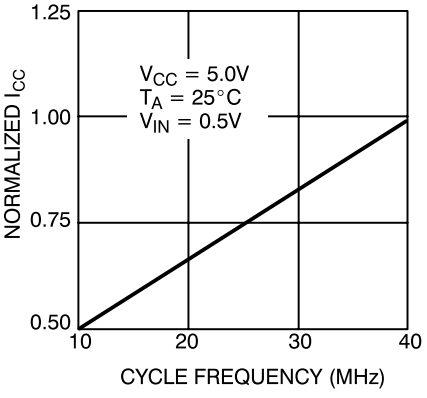
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C198−15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
20	CY7C198−20ZC	Z32	32-Lead Thin Small Outline Package	Commercial
	CY7C198−20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C198−25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C198−25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
35	CY7C198−35DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C198−35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
45	CY7C198−45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C198−45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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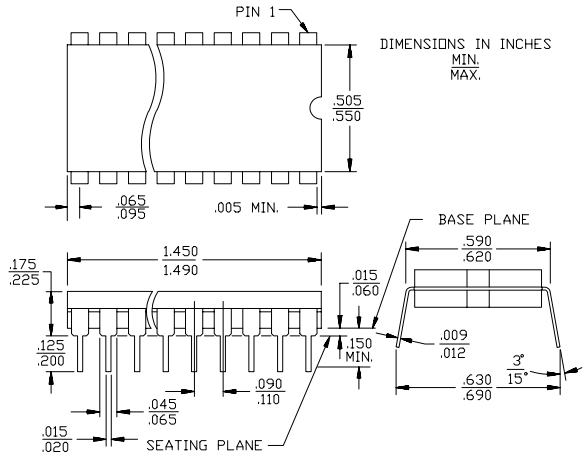
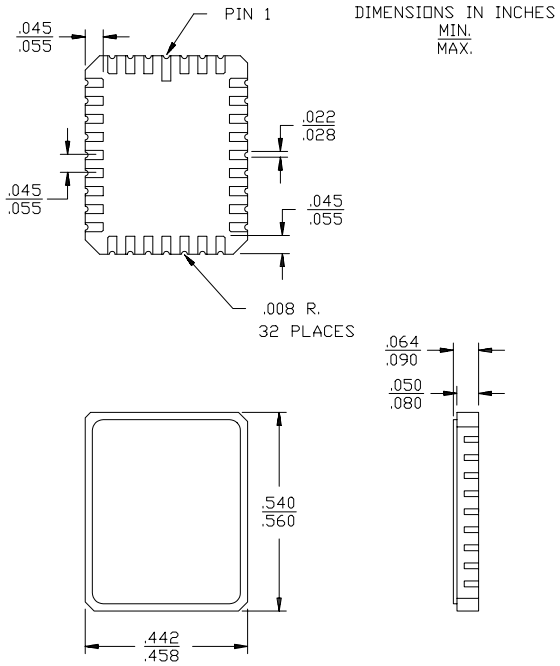
Package Diagrams

28-Lead (600-Mil) CerDIP D16
MIL−STD−1835 D−10 Config. A



32-Pin Rectangular Leadless Chip Carrier L55
MIL−STD−1835 C−12



32-Lead Thin Small Outline Package Z32