

SONY

CXK58257CTM/CYM/CM/CP -55LL/70LL

32768-word × 8-bit High Speed CMOS Static RAM *Preliminary*

Description

The CXK58257CTM/CYM/CM/CP is 262,144 bits high speed CMOS static RAM organized as 32768 words by 8 bits.

Special features are operating on a single 5V supply, low power consumption, high speed and broad package line-up.

The CXK58257CTM/CYM/CM/CP is a suitable RAM for portable equipment with battery back up.

Features

- Single +5V supply: 5V ± 10%
- Fast access time:
CXK58257CTM/CYM/CM/CP (Access time)
-55LL 55ns (Max.)
-70LL 70ns (Max.)
- Low standby current: 5µA (Max.)
- Low data retention current: 3µA (Max.)
- Direct TTL compatible: All inputs and outputs
- Data retention voltage: 2.0V (Min.)
- Broad package line-up

CXK58257CTM/CYM

8mm × 13.4mm 28 pin TSOP Package

CXK58257CM 450mil 28 pin SOP Package

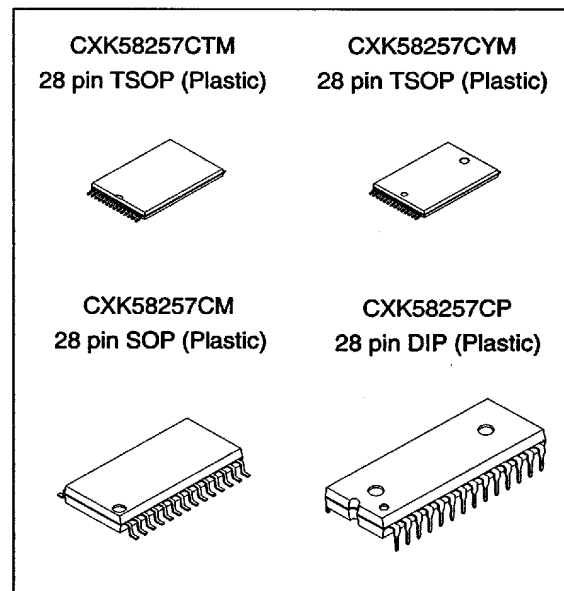
CXK58257CP 600mil 28 pin DIP Package

Function

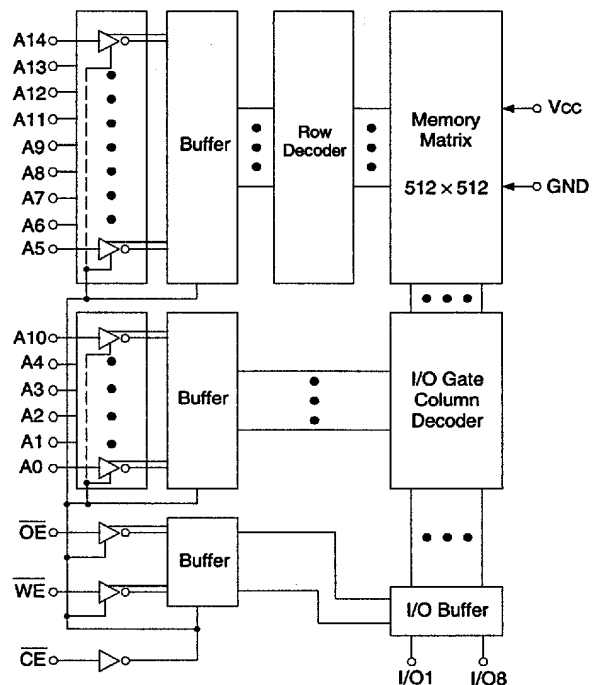
32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

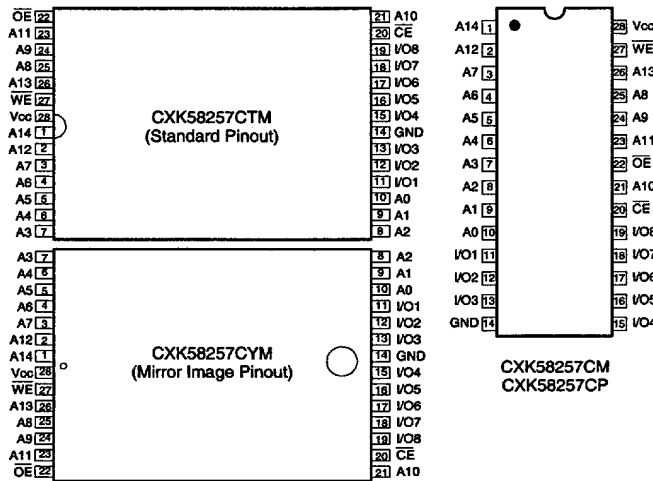


Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit	
Supply voltage	Vcc	-0.5 to +7.0	V	
Input voltage	V _{IN}	-0.5*1 to Vcc + 0.5		
Input and output voltage	V _{I/O}	-0.5*1 to Vcc + 0.5		
Allowable power dissipation	P _D	CXK58257CP	1.0	W
		CXK58257CTM/CYM/CM	0.7	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150		
Soldering temperature · time	T _{solder}	CXK58257CP	260 · 10	°C · s
		CXK58257CTM/CYM/CM	235 · 10	

*1 V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8 pin	Vcc Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	x	L	Write	Data in	I _{CC1} , I _{CC2}

x: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc + 0.3	
Input low voltage	V _{IL}	-0.3*2	—	0.8	

*2 V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*1	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}		-0.5	—	0.5	
Operation power supply current	I _{CC1}	$\overline{CE} = V_{IL}$ V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA		—	3	10	mA
Average operating current	I _{CC2}	Min. cycle duty = 100% I _{OUT} = 0mA	-55LL	—	45	70	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	0 to +70°C	—	—	5	μA
			0 to +40°C	—	—	1	
	+25°C	—	0.2	0.5			
	I _{SB2}	$\overline{CE} = V_{IH}$		—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA		2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	

*1 V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	8	

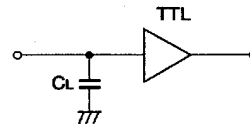
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions	
Input pulse high level	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.8V	
Input rise time	t _r = 5ns	
Input fall time	t _f = 5ns	
Input and output reference level	1.5V	
Output load conditions	-55LL	C _L *2 = 30pF, 1TTL
	-70LL	C _L *2 = 100pF, 1TTL



*2 C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-55LL		-70LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	55	—	70	—	ns
Address access time	t_{AA}	—	55	—	70	
Chip enable access time	t_{CO}	—	55	—	70	
Output enable to output valid	t_{OE}	—	30	—	40	
Output hold from address change	t_{OH}	15	—	20	—	
Chip enable to output in low Z (\overline{CE})	t_{LZ}	10	—	10	—	
Output enable to output in low Z (\overline{OE})	t_{OLZ}	5	—	5	—	
Chip disable to output in high Z (\overline{CE})	t_{HZ}^{*1}	—	20	—	25	
Output disable to output in high Z (\overline{OE})	t_{OHZ}^{*1}	—	20	—	25	

*1 t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

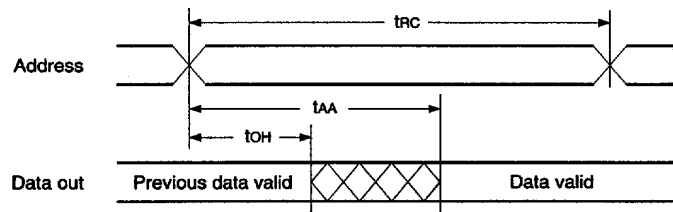
• Write cycle

Item	Symbol	-55LL		-70LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	55	—	70	—	ns
Address valid to end of write	t_{AW}	50	—	60	—	
Chip enable to end of write	t_{CW}	50	—	60	—	
Data to write time overlap	t_{DW}	25	—	30	—	
Data hold from write time	t_{DH}	0	—	0	—	
Write pulse width	t_{WP}	40	—	50	—	
Address setup time	t_{AS}	0	—	0	—	
Write recovery time (\overline{WE})	t_{WR}	0	—	0	—	
Write recovery time (\overline{CE})	t_{WR1}	0	—	0	—	
Output active from end of write	t_{OW}	10	—	10	—	
Write to output in high Z	t_{WHZ}^{*2}	—	20	—	25	

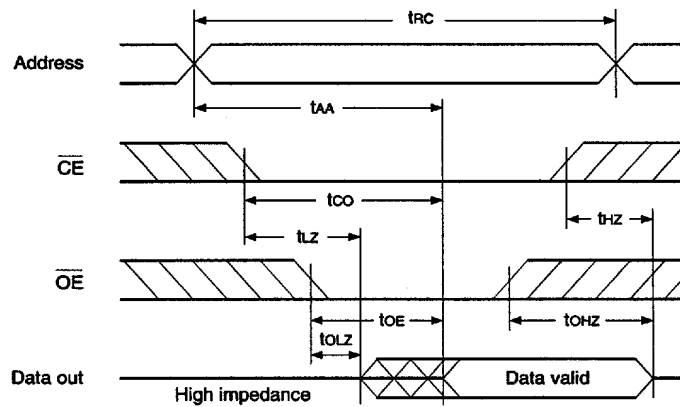
*2 t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

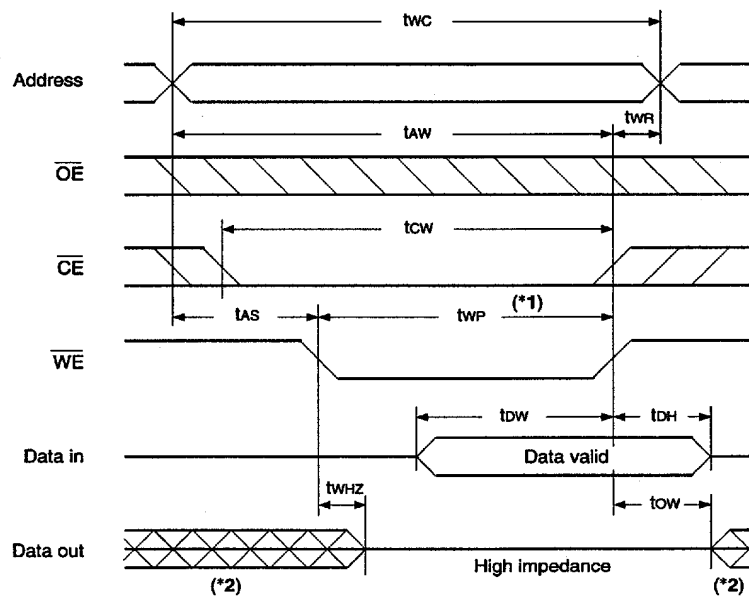
- Read cycle (1): $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$



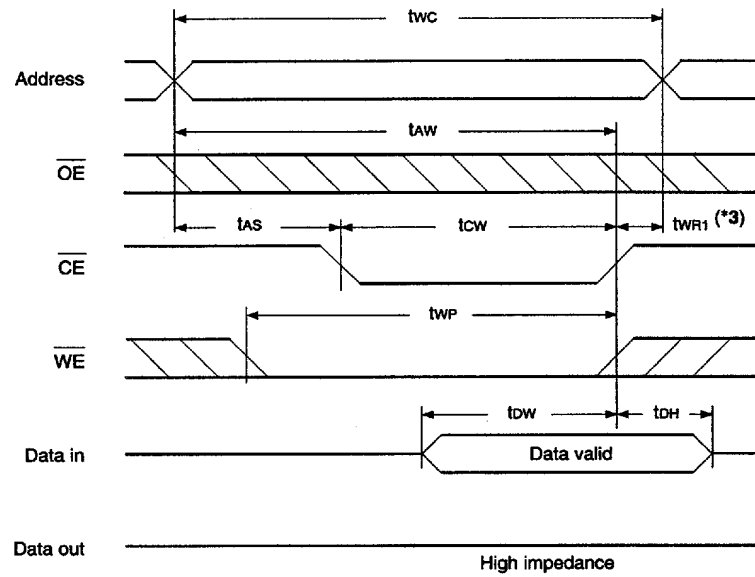
- Read cycle (2): $\overline{WE} = V_{IH}$



- Write cycle (1): \overline{WE} control



• Write cycle (2): \overline{CE} control



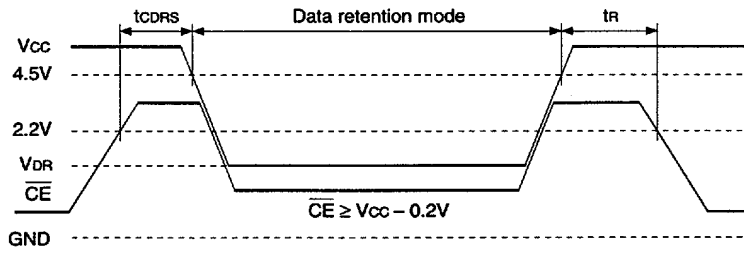
*1 Write is executed when both \overline{CE} and \overline{WE} are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} is tested from the rising edge of \overline{CE} , until the end of the write cycle.

Data retention waveform

- Low supply voltage data retention waveform



Data Retention Characteristics

(Ta = 0 to +70°C)

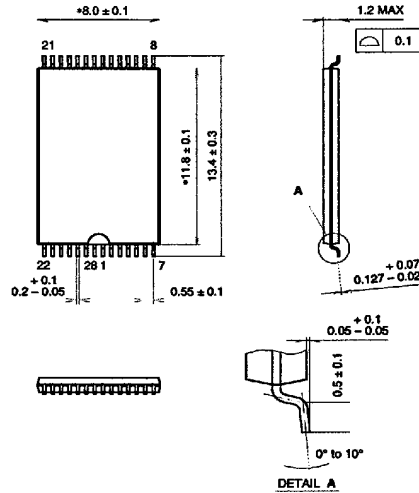
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	V	
Data retention current	I _{CCDR1}	V _{CC} = 3.0V CE ≥ 2.8V	0 to +70°C	—	—	3	μA
			0 to +40°C	—	—	0.6	
			+25°C	—	0.1	0.3	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V CE ≥ V _{CC} - 0.2V	—	0.2*1	5		
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t _R		5	—	—	ms	

*1 V_{CC} = 5V, Ta = 25°C

Package Outline Unit: mm

CXK58257CTM

28PIN TSOP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

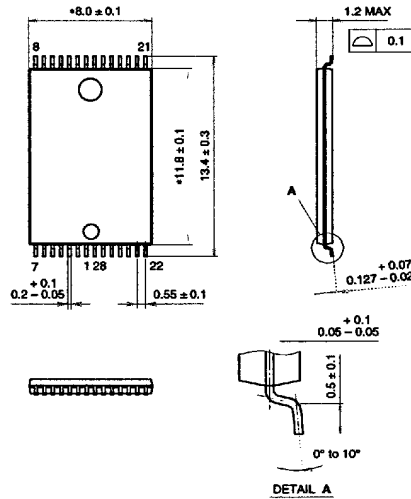
PACKAGE STRUCTURE

SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK58257CYM

28PIN TSOP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

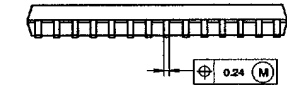
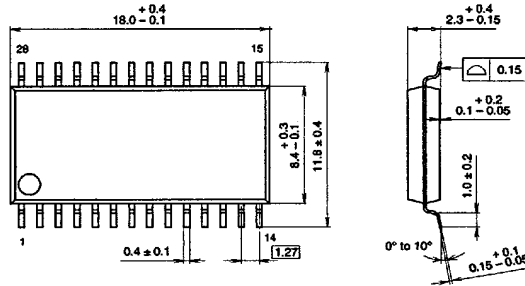
PACKAGE STRUCTURE

SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK58257CM

28PIN SOP (PLASTIC)



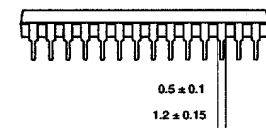
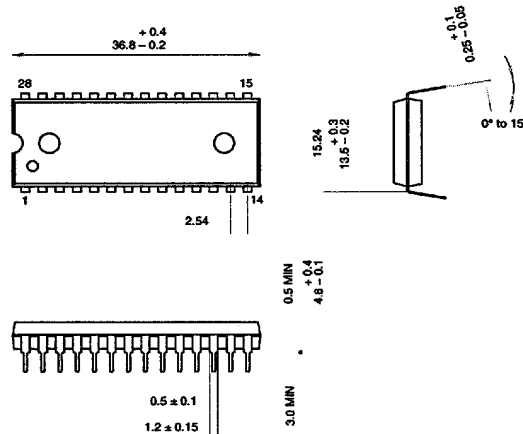
SONY CODE	SOP-28P-L05
EIAJ CODE	*SOP028-P-0450
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g

CXK58257CP

28PIN DIP (PLASTIC) 600mil



SONY CODE	DIP-28P-04
EIAJ CODE	*DIP028-P-0600-D
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.2g