SONY CXK58258BP/BJ/BM* -20L*/25L/35L -20LL*/25LL/35LL

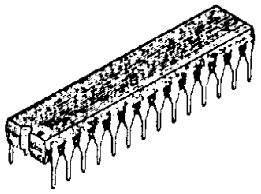
32,768-word × 8-bit High Speed CMOS Static RAM * under development

Description

The CXK58258BP/BJ/BM is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 20/25/35ns access time from 5V single power supply.

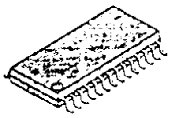
This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

CXK58258BP
28 pin DIP (Plastic)



CXK58258BJ
28 pin SOJ (Plastic)

CXK58258BM
28 pin SOP (Plastic)



Features

- Fast access time (Access time)

CXK58258BP/BJ/BM-20L, 20LL	20ns (Max.)
CXK58258BP/BJ/BM-25L, 25LL	25ns (Max.)
CXK58258BP/BJ/BM-35L, 35LL	35ns (Max.)

- Low power operation

	Standby (Max.)	Operation (Typ., Min. Cycle)
CXK58258BP/BJ/BM-20LL	5 µW	400mW
CXK58258BP/BJ/BM-25LL	5 µW	350mW
CXK58258BP/BJ/BM-35LL	5 µW	300mW
CXK58258BP/BJ/BM-20L	10 µW	400mW
CXK58258BP/BJ/BM-25L	10 µW	350mW
CXK58258BP/BJ/BM-35L	10 µW	300mW

- Single +5V power supply: 5V ± 10%
- Fully static memory···No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output:three state output
- Available in 28 pin 300mil DIP, 300mil SOJ, 450mil SOP package.

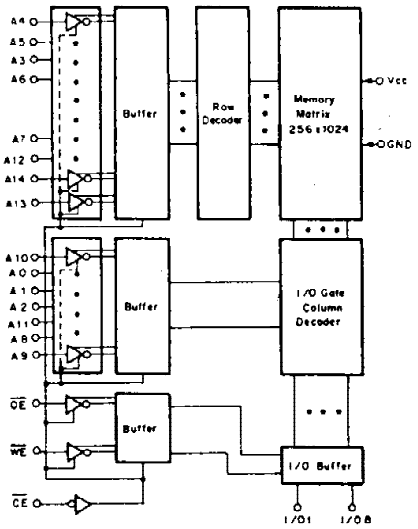
Function

32,768-word × 8-bit static RAM

Structure

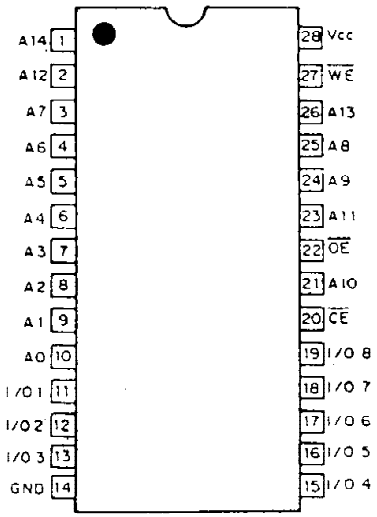
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

E90268A19 - ST

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5 * to +7.0	V
Input voltage	V_{IN}		−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	CXK58258BP/BJ	1.0	W
		CXK58258BM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature • time	Tsolder		260 • 10	°C • sec

* Vcc, V_{IN}, $V_{I/O}$= −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}= −3.0V Min. for pulse width less than 20ns.

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Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		-1	—	1	-1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$=GND to Vcc, $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}		-1	—	1	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		—	—	—	—	—	—	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100%, I_{OUT}=0mA, $\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}	-20L/20LL	—	80	120	—	80	120	mA
			-25L/25LL	—	70	120	—	70	120	
			-35L/35LL	—	60	100	—	60	100	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc-0.2V		—	0.002	0.1	—	0.001	0.05	mA
	I_{SB2}	Cycle=Min, Duty=100%, $\overline{CE}$=V_{IH}		—	1.5	5	—	1.5	5	mA
Output high voltage	V_{OH}	I_{OH}= -4.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

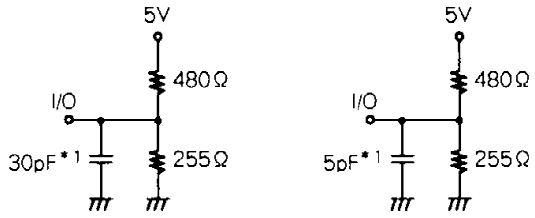
AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=3ns
Input fall time	tf=3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) **Output Load (2)** *2



*1 including scope and jig capacitance
*2 for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip enable access time	t_{CC}	—	20	—	25	—	35	ns
Output enable to output valid	t_{OE}	—	10	—	12	—	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ} *	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ} *	—	9	—	10	—	15	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	8	—	9	—	12	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	35	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

• Write cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Address valid to end of write	t_{AW}	13	—	15	—	20	—	ns
Chip enable to end of write	t_{CW}	14	—	16	—	20	—	ns
Data to write time overlap	t_{DW}	11	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	13	—	15	—	20	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ} *	—	9	—	10	—	12	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

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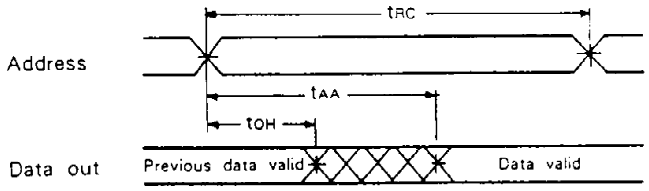
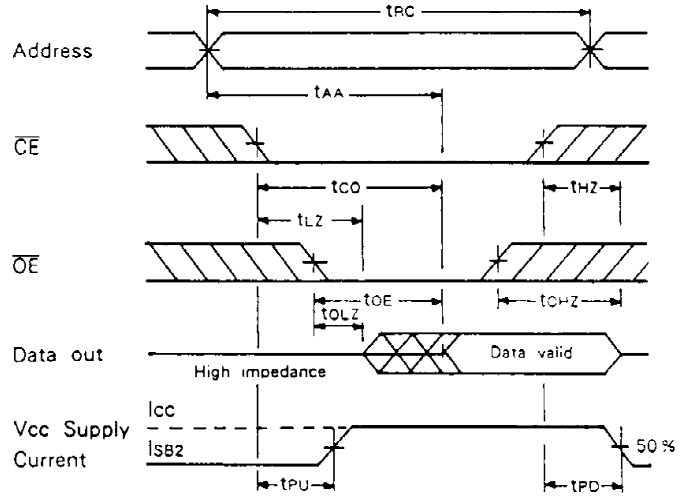
Timing Waveform

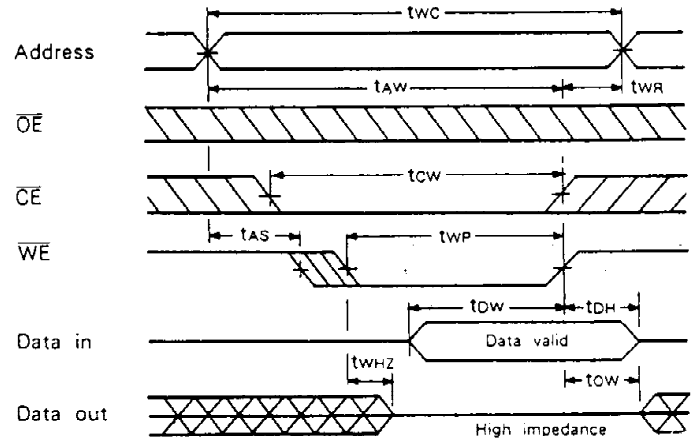
• Read cycle (1): $\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}



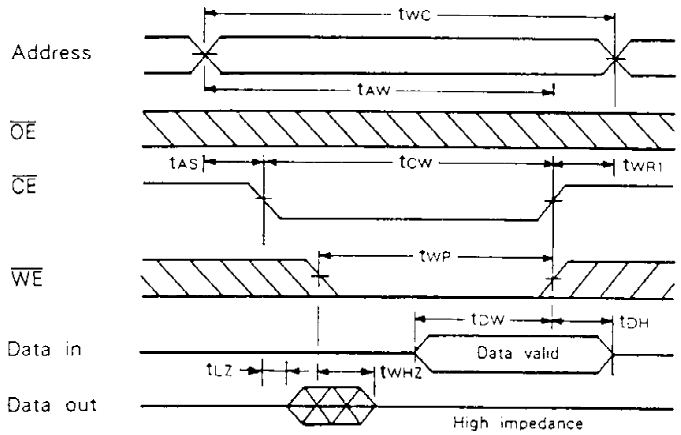
• Read cycle (2): $\overline{WE}$=V_{IH}



• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE}$ control



Note)

1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

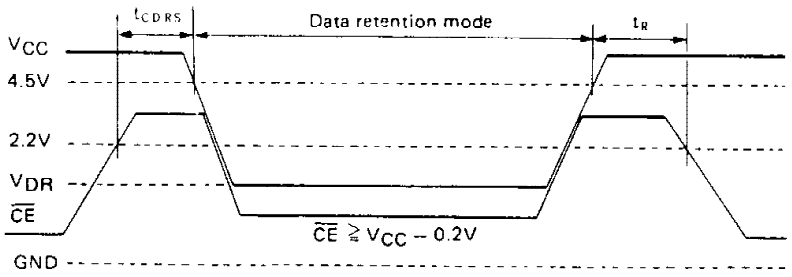
Data Retention Characteristics

(Ta=0 to +70°C)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V $\overline{CE} \geqq 2.8V$	Ta=0 to 70°C	—	—	50	—	—	10	μA
			Ta=0 to 40°C	—	—	10	—	—	4	
			25°C	—	1	3	—	0.5	1	
	I_{CCDR2}	Vcc=2.0 to 5.5V $\overline{CE} \geqq V_{CC}-0.2V$		—	0.002	0.1	—	0.001	0.05	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC} *	—	—	t_{RC} *	—	—	ns

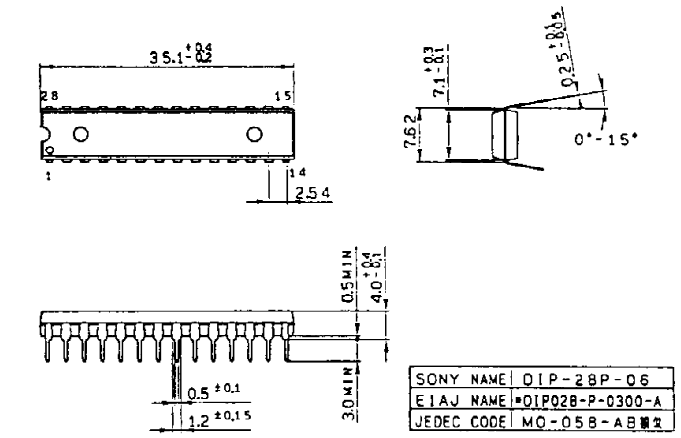
* t_{RC}: Read cycle time

Data retention time

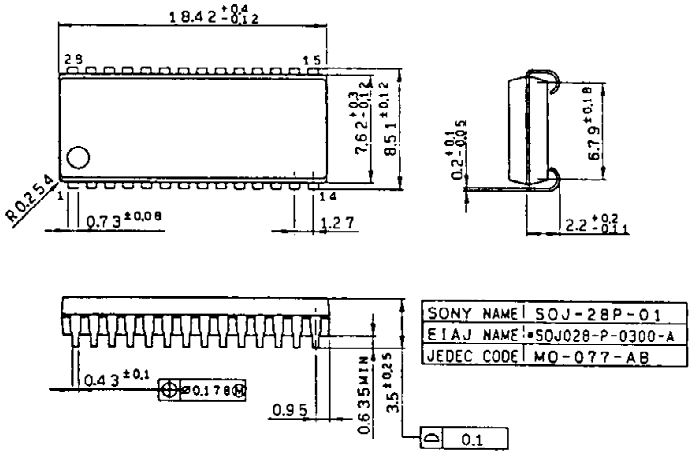


Package Outline Unit : mm

CXK58258BP 28pin DIP (Plastic) 300mil 2.0g



CXK58258BJ 28pin SOJ (Plastic) 300mil 0.8g



CXK58258BM 28pin SOP (Plastic) 450mil 0.7g