DESCRIPTION

The HY6264A is a high-speed, low power and 8,192x8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns. The HY6264A has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltage from 2.0 to 5.5 volt has little effect on supply current in the data retention mode. Reducing the supply voltage to minimize current drain is unnecessary for the HY6264A Series.

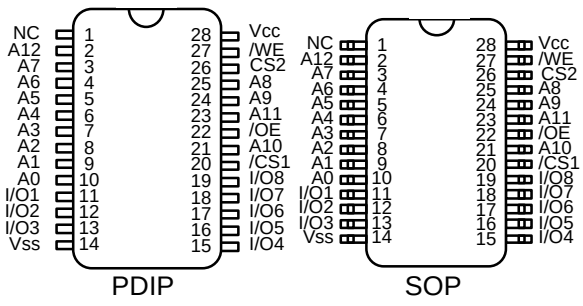
FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  -2.0V(min.) data retention
- Standard pin configuration
  -28 pin 600 mil PDIP
  -28 pin 330 mil SOP

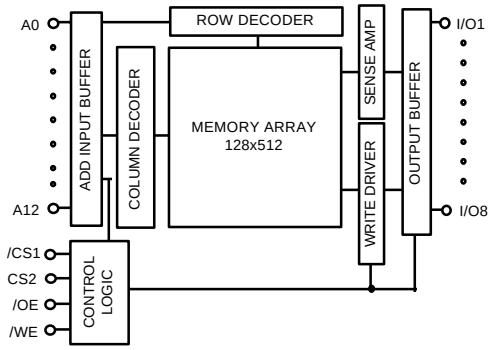
Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (°C)
					L	LL	
HY6264A	5.0	70/85/100	50	1mA	100	10	0~70(Normal)

Note 1. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select 1	I/O1-I/O8	Data Input/Output
CS2	Chip Select 2	Vcc	Power(+5V)
/WE	Write Enable	Vss	Ground
/OE	Output Enable	NC	No Connect
A0-A12	Address Inputs		

ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY6264AP	70/85/100		PDIP
HY6264ALP	70/85/100	L-part	PDIP
HY6264ALLP	70/85/100	LL-part	PDIP
HY6264AJ	70/85/100		SOP
HY6264ALJ	70/85/100	L-part	SOP
HY6264ALLJ	70/85/100	LL-part	SOP

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 125	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 •10	°C•sec

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for an extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

T_A=0°C TO 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note
1. V_{IL} = -3.0V for pulse width less than 50ns

TRUTH TABLE

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION
H	X	X	X	Standby	High-Z
X	L	X	X		High-Z
L	H	H	H	Output Disabled	High-Z
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In

Note
1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V±10%, T_A = 0°C to 70°C (Normal) unless otherwise specified

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc /CS1=V_{IH} or CS2=V_{IL} or /OE = V_{IH} or/ WE = V_{IL}		-1	-	1	uA
Icc	Operating Power Supply Current	/CS1 = V_{IL}, CS2=V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	30	50	mA
I_{CC1}	Average Operating Current	/CS1 = V_{IL}, CS2=V_{IH} Min. Duty Cycle = 100%, $I_{I/O}$ = 0mA		-	30	50	mA
I_{SB}	TTL Standby Current (TTL Input)	/CS1 = V_{IH} or CS2=V_{IL}		-	0.4	2	mA
I_{SB1}	CMOS Standby Current (CMOS Input)	/CS1 ≥ Vcc - 0.2V,		-	-	1	mA
		CS2 ≤0.2V,or	L	-	2	100	uA
		CS2 ≥Vcc-0.2V	LL	-	1	10	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA		2.4	-	-	V

Note : Typical values are at Vcc = 5.0V, T_A = 25°C

AC CHARACTERISTICS

Vcc = 5.0V±10%, T_A = 0°C to 70°C (Normal), unless otherwise noted

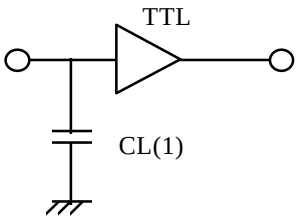
#	Symbol	Parameter	-70		-85		-10		Unit
			Min	Max	Min	Max	Min	Max	
	READ CYCLE								
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	55	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Outputin Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	35	0	35	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	35	0	35	ns
9	tOH	Output Hold from Address Change	5	-	5	-	10	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	70	-	85	-	100	-	ns
11	tCW	Chip Selection to End of Write	55	-	60	-	70	-	ns
12	tAW	Address Valid to End of Write	55	-	60	-	70	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	55	-	60	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	30	0	35	0	35	ns
17	tDW	Data to Write Time Overlap	35	-	35	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal), unless otherwise specified.

PARAMETER	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

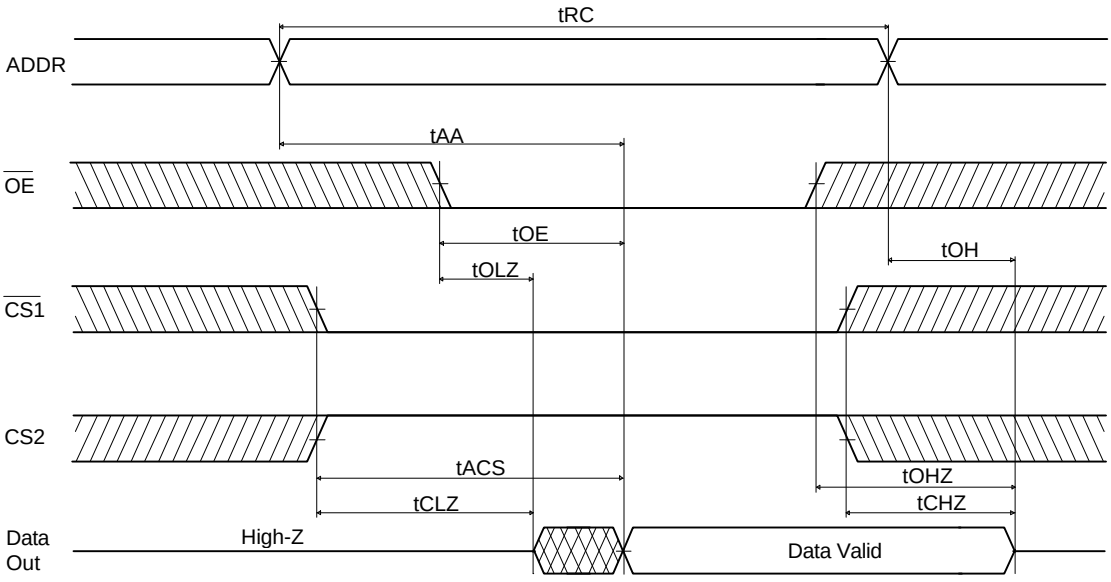
Temp = 25°C, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameter are sampled and not 100% tested

TIMING DIAGRAM

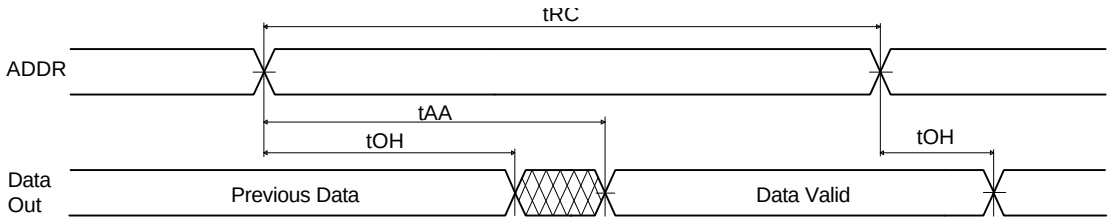
READ CYCLE 1(Note 1)



Note(READ CYCLE):

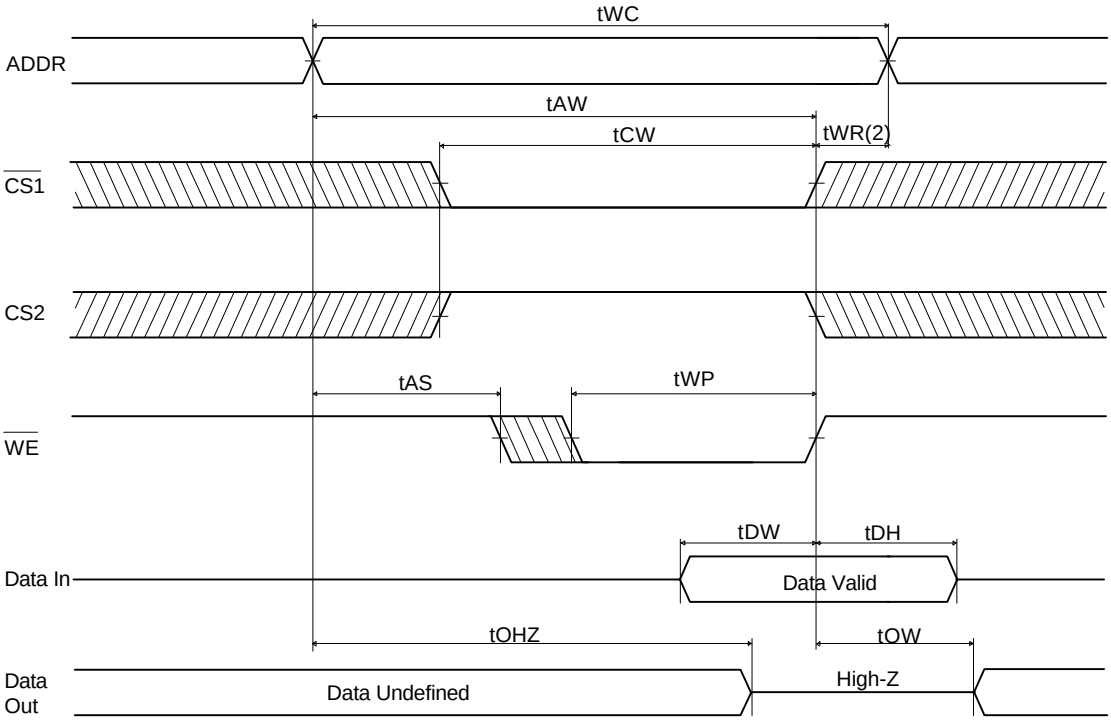
1.t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2.At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3./WE is high for the read cycle.

READ CYCLE 2(Note 1,2,3)

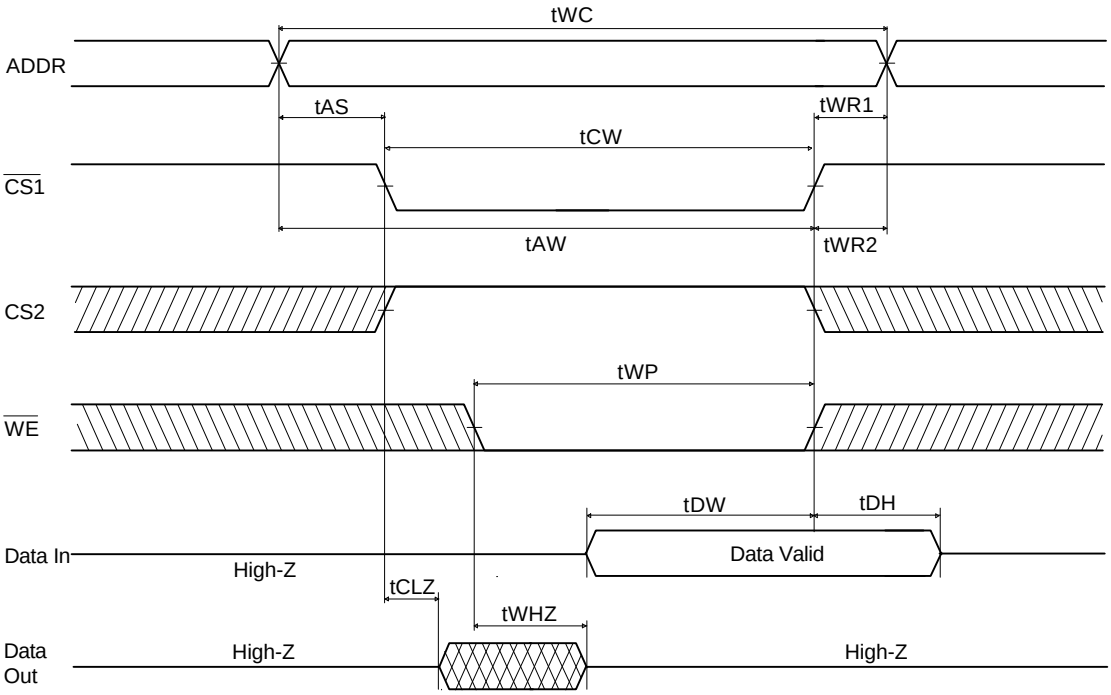


Note(Read Cycle)
1./WE is high for the read cycle.
2.Device is continuously selected /CS=V_{IL}, CS2=V_{IH}.
3./OE=V_{IL}.

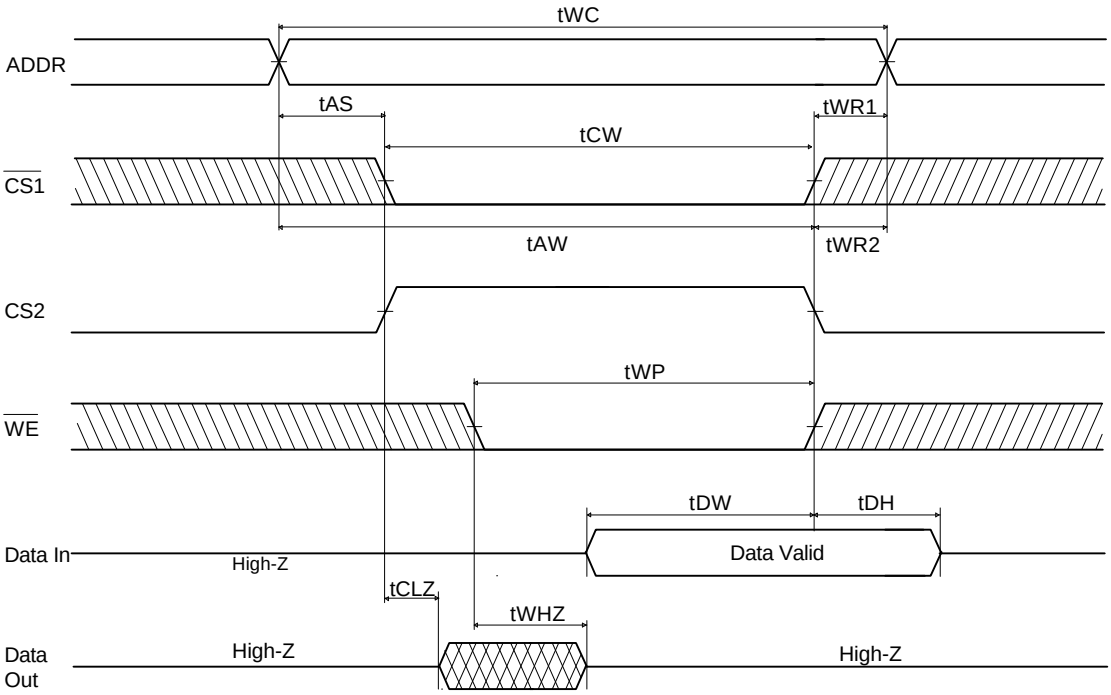
WRITE CYCLE 1(/WE Controlled)



WRITE CYCLE 2 (/CS1Controlled)



WRITE CYCLE 3 (CS2 Controlled)



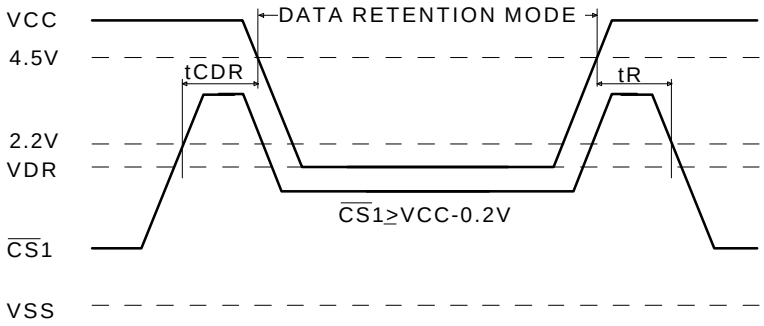
Notes(Write Cycle):
1. A write occurs during the overlap of a low /CS1 and high CS2 and a low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 going low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 is applied in case a write ends as /CS1, or /WE going high, and tWR2 is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.
7. DOUT is the read data of the new address.
8. When /CS1 is low and CS2 is high,I /O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION CHARACTERISTICS.

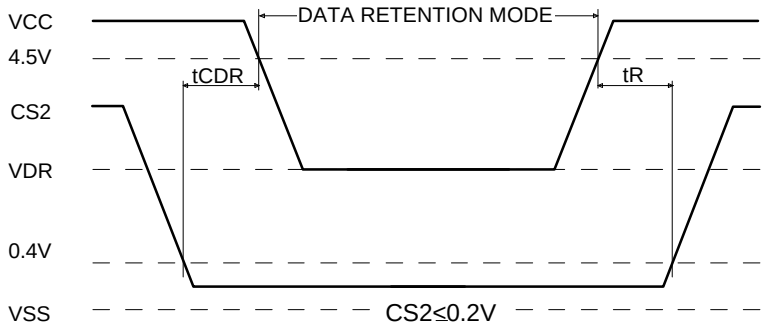
Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
VDR	Vcc for Data Retention	/CS1≥Vcc-0.2V, CS2≥0.2V or≥Vcc-0.2V, Vss≤VIN≤Vcc		2	-	-	V
ICCDR	Data Retention Current	Vcc = 3.0V, /CS1≥Vcc-0.2V CS2≤0.2V or ≥Vcc-0.2V Vss≤VIN≤Vcc	L	-	1	50	uA
			LL	-	1	5	uA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC(2)	-	-	ns

Note
1.Typical values are under the condition of TA=25°C.
2.tRC is read cycle time

DATA RETENTION TIMING DIAGRAM 1



DATA RETENTION TIMING DIAGRAM 2

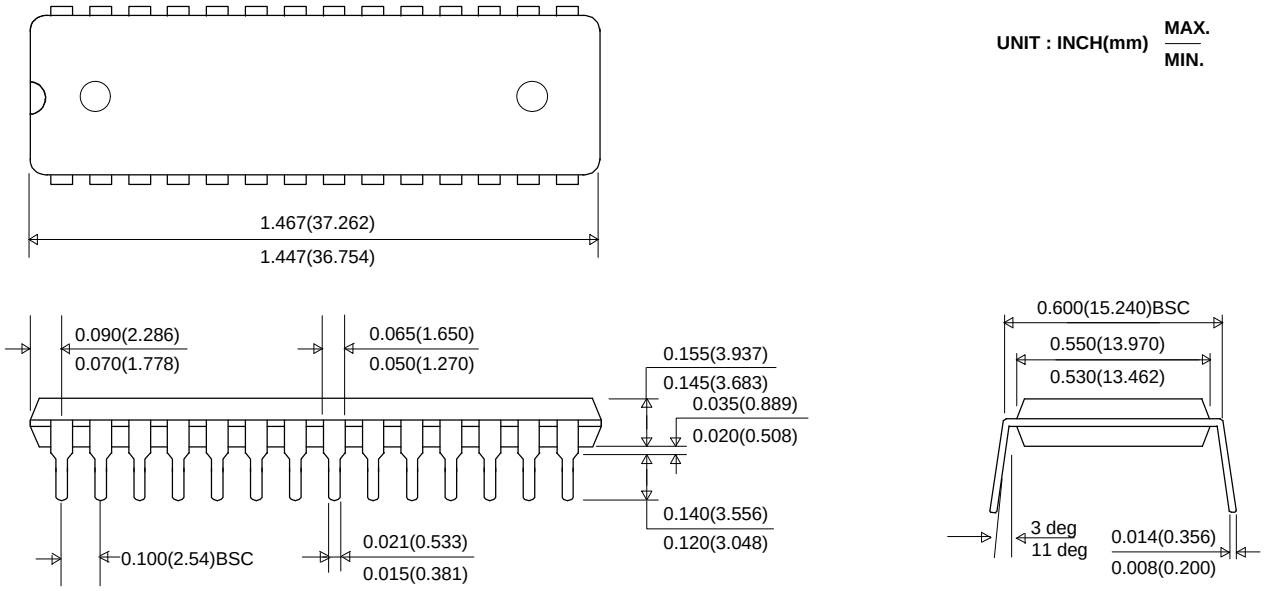


RELIABILITY SPEC.

TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥100mA

PACKAGE INFORMATION

28pin 600mil Dual In-Line Package(P)



28pin 330mil Small Outline Package(J)