

SONY®

# CXK5864CP/CM -70LL/10LL

8,192-word × 8-bit High Speed CMOS Static RAM

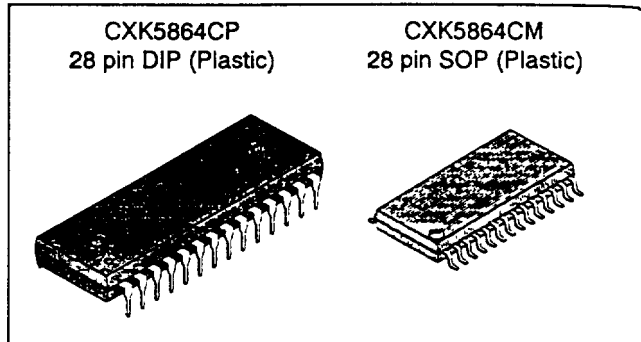
205-760

## Description

CXK5864CP/CM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

## Features

- Fast access time: (Access time)  
 CXK5864CP/CM-70LL 70ns (Max.)  
 CXK5864CP/CM-10LL 100ns (Max.)
- Low power operation:  
 CXK5864CP/CM-70LL, 10LL;  
 Standby/Operation: 1 μW (Typ.) /15mW (Typ.)
- Single power supply 5V: +5V ± 10%
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP and 450mil SOP



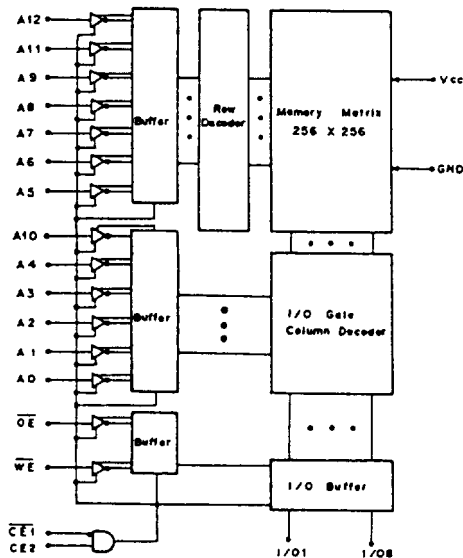
## Function

8,192-word × 8-bit static RAM

## Structure

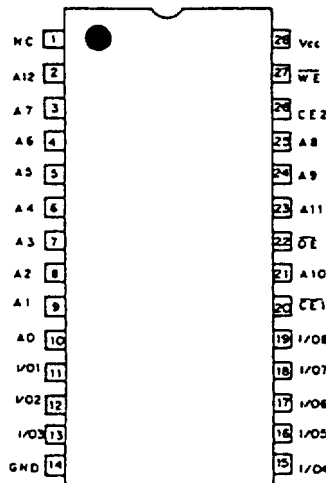
Silicon gate CMOS IC

## Block Diagram



## Pin Configuration

(Top View)



## Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

## Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 * to V <sub>CC</sub> +0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5 * to V <sub>CC</sub> +0.5	V
Allowable power dissipation	P <sub>D</sub>	CXK5864CP	1.0
		CXK5864CM	0.7
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature • time	T <sub>solder</sub>	260 • 10	°C • sec

\* V<sub>IN</sub>, V<sub>I/O</sub>=-3.0V Min. for pulse width less than 50ns.

## Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V <sub>CC</sub> Current
H	X	X	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
X	L	X	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub>
L	H	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub>
L	H	X	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub>

X : "H" or "L"

## DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	-0.3 *	—	0.8	V

\* V<sub>IL</sub>=-3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

**• DC and operating characteristics**

(V<sub>CC</sub>=5V ± 10%, GND=0V, T<sub>a</sub>=0 to +70 °C)

Item	Symbol	Test conditions	- 70LL/10LL			Unit
			Min.	Typ. *	Max.	
Input leak current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	-500	—	500	nA
Output leak current	I <sub>LO</sub>	V <sub>I/O</sub> =GND to V <sub>CC</sub> $\overline{CE1}=V_{IH}$ or CE2=V <sub>IL</sub> or $\overline{OE}=V_{IH}$ or WE=V <sub>IL</sub>	-500	—	500	nA
Operating supply current	I <sub>CC1</sub>	$\overline{CE1}=V_{IL}$ , CE2=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	—	3	10	mA
Average operating current	I <sub>CC2</sub>	Min. cycle Duty=100%, I <sub>OUT</sub> =0mA	—	30	50	mA
Standby current	I <sub>SB1</sub>	CE2 ≤ 0.2V or { CE1 ≥ V <sub>CC</sub> -0.2V CE2 ≥ V <sub>CC</sub> -0.2V	—	0.2	6	μA
	I <sub>SB2</sub>	$\overline{CE1}=V_{IH}$ or CE2=V <sub>IL</sub>	—	0.4	2	mA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	—	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	V

\* V<sub>CC</sub>=5V, T<sub>a</sub>=25 °C

**Pin capacitance**

(T<sub>a</sub>=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	—	8	pF
Input/Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	—	6	pF

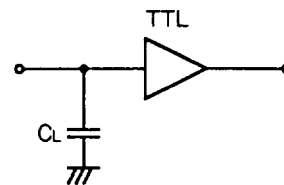
**Note)** This parameter is sampled and is not 100% tested.

**AC characteristics**

**• AC test conditions** (V<sub>CC</sub>=5V ± 10%, T<sub>a</sub>=0 to +70 °C)

Item	Conditions	
Input pulse high level	V <sub>IH</sub> =2.2V	
Input pulse low level	V <sub>IL</sub> =0.8V	
Input rise time	t <sub>r</sub> =5ns	
Input fall time	t <sub>f</sub> =5ns	
Input and output reference level	1.5V	
Output load conditions	10LL	C <sub>L</sub> * =100pF, 1TTL
	70LL	C <sub>L</sub> * =30pF, 1TTL

\* C<sub>L</sub> includes scope and jig capacitances.



## ● Read cycle

Item	Symbol	-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>rc</sub>	70	—	100	—	ns
Address access time	t <sub>AA</sub>	—	70	—	100	ns
Chip enable access time ( $\overline{CE1}$ , CE2)	t <sub>CO1</sub> t <sub>CO2</sub>	—	70	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	35	—	50	ns
Output hold from address change	t <sub>OH</sub>	15	—	15	—	ns
Chip enable to output in low Z ( $\overline{CE1}$ , CE2)	t <sub>LZ1</sub> t <sub>LZ2</sub>	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t <sub>HZ1</sub> * t <sub>HZ2</sub> *	0	30	0	35	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	0	30	0	35	ns

\* t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

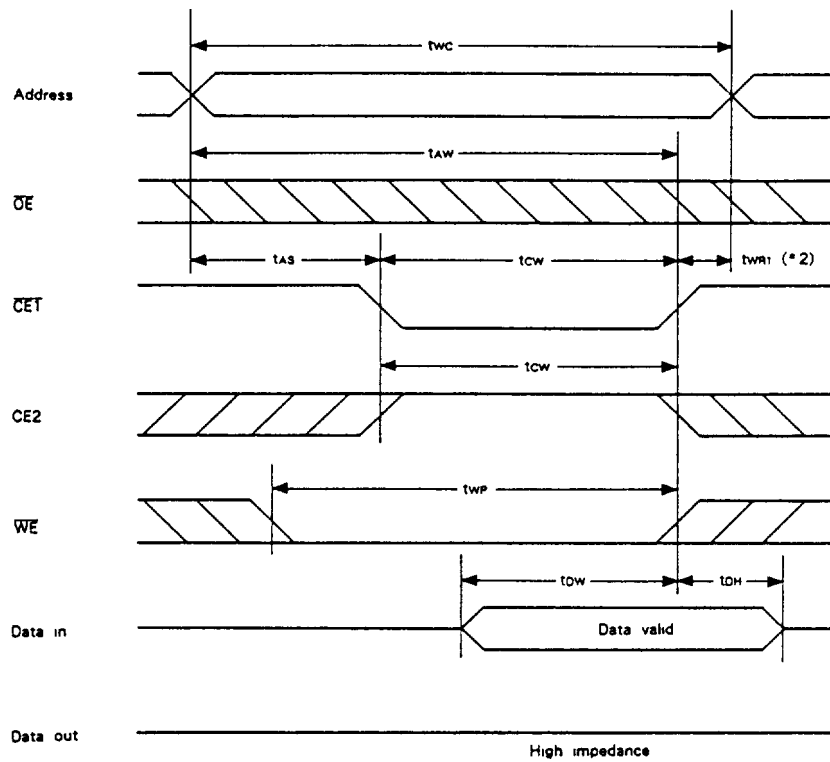
## ● Write cycle

Item	Symbol	-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>wc</sub>	70	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	60	—	75	—	ns
Chip enable to end of write	t <sub>cw</sub>	60	—	75	—	ns
Data to write time overlap	t <sub>dw</sub>	30	—	35	—	ns
Data hold from write time	t <sub>dH</sub>	0	—	0	—	ns
Write pulse width	t <sub>wP</sub>	45	—	60	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	ns
Write recovery time ( $\overline{CE1}$ , CE2)	t <sub>WR1</sub>	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	30	0	35	ns

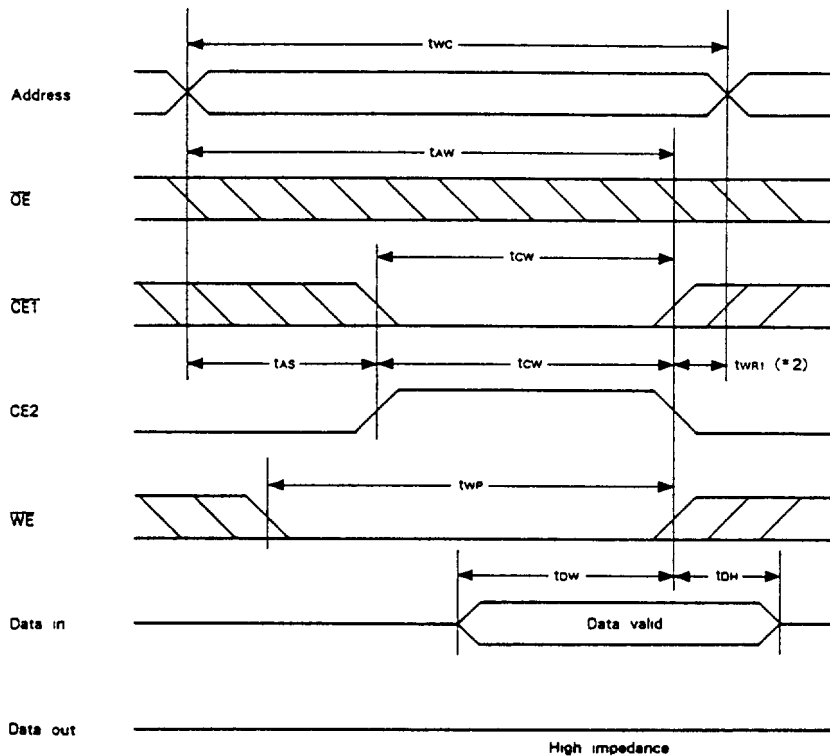
\* t<sub>WHZ</sub> is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.



• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) : CE2 control



Note)

- \* 1. Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and CE2 is at high simultaneously.
- \* 2.  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- \* 3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

**Data Retention Characteristics**

(Ta=0 to +70 °C)

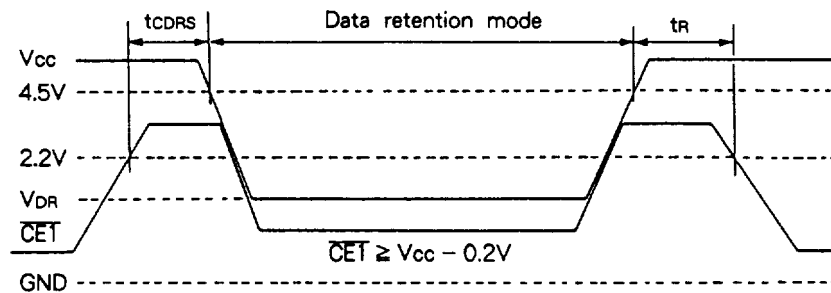
Item	Symbol	Test conditions	-70LL/10LL			Unit
			Min.	Typ.	Max.	
Data retention voltage	V <sub>DR</sub>	* 1	2.0	—	5.5	V
Data retention current	I <sub>CCDR1</sub>	* 1 V <sub>CC</sub> =3.0V	—	0.1	2.5	μA
		Ta=0 to 70 °C	—	—	0.5	
	I <sub>CCDR2</sub>	V <sub>CC</sub> =2.0 to 5.5V * 1	—	0.2	6	μA
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	ns
Recovery time	t <sub>R</sub>		t <sub>RC</sub> * 2	—	—	ns

\* 1.  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  [ $\overline{CE1}$  Control] or  $CE2 \leq 0.2V$  [CE2 Control]

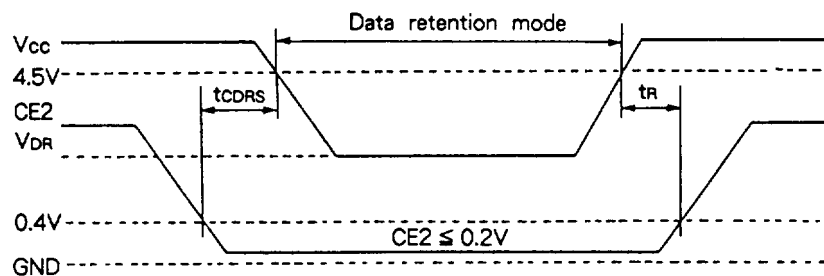
\* 2. t<sub>RC</sub>: Read cycle time

**Data Retention Waveform**

1.  $\overline{CE1}$  control



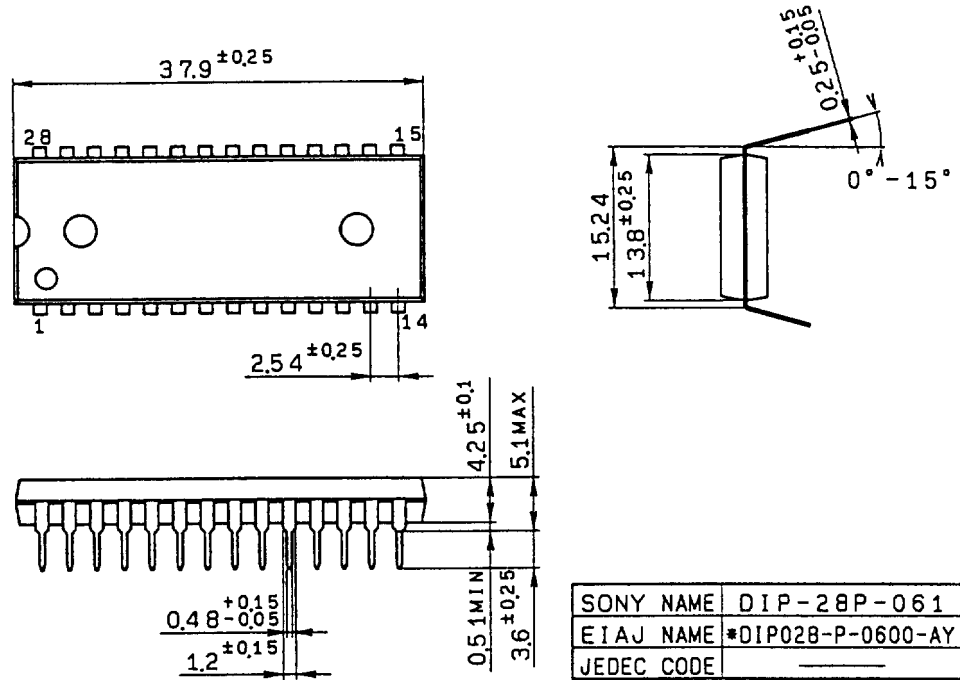
2. CE2 control



Package Outline Unit : mm

CXK5864CP

28pin DIP (Plastic) 600mil



CXK5864CM

28pin SOP (Plastic) 450mil 0.7g

