



GoldStar
GOLD STAR CO., LTD.

GM76C28

CMOS 16K-BIT STATIC RAM

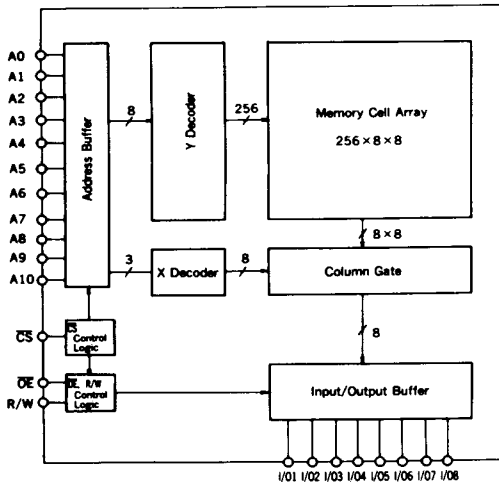
Description

The GM76C28_{10/12} is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

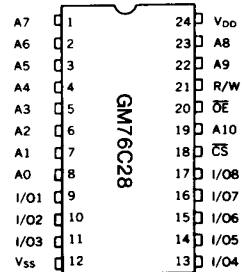
Features

- Access timeGM76C28-10 100ns (Max)
GM76C28-12 120ns (Max)
- Low supply currentstandby : 1μA (Typ)
operation :GM76C28-10 30mA (Typ)
GM76C28-12 25mA (Typ)
- Complete static operation
- Single power supply5V ±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries

Schematic Diagram



Pin Configuration



- | | |
|-----------|--------------------|
| A0 to A10 | Address Input |
| R/W | Read/Write |
| OE | Output Enable |
| CS | Chip Select |
| I/O1 to 8 | Data Input/Output |
| VDD | Power Supply (+5V) |
| Vss | Power Supply (0V) |

HEAD OFFICE
#20, YOIDO-DONG, YEONG DEUNG PO-GU, SEOUL, KOREA, 150
YOIDO P.O. BOX 335 SEOUL KOREA
TEL. INTERNATIONAL 787-3811~3819
DOMESTIC 787-3801~3807, INFORMATION 787-3114
TLX. GSRADIO K23751 SEOUL
FAX: 787-3400

SUNNYVALE
#1130 EAST ARQUES AVENUE SUNNYVALE, CA94086
TEL. (408) 737-8575
TLX. 176835 LKYGS SUVL
FAX: (408) 737-0186

Absolute Maximum Ratings

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
Input/output voltage*	V _{I/O}	-0.5 to V _{DD} +0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temp. & time	T _{sol}	260°C, 10s (at lead)	—

*V_I, V_{I/O} = -1.0V when pulse width is 50 ns

Recommended Operating Conditions

(T_a = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V _{DD}		4.5	5.0	5.5	V
	V _{SS}		0	0	0	V
Input voltage	V _{IH}		2.2	3.5	V _{DD} +0.3	V
	V _{IL}		-0.3*	—	0.8	V

*V_{IL}(Min) = -1.0V when pulse width is 50ns

Electrical Characteristics

DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Conditions	GM76C28-10			GM76C28-12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I _{LI}	V _{DD} = 5.5V, V _I = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CS = V _{IH} , or OE = V _{IH} , V _{I/O} = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Operating supply current	I _{DD0}	CS = V _{IL} , I _{I/O} = 0mA	—	30	60	—	25	50	mA
	I _{DD01}	V _{IH} = 3.5V, V _{IL} = 0.6V, I _{I/O} = 0mA	—	16	—	—	16	—	mA
Average operating current	I _{DDA}	Min. cycle, duty = 100%, I _{I/O} = 0mA	—	30	60	—	25	50	mA
Standby supply current	I _{DDS}	CS = V _{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I _{DDS1}	CS = V _{DD} - 0.2V	—	1	50	—	1	50	μA
Output voltage	V _{OL}	I _{OL} = 4.0mA	—	—	0.4	—	—	0.4	V
	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V

* Typical values are for reference, with V_{DD} = 5V and T_a = 25°C assumed

Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C _I	V _I = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	6	8	pF

AC Electrical Characteristics

Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Conditions	GM76C28-10		GM76C28-12		Unit
			Min	Max	Min	Max	
Read cycle time	t _{RC}		100	—	120	—	ns
Address access time	t _{ACC}	*1	—	100	—	120	ns
CS access time	t _{ACS}		—	100	—	120	ns
CS output setup time	t _{CLZ}	*2	10	—	10	—	ns
OE access time	t _{OE}	*1	—	55	—	60	ns
OE output setup time	t _{OLZ}		5	—	10	—	ns
CS output floating	t _{CHZ}	*2	0	40	0	40	ns
OE output floating	t _{OHZ}		0	40	0	40	ns
Output hold time	t _{OH}	*1	10	—	10	—	ns

Write Cycle

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $70^\circ C$)

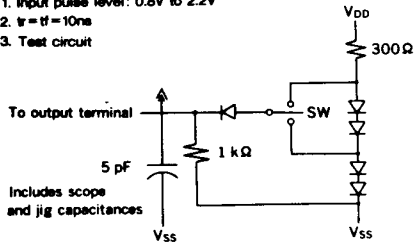
Parameter	Symbol	Conditions	GM76C28-10		GM76C28-12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{wc}	*1	100	—	120	—	ns
Chip select time (CS)	t_{cw}		80	—	85	—	ns
Address enable time	t_{aw}		80	—	85	—	ns
Address setup time	t_{as}		0	—	0	—	ns
Write pulse width	t_{wp}		65	—	70	—	ns
\overline{OE} output floating	t_{ohz}	*2	0	40	0	40	ns
R/W output floating	t_{whz}	*3	0	45	0	50	ns
Input data setup time	t_{dw}	*1	45	—	50	—	ns
Address hold time	t_{wr}		5	—	5	—	ns
Input data hold time	t_{dh}		0	—	0	—	ns
R/W output setup time	t_{ow}	*3	5	—	10	—	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Input/output timing reference level: 1.5V
4. Output load: $t_{m} + C_L = 100pF$

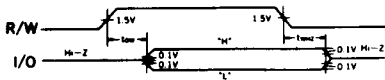
*3 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit



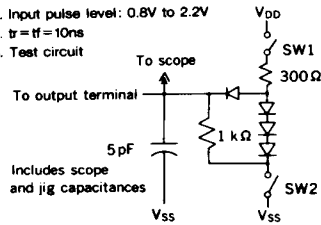
- SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of low or t_{we} .
- SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of low or t_{we} .

Output turnon turnoff times



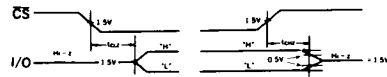
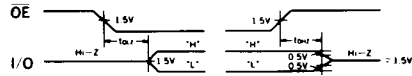
*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit



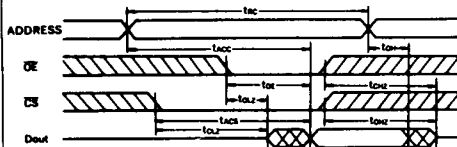
- Both SW1 and SW2 are closed when measuring t_{oz} or t_{oz} .
- SW1 is open and SW2 is closed when measuring Hi-z-high of t_{oz} or t_{oz} .
- SW1 is closed and SW2 is open when measuring Hi-z-low of t_{oz} or t_{oz} .

Output turnon turnoff times

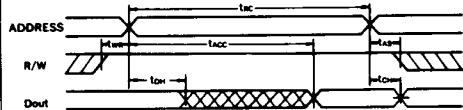


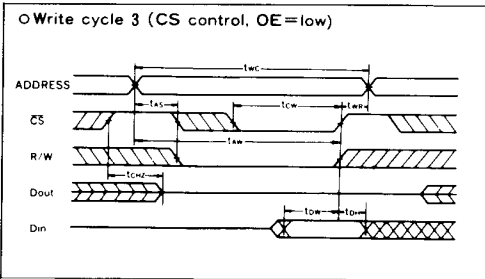
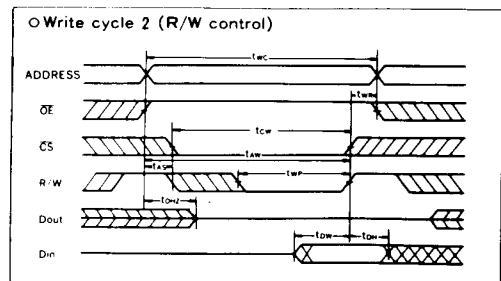
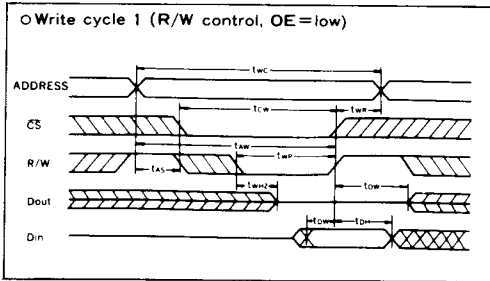
Timing Chart

○ Read cycle 1 (\overline{OE} , CS control, R/W=high)



○ Read cycle 2 (R/W control, \overline{OE} =low, CS=low)





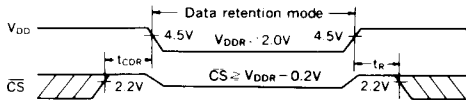
Data Retention Characteristics with Low Voltage Power Supply

(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDR}	$\overline{CS} \geq V_{DDR} - 0.2V$	2.0	—	5.5	V
Data retention current	I _{DDR}	V _{DD} = 3.0V, $\overline{CS} \geq 2.8V$	—	—	25	μA
Chip select data hold time	t _{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t _R		t _{RC} *	—	—	ns

* t_{RC} : read cycle time

Data retention timing



Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

Functions

Truth Table

CS	OE	R/W	A0 to A10	DATA I/O	Mode	I _{DD}
H	—	—	—	Hi-Z	Unselected	I _{DDS} , I _{DDSI}
L	L	H	Stable	Output data	Read	I _{DDO}
L	H	L	Stable	Input data	Write	I _{DDO}
L	L	L	Stable	Input data	Write	I _{DDO}

X: "H" or "L", —: "H", "L" or "Hi-Z"

Reading Data

Data can be read out if an address is set while \overline{CS} and \overline{OE} are held low, and R/W is held high.

Writing Data

There are following three ways of writing data.

- (1) Hold \overline{CS} low, set the address, and apply a low pulse to R/W.
- (2) Hold R/W low, set the address, and apply a low pulse to \overline{CS} .
- (3) Set the address, then apply low pulses to both \overline{CS} and R/W.

In any case, data from the DATA I/O terminal is fetched into the GM76C28_{10/12} at the last transition of a section in which both \overline{CS} and R/W are low. Because the DATA I/O terminal is in high-impedance state when \overline{CS} or \overline{OE} is high, or R/W is low, contention of data driver on the bus and memory output is avoided.

Standby Mode

When \overline{CS} is high, GM76C28 is in standby mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/W signal, or data is prohibited. When \overline{CS} is above $V_{DD} - 0.2V$, current flow within the GM76C28 chip is only that in the high-resistance portion of memory cells and leakage current.

Characteristics Curves

