M5L 2114L P, S; P-2, S-2; P-3, S-3

4096-BIT (1024-WORD BY 4-BIT) STATIC RAM

DESCRIPTION

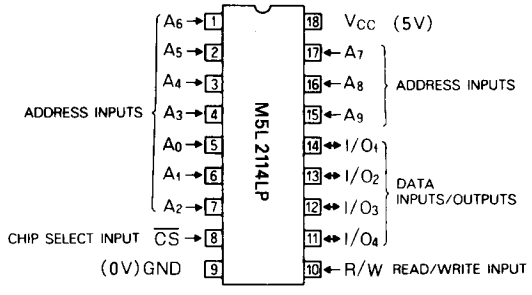
This is a family of 4096-bit static RAMs organized as 1024 words of 4 bits and designed for simple interfacing. They are fabricated using N-channel silicon-gate MOS technology. They operate with a single 5V supply, as does TTL, and the inputs and outputs are directly TTL compatible. I/O terminals are common.

FEATURES

Parameter	M5L 2114LP, S-2	M5L 2114LP, S-3	M5L 2114LP, S
Access time (max)	200ns	300ns	450ns
Cycle time (min)	200ns	300ns	450ns

- Low power dissipation: 50μw/bit (typ)
- Single 5V supply voltage (±10% tolerance)
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- All outputs are three-state, with OR-tie capability
- Easy memory expansion by chip-select ($\overline{CS}$) input
- Common data I/O terminals
- Interchangeable with Intel's 2114L and TI's TMS4045 in pin configuration and electrical characteristics

PIN CONFIGURATION (TOP VIEW)



Outline 18P1 (M5L 2114LP)
18S1 (M5L 2114LS)

APPLICATION

- Small-capacity memory units

FUNCTION

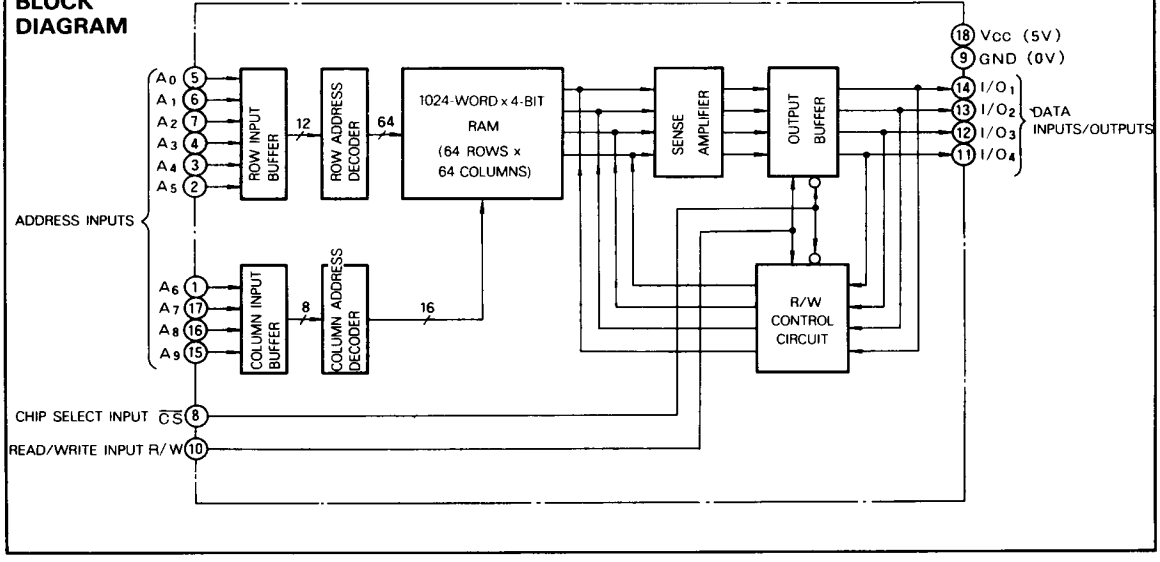
These devices operate with a single 5V power supply, and the inputs and outputs are directly compatible with TTL. All circuits are completely static, rendering external clock and refresh operations unnecessary, and making the members of the series extremely easy to use. Common data input and output terminals are provided.

During a write cycle, when a location is designated by address signals $A_0 \sim A_9$ and the R/W signal goes low, the data at the I/O terminals is written.

During a read cycle, when the R/W signal goes high and a location is designated by address signals $A_0 \sim A_9$, the data of the designated address is available at the I/O terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the data outputs are in the floating (high-impedance) state, useful for OR-ties with the output terminals of other chips.

BLOCK DIAGRAM



M5L 2114L P, S; P-2, S-2; P-3, S-3

4096-BIT (1024-WORD BY 4-BIT) STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.5～7	V
V_I	Input voltage			−0.5～7	V
V_O	Output voltage			−0.5～7	V
P_d	Maximum power dissipation	M5L 2114L P	T_a=25℃	700	mW
		M5L 2114L S	T_a=25℃	1000	mW
T_{opr}	Operating free-air ambient temperature range			0～70	℃
T_{stg}	Storage temperature range	M5L 2114L P		−40～125	℃
		M5L 2114L S		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (T_a = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −200μA, V_{CC} = 4.5V	2.4			V
V_{OH}	High-level output voltage	I_{OH} = −1mA, V_{CC} = 4.75V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA			0.4	V
I_I	Input current	V_I = 0～5.5V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I = 5.5V, (all inputs), output open, T_a = 25℃		40	65	mA
C_I	Input capacitance, all inputs	V_I = GND, V_i = 25mVrms, f = 1MHz		3	5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz		5	8	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (T_a = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	Alt. symbol	M5L 2114L P-2, S-2			M5L 2114L P-3, S-3			M5L 2114L P, S			Unit
			Limits			Limits			Limits			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	t_{WC}	200			300			450			ns
$t_{su(AD)}$	Address setup time with respect to write pulse		0			0			0			ns
$t_{w(WR)}$	Write pulse width	t_W	120			150			200			ns
t_{wr}	Write recovery time	t_{WR}	0			0			0			ns
$t_{su(DA)}$	Data setup time	t_{DW}	120			150			200			ns
$t_{h(DA)}$	Data hold time	t_{DH}	0			0			0			ns
$t_{su(\overline{CS})}$	Chip select setup time		120			150			200			ns
$t_{PXZ(WR)}$	Output disable time with respect to write pulse	t_{OTW}			40			80			100	ns

SWITCHING CHARACTERISTICS (For Read Cycle) (T_a = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	Alt. symbol	M5L 2114L P, S-2			M5L 2114L P, S-3			M5L 2114L P, S			Unit
			Limits			Limits			Limits			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	t_{RC}	200			300			450			ns
$t_{a(AD)}$	Address access time	t_A			200			300			450	ns
$t_{a(\overline{CS})}$	Chip select access time	t_{CO}			80			100			120	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select	t_{OTD}			40			80			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	t_{OHA}	50			50			50			ns
$t_{PZX(\overline{CS})}$	Chip select to output active	t_{CX}	20			20			20			ns

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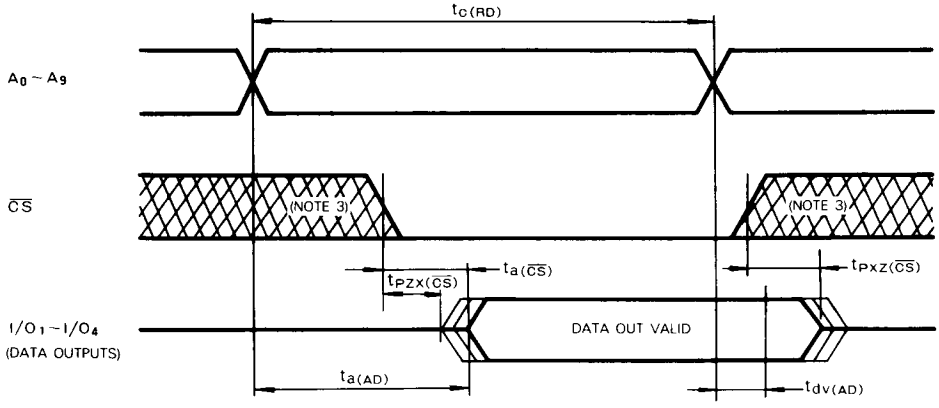
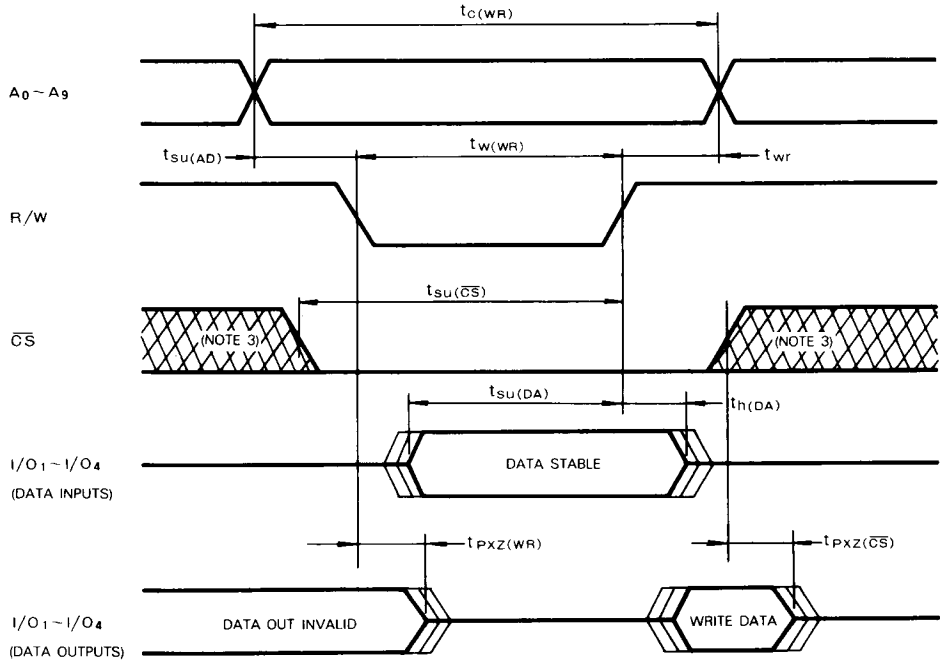
TIMING DIAGRAMS

Read Cycle



Write Cycle

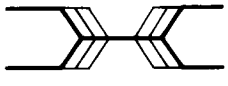


Note : 2 Test conditions

Input pulse level	0.8~2V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level	
Input	1.5V
Output	1.5V

Load = 1TTL, C_L = 100pF

Note 3 : Hatching indicates the state is don't care.

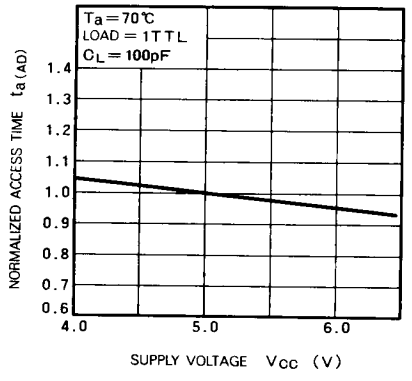


The center line indicates a floating (high-impedance) state.

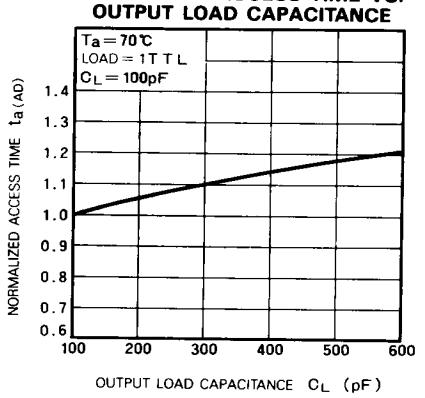
4096-BIT (1024-WORD BY 4-BIT) STATIC RAM

TYPICAL CHARACTERISTICS

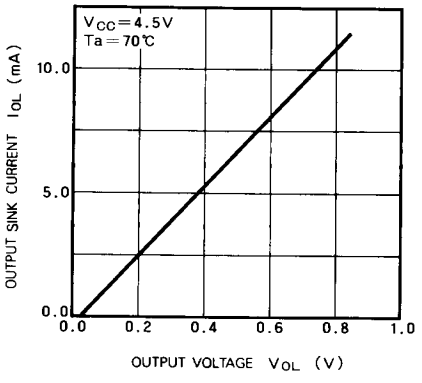
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



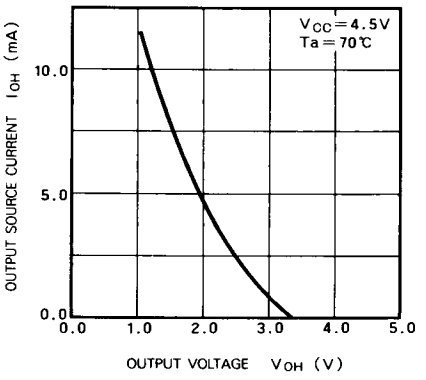
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



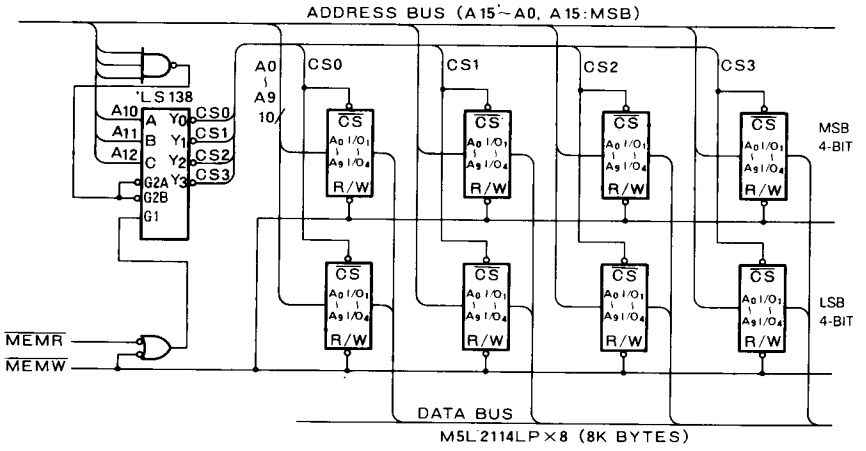
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL APPLICATION (for an M5L8080A P CPU)



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